TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74HCT574AP, TC74HCT574AF, TC74HCT574AFW

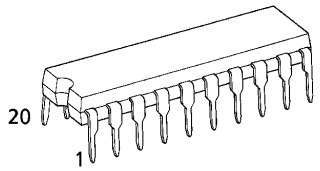
OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUT

(Note) The JEDEC SOP (FW) is not available in Japan.

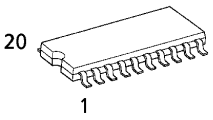
The TC74HCT574A is a high speed CMOS OCTAL FLIP-FLOP with 3-STATE OUTPUT fabricated with silicon gate C^2MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
Its inputs are compatible with TTL, NMOS, and CMOS output voltage levels.
Its 8-bit D-type flip-flops is controlled by a clock input (CK) and an output enable input ($\overline{OE}$).
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

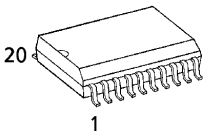
- High Speed ····· f_{MAX} = 62MHz (typ.) at V_{CC} = 5V
- Low Power Dissipation ····· I_{CC} = 4μA(Max.) at Ta = 25°C
- Compatible with TTL outputs ···· V_{IL} = 0.8V (Min.), V_{IH} = 2.0V (Max.)
- Output Drive Capability ····· 15 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}| = I_{OL}$ = 6mA (Min.)
- Balanced Propagation Delays ····· $t_{pLH} \simeq t_{pHL}$
- Pin and Function Compatible with 74LS574



P (DIP20-P-300-2.54A)
Weight : 1.30g (Typ.)

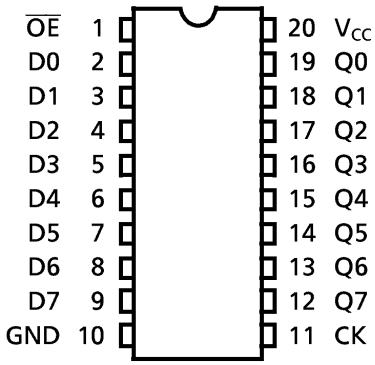


F (SOP20-P-300-1.27)
Weight : 0.22g (Typ.)



FW (SOL20-P-300-1.27)
Weight : 0.46g (Typ.)

PIN ASSIGNMENT



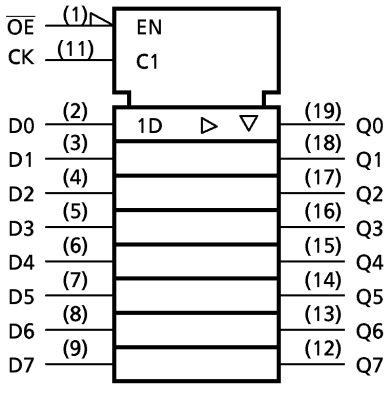
(TOP VIEW)

TRUTH TABLE

INPUTS			OUTPUT
$\overline{OE}$	CK	D	Q
H	X	X	Z
L	↓	X	Q_n
L	↑	L	L
L	↑	H	H

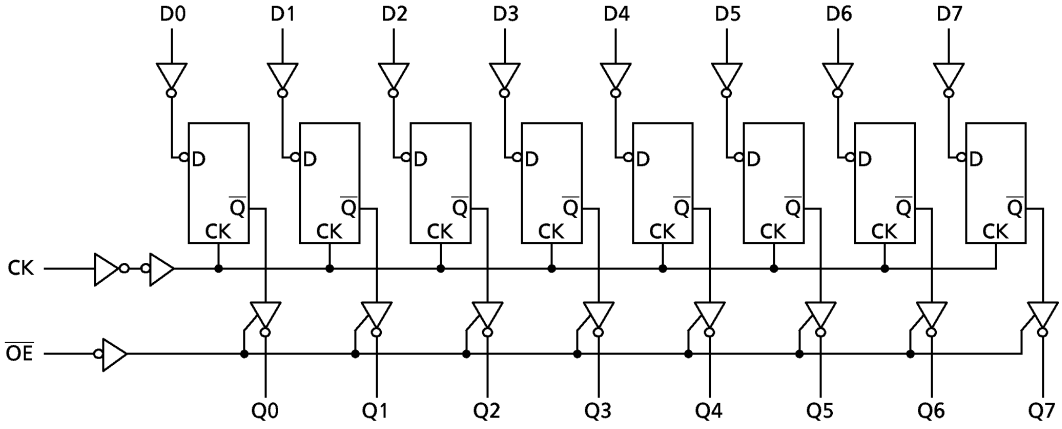
X : Don't Care
Z : High Impedance
Q_n : No Change

IEC LOGIC SYMBOL



980508EBA2

SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7	V
DC Input Voltage	V_{IN}	−0.5~V_{CC} + 0.5	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC} + 0.5	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 35	mA
DC V_{CC}/ Ground Current	I_{CC}	± 75	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	T_{stg}	−65~150	°C

*500mW in the range of Ta = −40°C~65°C. From Ta = 65°C to 85 °C a derating factor of −10mW/ °C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	t_r, t_f	0~500	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C			Ta = −40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	—	—	2.0	—	V
Low - Level Input Voltage	V_{IL}			4.5 ~ 5.5	—	—	0.8	—	0.8	V
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −20 μA	4.5	4.4	4.5	—	4.4	—	V
			I_{OH} = −6 mA	4.5	4.18	4.31	—	4.13	—	
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20 μA	4.5	—	0.0	0.1	—	0.1	V
			I_{OL} = 6 mA	4.5	—	0.17	0.26	—	0.33	
3 - State Output Off - State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		5.5	—	—	± 0.5	—	± 5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		5.5	—	—	± 0.1	—	± 1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	—	4.0	—	40.0	μA
	I_C	Per input: V_{IN} = 0.5V or 2.4V Other input: V_{CC} or GND		5.5	—	—	2.0	—	2.9	mA

TIMING REQUIREMENTS (Input $t_r = t_f = 6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C TYP.	Ta = 25°C LIMIT	Ta = −40~85°C LIMIT	UNIT
Minimum Pulse Width (CK)	$t_{W(H)}$ $t_{W(L)}$		4.5 5.5	— —	15 14	19 17	ns
Minimum Set−up Time (Dn)	t_s		4.5 5.5	— —	15 14	19 17	
Minimum Hold Time (Dn)	t_h		4.5 5.5	— —	0 0	0 0	
Clock Frequency	f		4.5 5.5	— —	31 34	25 27	MHz

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 6ns$)

PARAMETER	SYMBOL	TEST CONDITION	CL (pF)	V_{CC} (V)	Ta = 25°C MIN.	Ta = 25°C TYP.	Ta = 25°C MAX.	Ta = −40~85°C MIN.	Ta = −40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		50	4.5 5.5	— —	7 6	12 11	— —	15 14	ns
Propagation Delay Time (CK−Q)	t_{pLH} t_{pHL}		50	4.5 5.5	— —	19 16	30 27	— —	38 34	
			150	4.5 5.5	— —	24 21	40 35	— —	48 44	
Output Enable time	t_{pZL} t_{pZH}	$R_L = 1k\Omega$	50	4.5 5.5	— —	19 16	30 27	— —	38 34	
			150	4.5 5.5	— —	24 21	40 35	— —	48 44	
Output Disable time	t_{pLZ} t_{pHZ}	$R_L = 1k\Omega$	50	4.5 5.5	— —	19 16	30 27	— —	38 34	
Maximum Clock Frequency	f_{MAX}		50	4.5 5.5	31 34	50 60	— —	25 27	— —	MHz
Input Capacitance	C_{IN}				—	5	10	—	10	pF
Output Capacitance	C_{OUT}				—	10	—	—	—	
Power Dissipation Capacitance	C_{PD} (1)				—	62	—	—	—	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

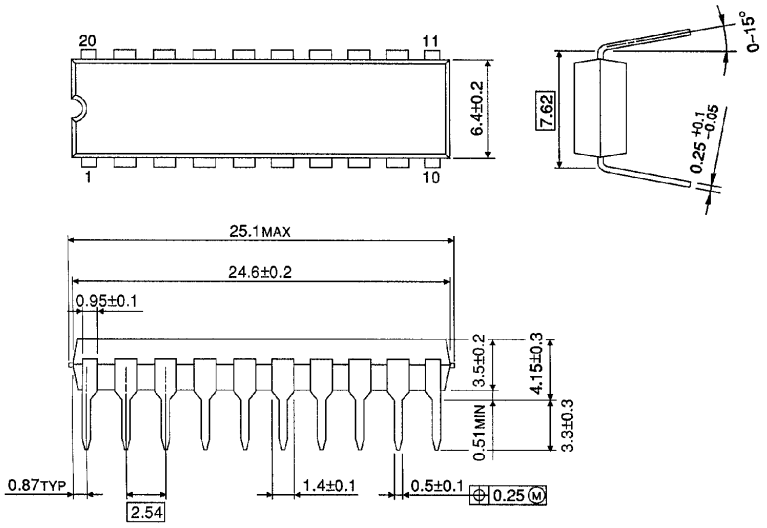
Average operating current can be obtained by the equation :

$$I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 8 \text{ (per bit)}$$

And the total C_{PD} when n pcs. of Flip flop operate can be gained by the following equation:

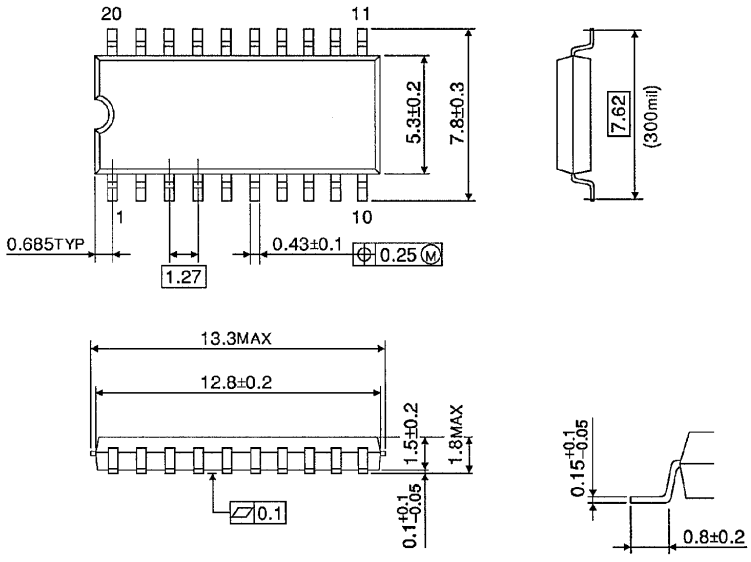
$$C_{PD}(total) = 47 + 15 \cdot n$$

DIP 20PIN OUTLINE DRAWING (DIP20-P-300-2.54A) Unit in mm



Weight : 1.30g (Typ.)

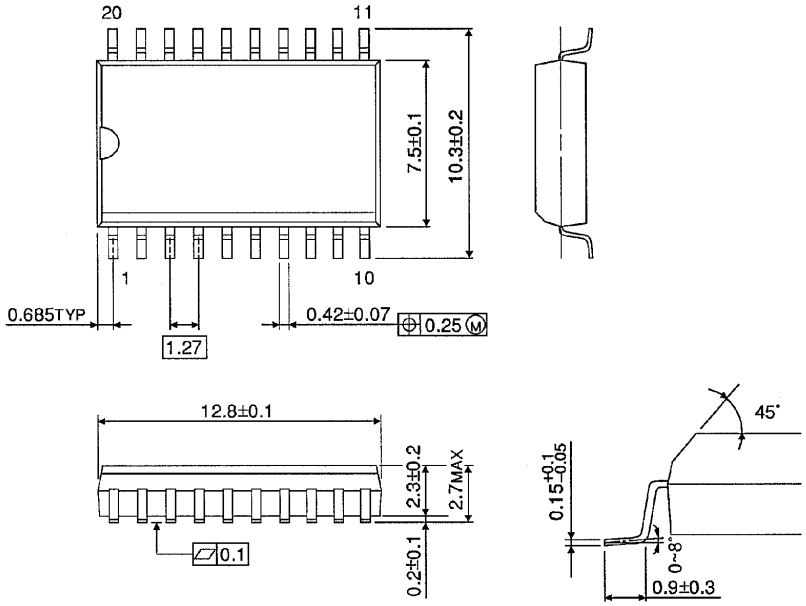
SOP 20PIN (200mil BODY) OUTLINE DRAWING (SOP20-P-300-1.27) Unit in mm



Weight : 0.22g (Typ.)

SOP 20PIN (300mil BODY) OUTLINE DRAWING (SOL20-P-300-1.27) Unit in mm

(Note) This package is not available in Japan.



Weight : 0.46g (Typ.)