

$\mathbf{QFET}^{\scriptscriptstyle{\mathsf{M}}}$

FQP9N50C/FQPF9N50C

500V N-Channel MOSFET

General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction, electronic lamp ballasts based on half bridge topology.

Features

- 9 A, 500V, $R_{DS(on)} = 0.8 \Omega @V_{GS} = 10 V$
- Low gate charge (typical 28 nC)
- Low Crss (typical 24 pF)
- Fast switching
- 100% avalanche tested
- · Improved dv/dt capability



Absolute Maximum Ratings $T_C = 25$ °C unless otherwise noted

Symbol	Parameter		FQP9N50C	FQPF9N50C	Units
V _{DSS}	Drain-Source Voltage		500		V
I _D	Drain Current - Continuous (T _C = 25°C	;)	9	9 *	Α
	- Continuous (T _C = 100°	C)	5.4	5.4 *	Α
I _{DM}	Drain Current - Pulsed	(Note 1)	36	36 *	Α
V _{GSS}	Gate-Source Voltage		± 30		V
E _{AS}	Single Pulsed Avalanche Energy (Note 2)		360		mJ
I _{AR}	Avalanche Current	(Note 1)		9	Α
E _{AR}	Repetitive Avalanche Energy (Note 1)		13.5		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		4.5		V/ns
P_D	Power Dissipation (T _C = 25°C)		135	44	W
	- Derate above 25°C		1.07	0.35	W/°C
T _J , T _{STG}	Operating and Storage Temperature Range		-55 to +150		°C
T _L	Maximum lead temperature for soldering purposes,		300		°C
'L	1/8" from case for 5 seconds				

^{*} Drain current limited by maximum junction temperature

Thermal Characteristics

Symbol	Parameter	FQP9N50C	FQPF9N50C	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.93	2.86	°C/W
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink Typ.	0.5		°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	62.5	°C/W

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Cha	aracteristics					
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	500			V
ΔBV _{DSS} / ΔΤ _J	Breakdown Voltage Temperature Coefficient	I_D = 250 μ A, Referenced to 25°C		0.57		V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 500 V, V _{GS} = 0 V			1	μΑ
		V _{DS} = 400 V, T _C = 125°C			10	μΑ
I _{GSSF}	Gate-Body Leakage Current, Forward	V _{GS} = 30 V, V _{DS} = 0 V			100	nA
I _{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -30 \text{ V}, V_{DS} = 0 \text{ V}$			-100	nA
On Cha	racteristics					
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$	2.0		4.0	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = 10 V, I _D = 4.5 A		0.65	0.8	Ω
9 _{FS}	Forward Transconductance	$V_{DS} = 40 \text{ V}, I_D = 4.5 \text{ A}$ (Note 4)		6.5		S
	ic Characteristics	T		700	1000	
Ciss	Input Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$		790	1030	pF
Coss	Output Capacitance	f = 1.0 MHz		130	170	pF
C _{rss}	Reverse Transfer Capacitance			24	30	pF
Switchi	ing Characteristics					
t _{d(on)}	Turn-On Delay Time	V _{DD} = 250 V, I _D = 9 A,		18	45	ns
t _r	Turn-On Rise Time	$R_G = 25 \Omega$		65	140	ns
t _{d(off)}	Turn-Off Delay Time			93	195	ns
t _f	Turn-Off Fall Time	(Note 4, 5)		64	125	ns
Q_g	Total Gate Charge	$V_{DS} = 400 \text{ V}, I_{D} = 9 \text{ A},$		28	35	nC
Q_{gs}	Gate-Source Charge	V _{GS} = 10 V		4		nC
Q_{gd}	Gate-Drain Charge	(Note 4, 5)		15		nC
Drain-S	Source Diode Characteristics a	nd Maximum Ratings				
I _S	Maximum Continuous Drain-Source Diode Forward Current				9	Α
I _{SM}	Maximum Pulsed Drain-Source Diode F	Forward Current			36	Α
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 9 A			1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = 9 A,		335		ns
Q _{rr}	Reverse Recovery Charge	$dI_F / dt = 100 A/\mu s$ (Note 4)		2.95		μС

- Notes:
 1. Repetitive Rating : Pulse width limited by maximum junction temperature 2. L = 8 mH, I_{AS} = 9A, V_{DD} = 50V, R_G = 25 Ω, Starting T_J = 25°C 3. I_{SD} ≤ 9A, di/dt ≤ 200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C 4. Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2% 5. Essentially independent of operating temperature

Typical Characteristics

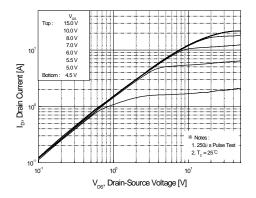


Figure 1. On-Region Characteristics

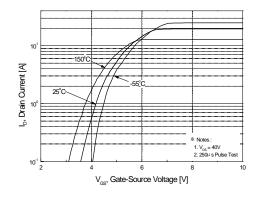


Figure 2. Transfer Characteristics

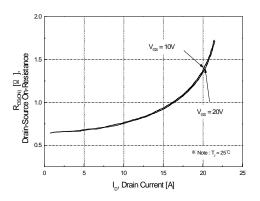


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

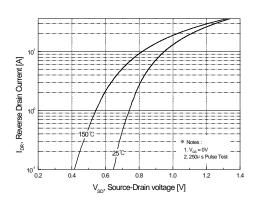


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

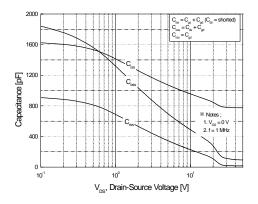


Figure 5. Capacitance Characteristics

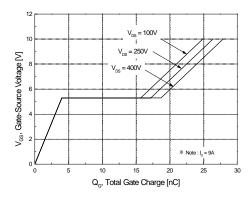


Figure 6. Gate Charge Characteristics

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Typical Characteristics (Continued)

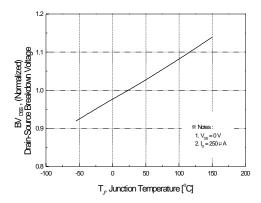


Figure 7. Breakdown Voltage Variation vs Temperature

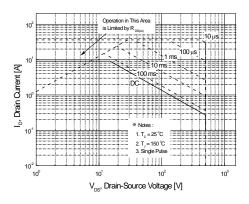


Figure 9-1. Maximum Safe Operating Area for FQP9N50C

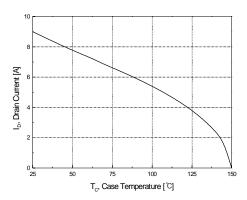


Figure 10. Maximum Drain Current vs Case Temperature

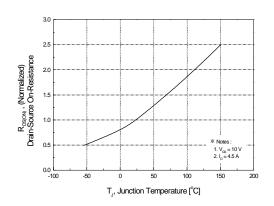


Figure 8. On-Resistance Variation vs Temperature

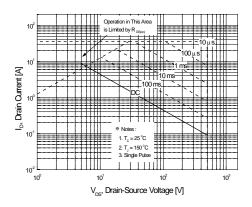


Figure 9-2. Maximum Safe Operating Area for FQPF9N50C

Typical Characteristics (Continued)

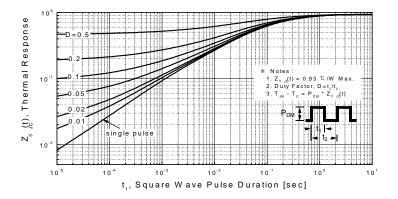


Figure 11-1. Transient Thermal Response Curve for FQP9N50C

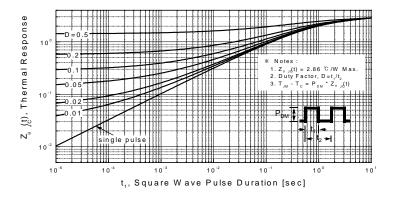
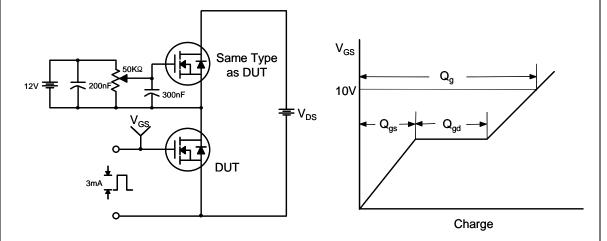


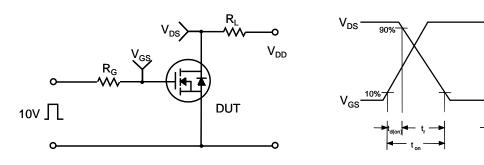
Figure 11-2. Transient Thermal Response Curve for FQPF9N50C

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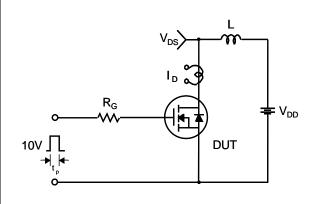
Gate Charge Test Circuit & Waveform

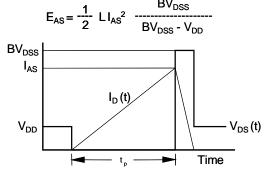


Resistive Switching Test Circuit & Waveforms

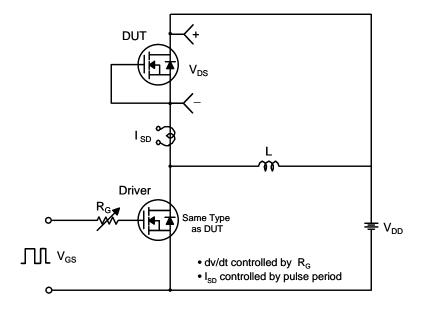


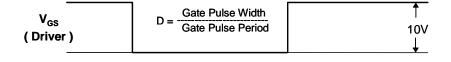
Unclamped Inductive Switching Test Circuit & Waveforms

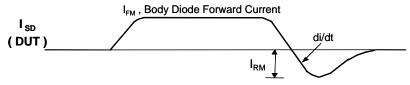




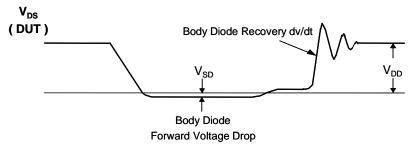
Peak Diode Recovery dv/dt Test Circuit & Waveforms

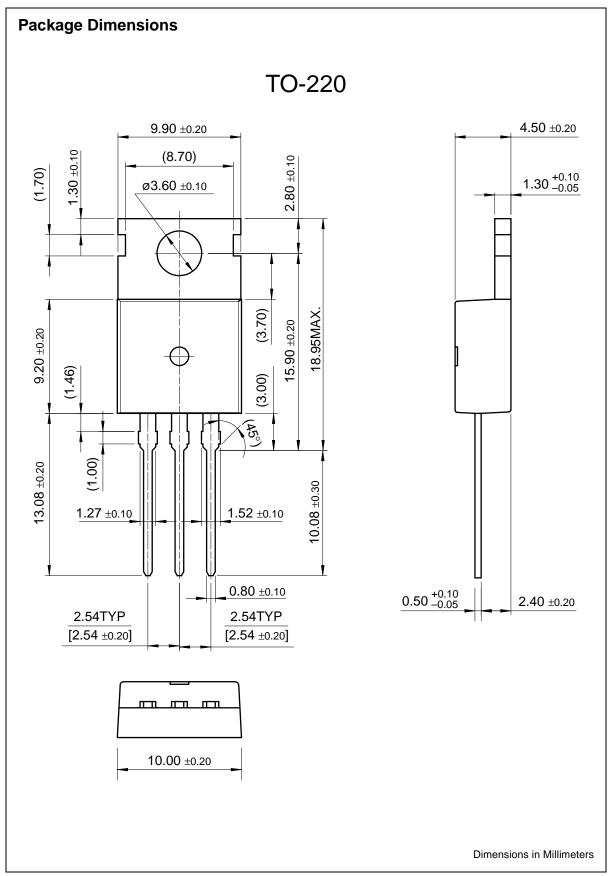


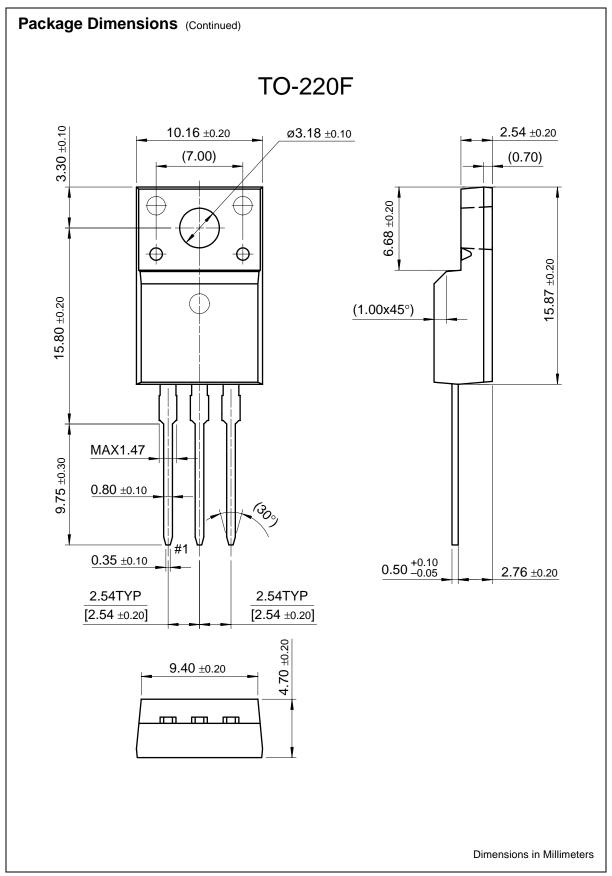




Body Diode Reverse Current







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