MC10EP142, MC100EP142

3.3V / 5V ECL 9-Bit Shift Register

The MC10EP/100EP142 is a 9-bit shift register, designed with byte-parity applications in mind. The MC10/100EP142 is capable of performing serial/parallel data into serial/parallel out and shifting in only one direction. The nine inputs D0 - D8 accept parallel input data, while S-IN accepts serial input data. The QT0:87 outputs do not need to be terminated for the shift operation to function. To minimize power, any Q output not used should be left unterminated.

The SEL (Select) input pin is used to switch between the two modes of operation - SHIFT and LOAD. The shift direction is from bit 0 to bit 8. Input data is accepted by the registers a set-up time before the positive going edge of CLK0 or CLK1; shifting is also accomplished on the positive clock edge. A HIGH on the Master Reset pin (MR) asynchronously resets all the resisters to zero.

The 100 Series contains temperature compensation.

- Minimum Shift Frequency >3 GHz (Typical)
- 9-Bit for Byte-Parity Applications
- Asynchronous Master Reset
- Dual Clocks
- PECL Mode Operating Range: V_{CC} = 3.0 V to 5.5 V with V_{EE} = 0 V
- NECL Mode Operating Range: V_{CC} = 0 V with V_{EE} = -3.0 V to -5.5 V
- Open Input Default State
- Safety Clamp on Inputs

ON Semiconductor®

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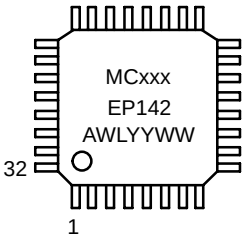
MARKING DIAGRAM*

LQFP-32
FA SUFFIX
CASE 873A



xxx = 10 or 100
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*For additional information, refer to Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC10EP142FA	LQFP-32	250 Units/Tray
MC10EP142FAR2	LQFP-32	2000/Tape & Reel
MC100EP142FA	LQFP-32	250 Units/Tray
MC100EP142FAR2	LQFP-32	2000/Tape & Reel

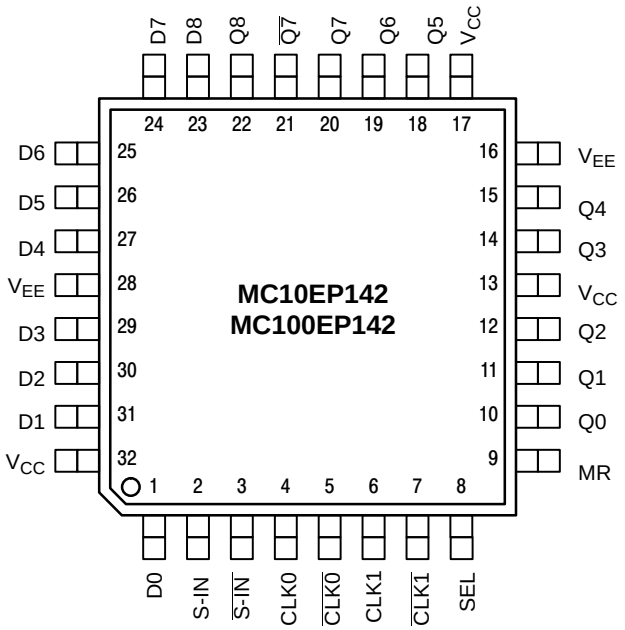


Figure 1. 32-Lead LQFP Pinout (Top View)

Table 1. Pin Description

Pin	Name	I/O	Default State	Description
1,23,24,25,26, 27,29,30,31	D[0:8]	ECL Input	Low	Single-Ended Parallel Data Inputs [0:8]. Internal 75 kΩ to V_{EE}.
2	S-IN	ECL Input	Low	Noninverted Differential Serial Input. Internal 75 kΩ to V_{EE}.
3	$\overline{\text{S-IN}}$	ECL Input	High	Inverted Differential Serial Input. Internal 75 kΩ to V_{EE} and 36.5 kΩ to V_{CC}.
4	CLK0	ECL Input	Low	Noninverted Differential CLK0 Input. Internal 75 kΩ to V_{EE}.
5	$\overline{\text{CLK0}}$	ECL Input	High	Inverted Differential CLK0B Input. Internal 75 kΩ to V_{EE} and 36.5 kΩ to V_{CC}.
6	CLK1	ECL Input	Low	Noninverted Differential CLK1 Input. Internal 75 kΩ to V_{EE}.
7	$\overline{\text{CLK1}}$	ECL Input	High	Inverted Differential CLK1B Input. Internal 75 kΩ to V_{EE} and 36.5 kΩ to V_{CC}.
8	SEL	ECL Input	Low	Single-Ended Select Logic Input. Internal 75 kΩ to V_{EE}.
9	MR	ECL Input	Low	Single-Ended Master Reset Logic Input. Internal 75 kΩ to V_{EE}.
10,11,12,14,1 5,18,19,22	Q0,Q1,Q2,Q3, Q4,Q5,Q6,Q8	ECL Output	-	Single-Ended parallel Data outputs [0,1,2,3,4,5,6,8]. Typically Terminated with 50 Ω to $V_{TT} = V_{CC}$ - 2 V.
13,17,32	V_{CC}	-	-	Positive supply Voltage. All V_{CC} Pins must be Externally Connected to Power Supply to Guarantee Proper Operation.
16,28	V_{EE}	-	-	Negative supply Voltage. All V_{EE} Pins must be Externally connected to Power Supply to Guarantee Proper Operation.
20	Q7	ECL Output	-	Noninverted Differential parallel/Serial Data Output 7. Typically Terminated with 50 Ω to $V_{TT} = V_{CC}$ - 2 V.
21	$\overline{\text{Q7}}$	ECL Output	-	Inverted Differential parallel/Serial Data Output 7. Typically Terminated with 50 Ω to $V_{TT} = V_{CC}$ - 2 V.

1. All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Table 2. TRUTH TABLE

Function (Note 2)	SEL	S-IN	MR	CLK0	CLK1	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Q9
Load	L	X	L	Z	Z	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9
Shift	H	L	L	Z	Z	L	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
	H	H	L	Z	Z	H	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
Reset	X	X	H	Z	Z	L	L	L	L	L	L	L	L	L	L

2. All functions are accomplished on the positive edge of CLK0 or CLK1.

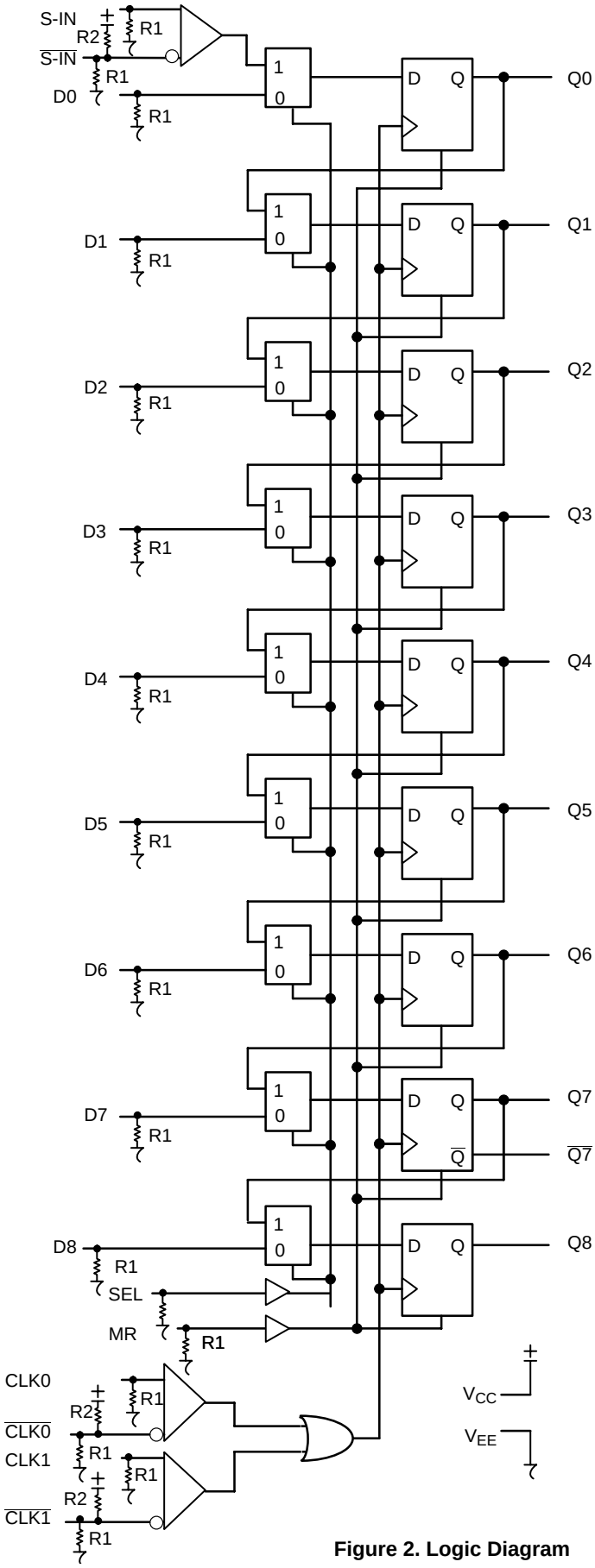


Figure 2. Logic Diagram

Table 3. ATTRIBUTES

Characteristics		Value
Internal Input Pulldown Resistor	(R1)	75 kΩ
Internal Input Pullup Resistor	(R2)	37.5 kΩ
ESD Protection	Human Body Model Machine Model Charged Device Model	> 2 kV > 100 V > 2 kV
Moisture Sensitivity (Note 3)		Level 2
Flammability Rating	Oxygen Index: 28 to 34	UL-94 V-0 @ 0.125 in
Transistor Count		405 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

3. For additional information, refer to Application Note AND8003/D.

Table 4. MAXIMUM RATINGS (Note 4)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	Positive Power Supply	V_{EE} = 0 V		8	V
V_{EE}	Negative Power Supply	V_{CC} = 0 V		-8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 -6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
T_A	Operating Temperature Range			-40 to +85	°C
T_{stg}	Storage Temperature Range			-65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 LFPM 500 LFPM	32 LQFP 32 LQFP	80 55	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	std bd	32 LQFP	12 to 17	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

4. Maximum Ratings are those values beyond which device damage may occur.

Table 5. 10EP DC CHARACTERISTICS, PECL V_{CC} = 3.3 V, V_{EE} = 0 V (Note 5)

Symbol	Characteristic	-40 °C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Negative Power Supply Current	105	125	145	105	125	145	105	125	145	mA
V_{OH}	Output HIGH Voltage (Note 6)	2165	2290	2415	2230	2355	2480	2290	2415	2540	mV
V_{OL}	Output LOW Voltage (Note 6)	1365	1490	1615	1430	1555	1680	1490	1615	1740	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	2090		2415	2155		2480	2215		2540	mV
V_{IL}	Input LOW Voltage (Single-Ended)	1365		1690	1460		1755	1490		1815	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 7)	2.0		3.3	2.0		3.3	2.0		3.3	V
I_{IH}	Input HIGH Current (@ V_{IH})			150			150			150	μA
I_{IL}	Input LOW Current (@ V_{IL}) $\overline{CLK0}$, $\overline{CLK1}$, D, $\overline{S\text{-}IN}$ CLK0, CLK1, $\overline{D}$, S-IN	 0.5 -150			 0.5 -150			 0.5 -150			μA

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

5. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.3 V to -2.2 V.
6. All loading with 50 Ω to V_{CC}-2.0 V.
7. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 6. 10EP DC CHARACTERISTICS, PECL V_{CC} = 5.0 V, V_{EE} = 0 V (Note 8)

		-40 °C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{EE}	Negative Power Supply Current (Note 9)	105	125	145	105	125	145	105	125	145	mA
V_{OH}	Output HIGH Voltage (Note 10)	3865	3990	4115	3930	4055	4180	3990	4115	4240	mV
V_{OL}	Output LOW Voltage (Note 10)	3065	3190	3315	3130	3255	3380	3190	3315	3440	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	3790		4115	3855		4180	3915		4240	mV
V_{IL}	Input LOW Voltage (Single-Ended)	3065		3390	3130		3455	3190		3515	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 11)	2.0		5.0	2.0		5.0	2.0		5.0	V
I_{IH}	Input HIGH Current (@ V_{IH})			150			150			150	μA
I_{IL}	Input LOW Current (@ V_{IL}) $\overline{CLK0}$, CLK1, D, S-IN CLK0, $\overline{CLK1}$, $\overline{D}$, $\overline{S\text{-}IN}$	0.5 -150			0.5 -150			0.5 -150			μA

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

8. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +2.0 V to -0.5 V.
9. Required 500 lfpm air flow when using +5 V power supply. For (V_{CC} - V_{EE}) >3.3 V, 5 Ω to 10 Ω in line with V_{EE} required for maximum thermal protection at elevated temperatures. Recommend V_{CC} - V_{EE} operation at $\leq$ 3.3 V.
10. All loading with 50 Ω to V_{CC}-2.0 V.
11. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 7. 10EP DC CHARACTERISTICS, NECL V_{CC} = 0 V, V_{EE} = -5.5 V to -3.0 V (Note 12)

		-40 °C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{EE}	Negative Power Supply Current (Note 13)	105	125	145	105	125	145	105	125	145	mA
V_{OH}	Output HIGH Voltage (Note 14)	-1135	-1010	-885	-1070	-945	-820	-1010	-885	-760	mV
V_{OL}	Output LOW Voltage (Note 14)	-1935	-1810	-1685	-1870	-1745	-1620	-1810	-1685	-1560	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	-1210		-885	-1145		-820	-1085		-760	mV
V_{IL}	Input LOW Voltage (Single-Ended)	-1935		-1610	-1870		-1545	-1810		-1485	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 15)	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V
I_{IH}	Input HIGH Current (@ V_{IH})			150			150			150	μA
I_{IL}	Input LOW Current (@ V_{IL}) $\overline{CLK0}$, CLK1, D, S-IN CLK0, $\overline{CLK1}$, $\overline{D}$, $\overline{S\text{-}IN}$	0.5 -150			0.5 -150			0.5 -150			μA

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

12. Input and output parameters vary 1:1 with V_{CC}.
13. Required 500 lfpm air flow when using -5 V power supply. For (V_{CC} - V_{EE}) >3.3 V, 5 Ω to 10 Ω in line with V_{EE} required for maximum thermal protection at elevated temperatures. Recommend V_{CC}-V_{EE} operation at $\leq$ 3.3 V.
14. All loading with 50 Ω to V_{CC} - 2.0 V.
15. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 8. 100EP DC CHARACTERISTICS, PECL V_{CC} = 3.3 V, V_{EE} = 0 V (Note 16)

Symbol	Characteristic	-40 °C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Negative Power Supply Current	105	125	145	105	130	150	105	130	150	mA
V_{OH}	Output HIGH Voltage (Note 17)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
V_{OL}	Output LOW Voltage (Note 17)	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	2075		2420	2075		2420	2075		2420	mV
V_{IL}	Input LOW Voltage (Single-Ended)	1355		1675	1355		1675	1355		1675	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 18)	2.0		3.3	2.0		3.3	2.0		3.3	V
I_{IH}	Input HIGH Current (@ V_{IH})			150			150			150	μA
I_{IL}	Input LOW Current (@ V_{IL}) CLK0, $\overline{CLK0}$, CLK1, $\overline{CLK1}$, D, $\overline{D}$, S-IN, $\overline{S\text{-}IN}$	0.5 -150			0.5 -150			0.5 -150			μA

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

16. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.3 V to -2.2 V.
17. All loading with 50 Ω to V_{CC}-2.0 V.
18. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 9. 100EP DC CHARACTERISTICS, PECL V_{CC} = 5.0 V, V_{EE} = 0 V (Note 19)

Symbol	Characteristic	-40 °C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Negative Power Supply Current (Note 20)	105	125	145	105	130	150	105	130	150	mA
V_{OH}	Output HIGH Voltage (Note 21)	3855	3980	4105	3855	3980	4105	3855	3980	4105	mV
V_{OL}	Output LOW Voltage (Note 21)	3055	3180	3305	3055	3180	3305	3055	3180	3305	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	3775		4120	3775		4120	3775		4120	mV
V_{IL}	Input LOW Voltage (Single-Ended)	3055		3375	3055		3375	3055		3375	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 22)	2.0		5.0	2.0		5.0	2.0		5.0	V
I_{IH}	Input HIGH Current (@ V_{IH})			150			150			150	μA
I_{IL}	Input LOW Current (@ V_{IL}) CLK0, $\overline{CLK0}$, CLK1, $\overline{CLK1}$, D, $\overline{D}$, S-IN, $\overline{S\text{-}IN}$	0.5 -150			0.5 -150			0.5 -150			μA

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

19. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +2.0 V to -0.5 V.
20. Required 500 lfpm air flow when using +5 V power supply. For (V_{CC} - V_{EE}) >3.3 V, 5 Ω to 10 Ω in line with V_{EE} required for maximum thermal protection at elevated temperatures. Recommend V_{CC}-V_{EE} operation at $\leq$ 3.3 V.
21. All loading with 50 Ω to V_{CC}-2.0 V.
22. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 10. 100EP DC CHARACTERISTICS, NECL V_{CC} = 0 V, V_{EE} = -5.5 V to -3.0 V (Note 23)

Symbol	Characteristic	-40 °C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Negative Power Supply Current (Note 24)	105	125	145	105	130	150	105	130	150	mA
V_{OH}	Output HIGH Voltage (Note 25)	-1145	-1020	-895	-1145	-1020	-895	-1145	-1020	-895	mV
V_{OL}	Output LOW Voltage (Note 25)	-1945	-1820	-1695	-1945	-1820	-1695	-1945	-1820	-1695	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	-1225		-880	-1225		-880	-1225		-880	mV
V_{IL}	Input LOW Voltage (Single-Ended)	-1945		-1625	-1945		-1625	-1945		-1625	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 26)	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V
I_{IH}	Input HIGH Current (@ V_{IH})			150			150			150	μA
I_{IL}	Input LOW Current (@ V_{IL}) CLK0, CLK1, D, S-IN $\overline{CLK0}$, $\overline{CLK1}$, $\overline{D}$, $\overline{S\text{-}IN}$	 0.5 -150			 0.5 -150			 0.5 -150			μA

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

23. Input and output parameters vary 1:1 with V_{CC}.
24. Required 500 lfpm air flow when using -5 V power supply. For (V_{CC} - V_{EE}) >3.3 V, 5 Ω to 10 Ω in line with V_{EE} required for maximum thermal protection at elevated temperatures. Recommend V_{CC}-V_{EE} operation at $\leq$ 3.3 V.
25. All loading with 50 Ω to V_{CC}-2.0 V.
26. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 11. AC CHARACTERISTICS V_{CC}= 3.0 V to 5.5 V; V_{EE} = 0.0 V or V_{CC} = 0.0 V; V_{EE} = -3.0 V to -5.5 V (Note 27)

Symbol	Characteristic	-40 °C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{SHIFT}	Maximum Shift Frequency				3.0	> 3.4					GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output CLKx MR	 500 500	 625 625	 750 750	 550 550	 675 675	 800 800	 575 575	 700 700	 825 825	ps
t_s	Setup Time D SEL	 50 100	 -50 50		 50 100	 -50 50		 50 100	 -50 50		ps
t_h	Hold Time D SEL	 100 50	 50 -50		 100 50	 50 -50		 100 50	 50 -50		ps
t_{RR}	Reset Recovery Time					800					ps
t_{pw}	Minimum Pulse Width					200					ps
t_{SKEW}	Within-Device Skew (Note 28) Q, $\overline{Q}$ Duty Cycle Skew (Note 29)		50 5.0	100 20		50 5.0	100 20		50 5.0	100 20	ps
t_{JITTER}	Cycle-to-Cycle Jitter (See Figure 3 F_{max}/JITTER)		1	2		1	2		1	2	ps
t_r, t_f	Rise/Fall Times @ 50 MHz (20 - 80%)	110	180	250	125	190	275	150	215	300	ps

27. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50 Ω to V_{CC}-2.0 V.
28. Within-device skew is defined as identical transitions on similar paths through a device.
29. Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.

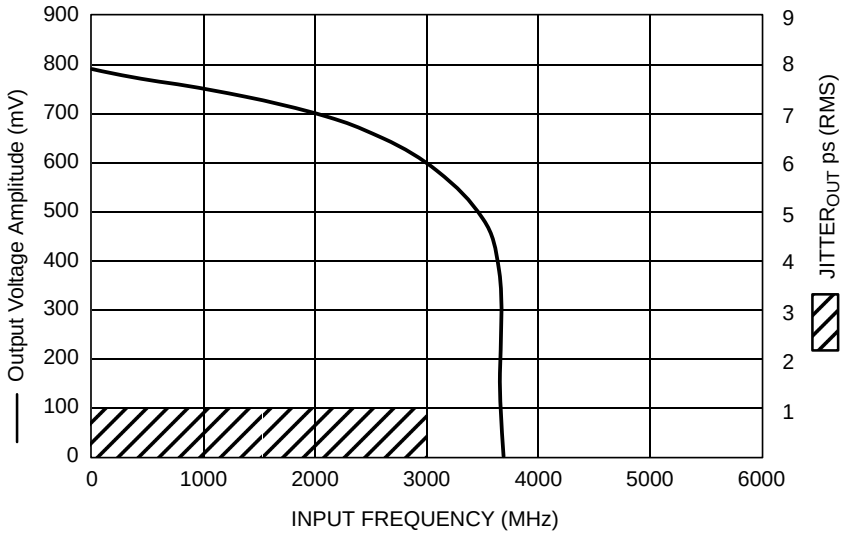


Figure 3. Output Voltage Amplitude / RMS Jitter vs. Input Frequency at Ambient Temperature (Typical)

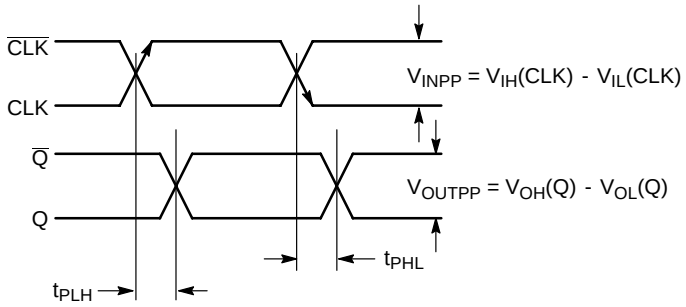


Figure 4. AC Reference Measurement

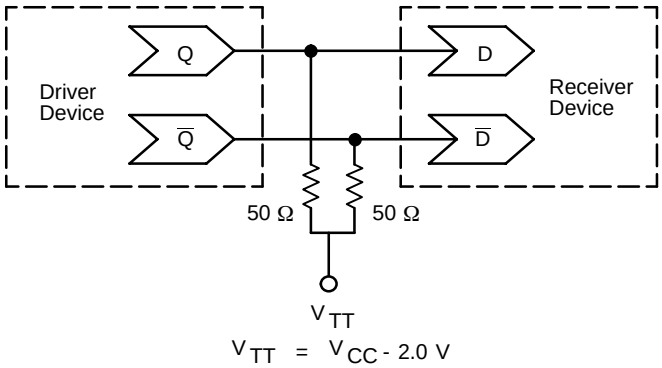


Figure 5. Typical Termination for Output Driver and Device Evaluation (Refer to Application Note AND8020 - Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404 - ECLinPS Circuit Performance at Non-Standard V_{IH} Levels

AN1405 - ECL Clock Distribution Techniques

AN1406 - Designing with PECL (ECL at +5.0 V)

AN1504 - Metastability and the ECLinPS Family

AN1568 - Interfacing Between LVDS and ECL

AN1650 - Using Wire-OR Ties in ECLinPS Designs

AN1672 - The ECL Translator Guide

AND8001 - Odd Number Counters Design

AND8002 - Marking and Date Codes

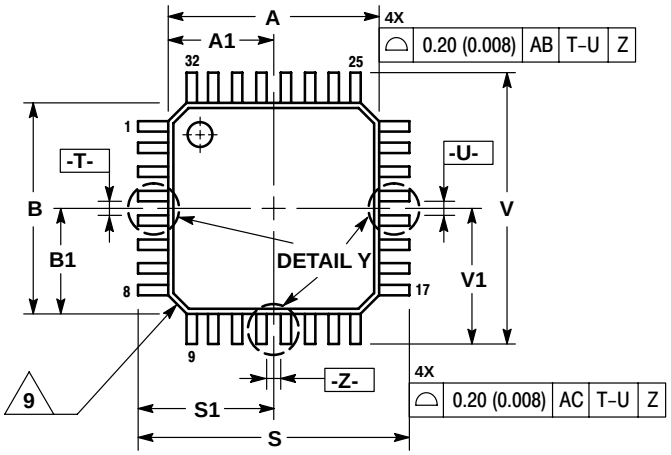
AND8009 - ECLinPS Plus Spice I/O Model Kit

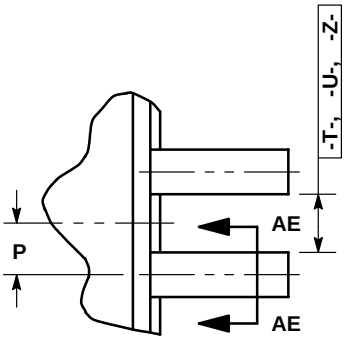
AND8020 - Termination of ECL Logic Devices

For an updated list of Application Notes, please see our website at http://onsemi.com.

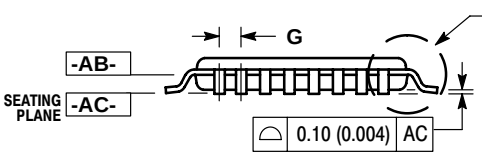
PACKAGE DIMENSIONS

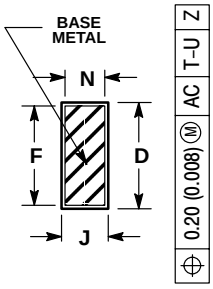
LQFP
FA SUFFIX
32-LEAD PLASTIC PACKAGE
CASE 873A-02
ISSUE A



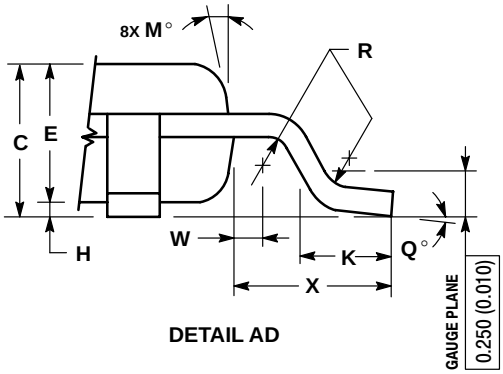


DETAIL Y





SECTION AE-AE



DETAIL AD

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800 BSC		0.031 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.400 BSC		0.016 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

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