# MC100EL14

# 5V ECL 1:5 Clock Distribution Chip

The MC100EL14 is a low skew 1:5 clock distribution chip designed explicitly for low skew clock distribution applications. The $V_{BB}$ pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to $V_{BB}$ as a switching reference voltage. $V_{BB}$ may also rebias AC coupled inputs. When used, decouple $V_{BB}$ and $V_{CC}$ via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, $V_{BB}$ should be left open.

The EL14 features a multiplexed clock input to allow for the distribution of a lower speed scan or test clock along with the high speed system clock. When LOW (or left open and pulled LOW by the input pulldown resistor) the SEL pin will select the differential clock input.

The common enable ($\overline{EN}$) is synchronous so that the outputs will only be enabled/disabled when they are already in the LOW state. This avoids any chance of generating a runt clock pulse when the device is enabled/disabled as can happen with an asynchronous control. The internal flip flop is clocked on the falling edge of the input clock, therefore all associated specification limits are referenced to the negative edge of the clock input.

- 50 ps Output-to-Output Skew
- Synchronous Enable/Disable
- Multiplexed Clock Input
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: $V_{CC}$ = 4.2 V to 5.7 V with $V_{EE}$ = 0 V
- NECL Mode Operating Range: $V_{CC}$ = 0 V with $V_{EE}$ = -4.2 V to -5.7 V
- Q Output will Default LOW with Inputs Open or at $V_{EE}$
- Internal Input Pull-down Resistors on All Inputs, Pull-up Resistors on Inverted Inputs

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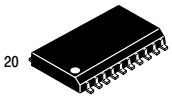
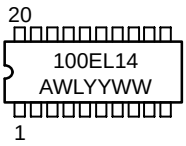



**SO-20L**
**DW SUFFIX**
**CASE 751D**

**MARKING DIAGRAM***




A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*For additional marking information, refer to Application Note AND8002/D.

**ORDERING INFORMATION**†

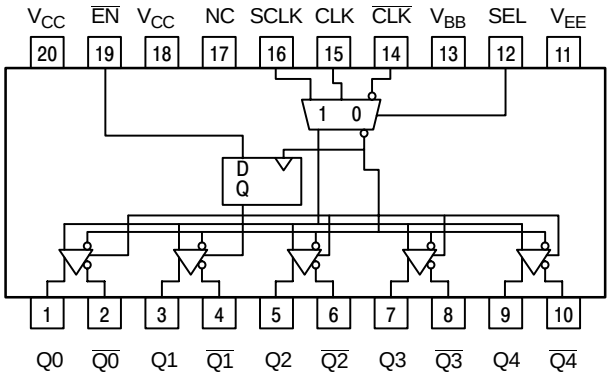
| Device | Package | Shipping |
|---|---|---|
| MC100EL14DW | SO-20L | 38 Units/Rail |
| MC100EL14DWR2 | SO-20L | 1000 /Tape & Reel |

†For additional tape and reel information, refer to Brochure BRD8011/D.

**ATTRIBUTES**

| Characteristics | | Value |
|---|---|---|
| Internal Input Pulldown Resistor | | 75 KΩ |
| Internal Input Pullup Resistor | | 75 KΩ |
| ESD Protection | Human Body Model<br>Machine Model<br>Charge Device Model | > 2 KV<br>> 200 V<br>> 4 KV |
| Moisture Sensitivity (Note 1) | | Level 1 |
| Flammability Rating | Oxygen Index: 28 to 34 | UL 94 V-0 @ 0.125 in |
| Transistor Count | | 303 Devices |
| Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | | |

1. For additional Moisture Sensitivity information, refer to Application Note AND8003/D.




* All $V_{CC}$ pins are tied together on the die.

Warning: All $V_{CC}$ and $V_{EE}$ pins must be externally connected to Power Supply to guarantee proper operation.

**Figure 1. Logic Diagram and Pinout Assignment**

**PIN DESCRIPTION**

| PIN | FUNCTION |
|---|---|
| CLK, $\overline{CLK}$ | ECL Diff Clock Inputs |
| SCLK | ECL Scan Clock Input |
| $\overline{EN}$ | ECL Sync Enable |
| SEL | ECL Clock Select Input |
| $Q_{0-4}$, $\overline{Q_{0-4}}$ | ECL Diff Clock Outputs |
| $V_{BB}$ | Reference Voltage Output |
| $V_{CC}$ | Positive Supply |
| $V_{EE}$ | Negative Supply |
| NC | No Connect |

**FUNCTION TABLE**

| CLK* | SCLK* | SEL* | $\overline{EN}$* | Q |
|---|---|---|---|---|
| L | X | L | L | L |
| H | X | L | L | H |
| X | L | H | L | L |
| X | H | H | L | H |
| X | X | X | H | L (1) |

1. On next negative transition of CLK or SCLK

* Pins will default low when left open.

**MAXIMUM RATINGS** (Note 2)

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Units |
|---|---|---|---|---|---|
| $V_{CC}$ | PECL Mode Power Supply | $V_{EE}$ = 0 V | | 8 | V |
| $V_{EE}$ | NECL Mode Power Supply | $V_{CC}$ = 0 V | | -8 | V |
| $V_I$ | PECL Mode Input Voltage<br>NECL Mode Input Voltage | $V_{EE}$ = 0 V<br>$V_{CC}$ = 0 V | $V_I \le V_{CC}$<br>$V_I \ge V_{EE}$ | 6<br>-6 | V<br>V |
| $I_{out}$ | Output Current | Continuous<br>Surge | | 50<br>100 | mA<br>mA |
| $I_{BB}$ | $V_{BB}$ Sink/Source | | | $\pm$ 0.5 | mA |
| $T_A$ | Operating Temperature Range | | | -40 to +85 | °C |
| $T_{stg}$ | Storage Temperature Range | | | -65 to +150 | °C |
| $\theta_{JA}$ | Thermal Resistance (Junction-to-Ambient) | 0 LFPM<br>500 LFPM | SO-20L<br>SO-20L | 90<br>60 | °C/W<br>°C/W |
| $\theta_{JC}$ | Thermal Resistance (Junction-to-Case) | Standard Board | SO-20L | 30 to 35 | °C/W |
| $T_{sol}$ | Wave Solder | < 2 to 3 sec @ 248°C | | 265 | °C |

2. Maximum Ratings are those values beyond which device damage may occur.

**100EL SERIES PECL DC CHARACTERISTICS** $V_{CC}$ = 5.0 V; $V_{EE}$ = 0.0 V (Note 3)

| | | -40 °C | | | 25°C | | | 85°C | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Characteristic** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** |
| $I_{EE}$ | Power Supply Current | | 32 | 40 | | 32 | 40 | | 34 | 42 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 4) | 3915 | 3995 | 4120 | 3975 | 4045 | 4120 | 3975 | 4050 | 4120 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 4) | 3170 | 3305 | 3445 | 3190 | 3295 | 3380 | 3190 | 3295 | 3380 | mV |
| $V_{IH}$ | Input HIGH Voltage (Single-Ended) | 3835 | | 4120 | 3835 | | 4120 | 3835 | | 4120 | mV |
| $V_{IL}$ | Input LOW Voltage (Single-Ended) | 3190 | | 3525 | 3190 | | 3525 | 3190 | | 3525 | mV |
| $V_{BB}$ | Output Voltage Reference | 3.62 | | 3.74 | 3.62 | | 3.74 | 3.62 | | 3.74 | V |
| $V_{IHCMR}$ | Common Mode Range (Differential)<br>(Note 5) $V_{PP}$ < 500 mV<br>$V_{PP} \geq$ 500 mV | <br>1.3<br>1.5 | | <br>4.6<br>4.6 | <br>1.2<br>1.4 | | <br>4.6<br>4.6 | <br>1.2<br>1.4 | | <br>4.6<br>4.6 | V |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| $I_{IL}$ | Input LOW Current | 0.5 | | | 0.5 | | | 0.5 | | | μA |

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

3. Input and output parameters vary 1:1 with $V_{CC}$. $V_{EE}$ can vary +0.8 V / -0.5 V.
4. Outputs are terminated through a 50 Ω resistor to $V_{CC}$ - 2.0 V.
5. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$, $V_{IHCMR}$ max varies 1:1 with $V_{CC}$. The $V_{IHCMR}$ range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak- to- peak voltage lies between $V_{PP}$(min) and 1 V.

**100EL SERIES NECL DC CHARACTERISTICS** $V_{CC}$ = 0.0 V; $V_{EE}$ = -5.0 V (Note 6)

| | | -40 °C | | | 25°C | | | 85°C | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Characteristic** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** |
| $I_{EE}$ | Power Supply Current | | 32 | 40 | | 32 | 40 | | 34 | 42 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 7) | - 1085 | - 1005 | - 880 | - 1025 | - 955 | - 880 | - 1025 | - 955 | - 880 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 7) | - 1830 | - 1695 | - 1555 | - 1810 | - 1705 | - 1620 | - 1810 | - 1705 | - 1620 | mV |
| $V_{IH}$ | Input HIGH Voltage (Single-Ended) | - 1165 | | - 880 | - 1165 | | - 880 | - 1165 | | - 880 | mV |
| $V_{IL}$ | Input LOW Voltage (Single-Ended) | - 1810 | | - 1475 | - 1810 | | - 1475 | - 1810 | | - 1475 | mV |
| $V_{BB}$ | Output Voltage Reference | - 1.38 | | - 1.26 | - 1.38 | | - 1.26 | - 1.38 | | - 1.26 | V |
| $V_{IHCMR}$ | Common Mode Range (Differential)<br>(Note 8) $V_{PP}$ < 500 mV<br>$V_{PP} \geq$ 500 mV | <br>- 3.7<br>- 3.5 | | <br>- 0.4<br>- 0.4 | <br>- 3.8<br>- 3.6 | | <br>- 0.4<br>- 0.4 | <br>- 3.8<br>- 3.6 | | <br>- 0.4<br>- 0.4 | V |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| $I_{IL}$ | Input LOW Current | 0.5 | | | 0.5 | | | 0.5 | | | μA |

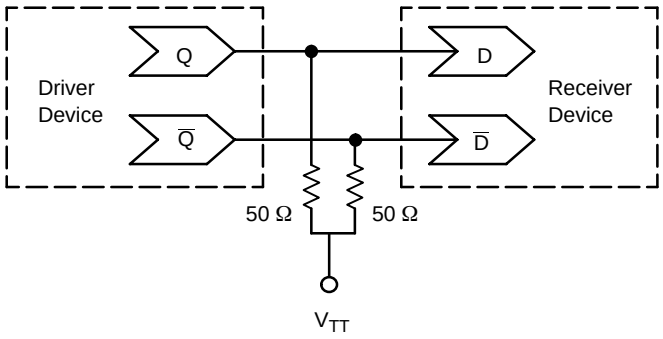
NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

6. Input and output parameters vary 1:1 with $V_{CC}$. $V_{EE}$ can vary +0.8 V / -0.5 V.
7. Outputs are terminated through a 50 Ω resistor to $V_{CC}$ - 2.0 V.
8. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$, $V_{IHCMR}$ max varies 1:1 with $V_{CC}$. The $V_{IHCMR}$ range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak- to- peak voltage lies between $V_{PP}$(min) and 1 V.

**AC CHARACTERISTICS** $V_{CC}$ = 5.0 V; $V_{EE}$ = 0.0 V or $V_{CC}$ = 0.0 V; $V_{EE}$ = -5.0 V (Note 9)

| Symbol | Characteristic | -40 °C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $f_{max}$ | Maximum Toggle Frequency | | TBD | | | TBD | | | TBD | | GHz |
| $t_{PLH}$<br>$t_{PHL}$ | Prop CLK to Q (Diff)<br>Delay CLK to Q (SE)<br>SCLK to Q | 520<br>470<br>470 | | 720<br>770<br>770 | 580<br>530<br>530 | 680<br>680<br>680 | 780<br>830<br>830 | 630<br>580<br>580 | | 830<br>880<br>880 | ps |
| $t_{SKEW}$ | Part-to-Part Skew<br>Within-Device Skew (Note 10) | | | 200<br>50 | | | 200<br>50 | | | 200<br>50 | ps |
| $t_{JITTER}$ | Cycle-to-Cycle Jitter | | TBD | | | TBD | | | TBD | | ps |
| $t_S$ | Setup Time $\overline{EN}$ | 0 | | | 0 | | | 0 | | | ps |
| $t_H$ | Hold Time $\overline{EN}$ | 0 | | | 0 | | | 0 | | | ps |
| $V_{PP}$ | Input Swing (Note 11) | 150 | | 1000 | 150 | | 1000 | 150 | | 1000 | mV |
| $t_r$<br>$t_f$ | Output Rise/Fall Times Q<br>(20% - 80%) | 230 | | 500 | 230 | | 500 | 230 | | 500 | ps |

9. $V_{EE}$ can vary +0.8 V / -0.5 V.
10. Skews are specified for identical LOW-to-HIGH or HIGH-to-LOW transitions.
11. $V_{PP}$(min) is the minimum input swing for which AC parameters guaranteed. The device has a DC gain of ≈40.




$V_{TT} = V_{CC}$ - 2.0 V

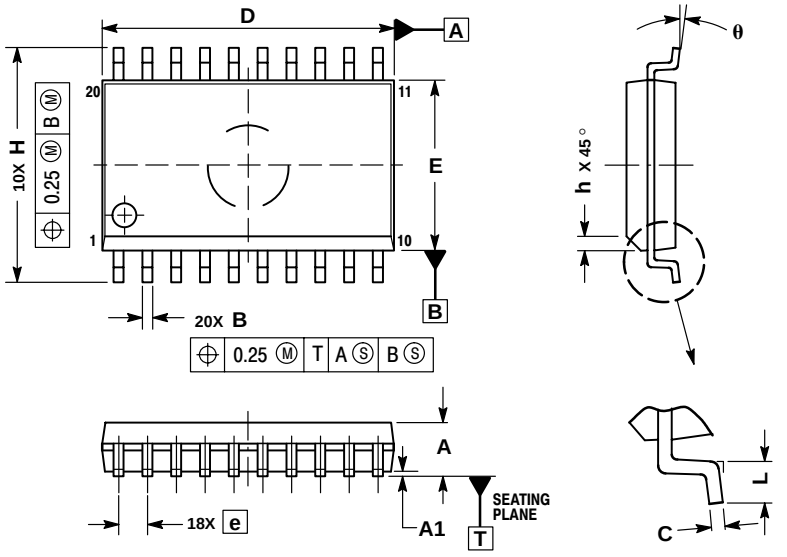
**Typical Termination for Output Driver and Device Evaluation**
**(See Application Note AND8020 - Termination of ECL Logic Devices.)**

### Resource Reference of Application Notes

| | | |
|---|---|---|
| **AN1404** | - | ECLinPS Circuit Performance at Non-Standard $V_{IH}$ Levels |
| **AN1405** | - | ECL Clock Distribution Techniques |
| **AN1406** | - | Designing with PECL (ECL at +5.0 V) |
| **AN1503** | - | ECLinPS I/O SPICE Modeling Kit |
| **AN1504** | - | Metastability and the ECLinPS Family |
| **AN1560** | - | Low Voltage ECLinPS SPICE Modeling Kit |
| **AN1568** | - | Interfacing Between LVDS and ECL |
| **AN1596** | - | ECLinPS Lite Translator ELT Family SPICE I/O Model Kit |
| **AN1650** | - | Using Wire-OR Ties in ECLinPS Designs |
| **AN1672** | - | The ECL Translator Guide |
| **AND8001** | - | Odd Number Counters Design |
| **AND8002** | - | Marking and Date Codes |
| **AND8020** | - | Termination of ECL Logic Devices |
| **AND8090** | - | AC Characteristics of ECL Devices |

## PACKAGE DIMENSIONS

**SO-20L**
**DW SUFFIX**
PLASTIC SOIC PACKAGE
CASE 751D-05
ISSUE F




NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| B | 0.35 | 0.49 |
| C | 0.23 | 0.32 |
| D | 12.65 | 12.95 |
| E | 7.40 | 7.60 |
| e | 1.27 BSC | |
| H | 10.05 | 10.55 |
| h | 0.25 | 0.75 |
| L | 0.50 | 0.90 |
| θ | 0° | 7° |

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