

NDC631N

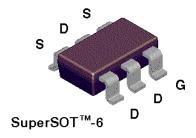
N-Channel Logic Level Enhancement Mode Field Effect Transistor

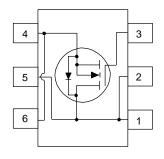
General Description

These N-Channel logic level enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications in notebook computers, portable phones, PCMICA cards, and other battery powered circuits where fast switching, and low in-line power loss are needed in a very small outline surface mount package.

Features

- 4.1 A, 20 V. $R_{DS(ON)} = 0.06~\Omega$ @ $V_{GS} = 4.5~V$ $R_{DS(ON)} = 0.075~\Omega$ @ $V_{GS} = 2.7~V$.
- Proprietary SuperSOTTM-6 package design using copper lead frame for superior thermal and electrical capabilities.
- High density cell design for extremely low R_{DS(ON)}.
- Exceptional on-resistance and maximum DC current capability.





Absolute Maximum Ratings T_a = 25°C unless otherwise note

Symbol	Parameter		NDC631N				
V _{DSS}	Drain-Source Voltage		20	V			
V_{GSS}	Gate-Source Voltage - Continuous		8	V			
I _D	Drain Current - Continuous	(Note 1a)	4.1	A			
	- Pulsed		15				
P_{D}	Maximum Power Dissipation	(Note 1a)	1.6	W			
		(Note 1b)	1				
		(Note 1c)	0.8				
T_J, T_{STG}	Operating and Storage Temperatur	e Range	-55 to 150	°C			
THERMA	AL CHARACTERISTICS	·					
R _{øJA}	Thermal Resistance, Junction-to-A	mbient (Note 1a)	78	°C/W			
R _{eJC}	Thermal Resistance, Junction-to-C	ase (Note 1)	30	°C/W			

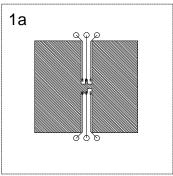
Symbol	Parameter	Conditions		Min	Тур	Max	Units
OFF CHA	ARACTERISTICS	<u> </u>		•		•	
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_{D} = 250 \mu\text{A}$		20			V
DSS	Zero Gate Voltage Drain Current	$V_{DS} = 16 \text{ V}, \ V_{GS} = 0 \text{ V}$				1	μA
			$T_J = 55^{\circ}C$			10	μA
GSSF	Gate - Body Leakage, Forward	$V_{GS} = 8 \text{ V}, V_{DS} = 0 \text{ V}$				100	nA
GSSR	Gate - Body Leakage, Reverse	$V_{GS} = -8 \text{ V}, V_{DS} = 0 \text{ V}$				-100	nA
	RACTERISTICS (Note 2)	<u> </u>		•		•	
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$		0.4	0.7	1	V
			$T_{J} = 125^{\circ}C$	0.3	0.5	0.8	
R _{DS(ON)}	Static Drain-Source On-Resistance	$V_{GS} = 4.5 \text{ V}, I_D = 4.1 \text{ A}$	•		0.039	0.06	Ω
			$T_{J} = 125^{\circ}C$		0.06	0.11	
		$V_{GS} = 2.7 \text{ V}, I_D = 3.6 \text{ A}$	•		0.05	0.075	1
D(on)	On-State Drain Current	$V_{GS} = 4.5 \text{ V}, V_{DS} = 5 \text{ V}$		15			Α
) _{FS}	Forward Transconductance	$V_{DS} = 4.5 \text{ V}, I_{D} = 4.1 \text{ A}$			12		S
OYNAMIC	CHARACTERISTICS	·					_
Ciss	Input Capacitance	$V_{DS} = 10 \text{ V}, \ V_{GS} = 0 \text{ V},$	$V_{DS} = 10 \text{ V}, \ V_{GS} = 0 \text{ V},$				
Coss	Output Capacitance	f = 1.0 MHz			230		pF
C_{rss}	Reverse Transfer Capacitance				95		pF
SWITCHI	NG CHARACTERISTICS (Note 2)						
D(on)	Turn - On Delay Time	$V_{DD} = 5 \text{ V}, I_{D} = 1 \text{ A},$			9	17	ns
r	Turn - On Rise Time	$V_{GEN} = 4.5 \text{ V}, R_{GEN} = 6 \Omega$			25	45	ns
D(off)	Turn - Off Delay Time			28	50	ns	
f	Turn - Off Fall Time				8	15	ns
Q _g	Total Gate Charge	$V_{DS} = 10 \text{ V},$ $I_{D} = 4.1 \text{ A}, V_{GS} = 4.5 \text{ V}$			10	14	nC
Q_{gs}	Gate-Source Charge	$I_D = 4.1 \text{ A}, \ V_{GS} = 4.5 \text{ V}$			1		nC
Q_{gd}	Gate-Drain Charge			3.3		nC	

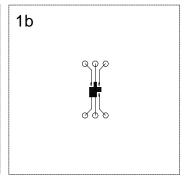
ELECTRICAL CHARACTERISTICS (T _A = 25°C unless otherwise noted)								
Symbol	Parameter Conditions Min Typ Max U							
DRAIN-SOURCE DIODE CHARACTERISTICS								
Is	Continuous Source Diode Current			1.3	Α			
V _{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = 1.3 \text{ A (Note 2)}$		0.75	1.2	V		

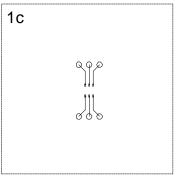
1. R_{BA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{BA} is guaranteed by design while $\boldsymbol{R}_{\theta\text{CA}}$ is determined by the user's board design.

$$\begin{split} P_{D}(t) &= \tfrac{T_{J^{-}T_{A}}}{R_{\theta J}} = \tfrac{T_{J^{-}T_{A}}}{R_{\theta J} d_{\theta} R_{\theta C}(t)} = I_{D}^{2}(t) \times R_{DS(ON)} \mathbf{g}_{T_{J}} \end{split}$$
 Typical $R_{\theta M}$ using the board layouts shown below on 4.5°x5° FR-4 PCB in a still air environment:

- a. 78°C/W when mounted on a 1 in 2 pad of 2oz copper.
- b. 125°C/W when mounted on a 0.01 in $^{\!2}$ pad of 2oz copper.
- c. 156°C/W when mounted on a 0.003 in $^{\!2}\,\text{pad}$ of 2oz copper.







Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2.0%.

Typical Electrical Characteristics

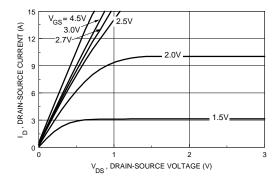


Figure 1. On-Region Characteristics.

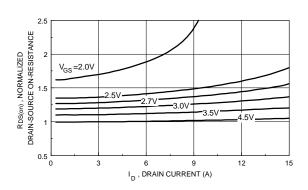


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

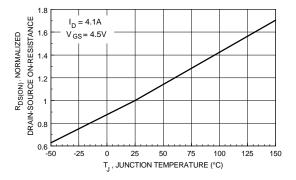


Figure 3. On-Resistance Variation with Temperature.

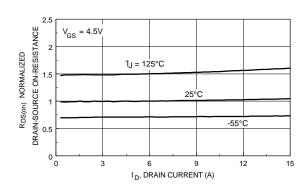


Figure 4. On-Resistance Variation with Drain Current and Temperature.

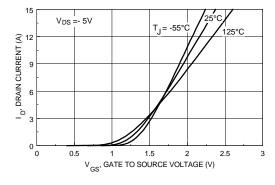


Figure 5. Transfer Characteristics.

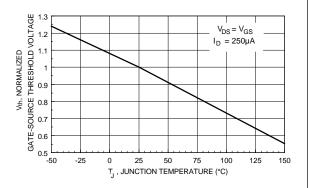


Figure 6. Gate Threshold Variation with Temperature.

Typical Electrical Characteristics (continued)

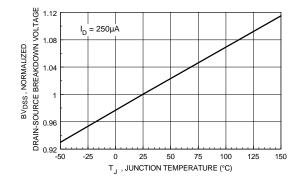


Figure 7. Breakdown Voltage Variation with Temperature.

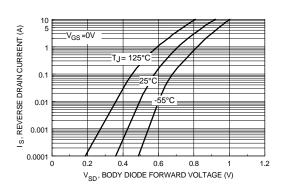


Figure 8. Body Diode Forward Voltage Variation with Source Current and Temperature.

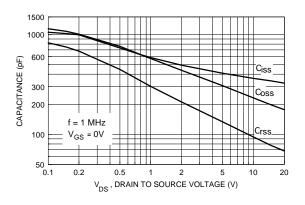


Figure 9. Capacitance Characteristics.

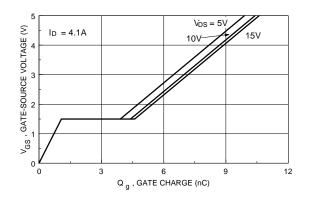


Figure 10. Gate Charge Characteristics.

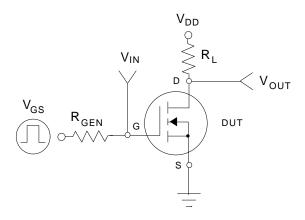


Figure 11. Switching Test Circuit.

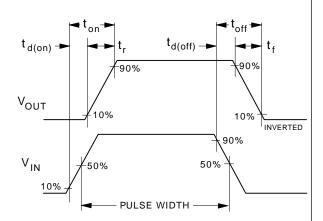


Figure 12. Switching Waveforms.

Typical Electrical and Thermal Characteristics (continued)

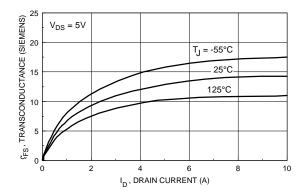
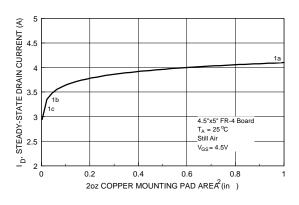


Figure 13. Transconductance Variation with Drain Current and Temperature.

Figure 14. SuperSOT[™]-6 Maximum Steady-State
Power Dissipation versus Copper Mounting Pad
Area.



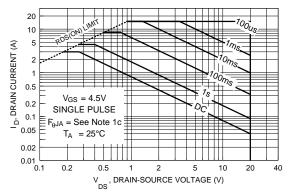


Figure 15. Maximum Steady-State Drain Current versus Copper Mounting Pad Area.

Figure 16. Maximum Safe Operating Area.

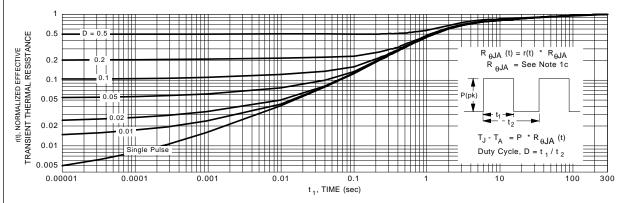
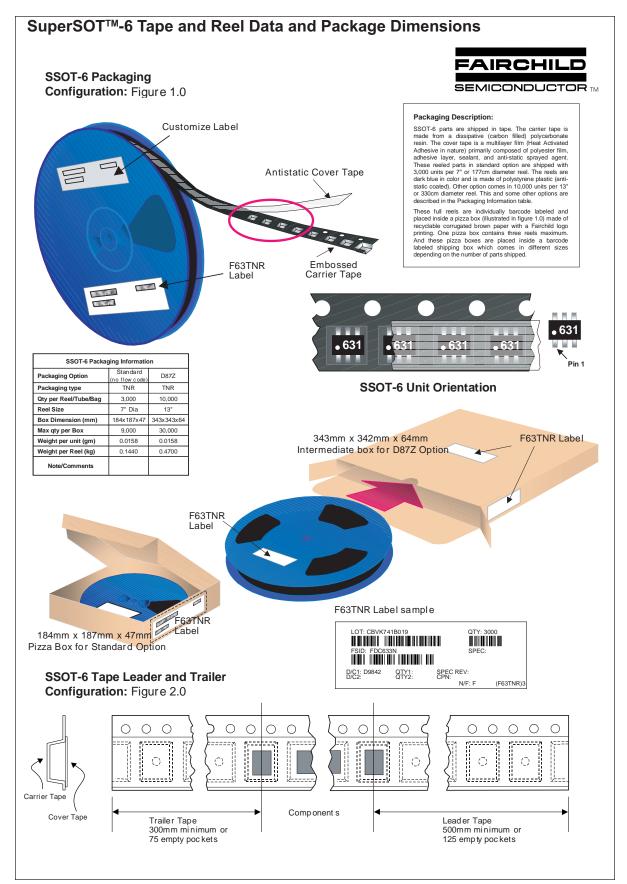
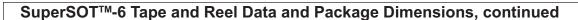


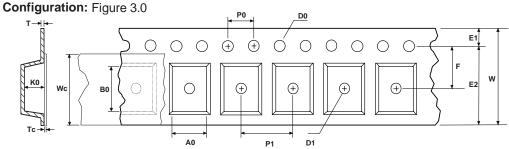
Figure 17. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.





SSOT-6 Embossed Carrier Tape



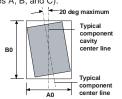


	Dimensions are in millimeter													
Pkg type	Α0	В0	w	D0	D1	E1	E2	F	P1	P0	K0	т	Wc	Тс
SSOT-6 (8mm)	3.23 +/-0.10	3.18 +/-0.10	8.0 +/-0.3	1.55 +/-0.05	1.125 +/-0.125	1.75 +/-0.10	6.25 min	3.50 +/-0.05	4.0 +/-0.1	4.0 +/-0.1	1.37 +/-0.10	0.255 +/-0.150	5.2 +/-0.3	0.06 +/-0.02

Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



Sketch A (Side or Front Sectional View)
Component Rotation

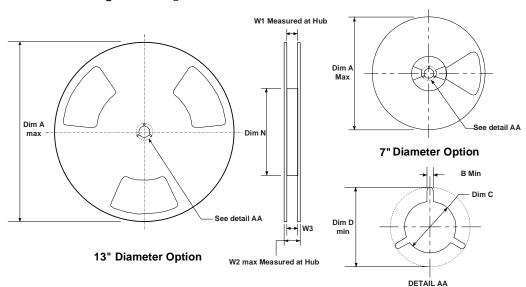


Sketch B (Top View)
Component Rotation



Sketch C (Top View)
Component lateral movement

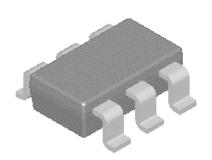
SSOT-6 Reel Configuration: Figure 4.0

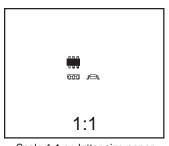


Dimensions are in inches and millimeters									
Tape Size	Reel Option	Dim A	Dim B	Dim C	Dim D	Dim N	Dim W1	Dim W2	Dim W3 (LSL-USL)
8mm	7" Dia	7.00 177.8	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	2.165 55	0.331 +0.059/-0.000 8.4 +1.5/0	0.567 14.4	0.311 - 0.429 7.9 - 10.9
8mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	4.00 100	0.331 +0.059/-0.000 8.4 +1.5/0	0.567 14.4	0.311 - 0.429 7.9 - 10.9

SuperSOT™-6 Tape and Reel Data and Package Dimensions, continued

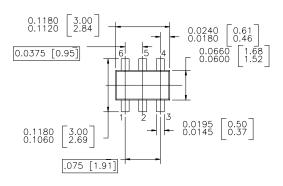
SuperSOT -6 (FS PKG Code 31, 33)

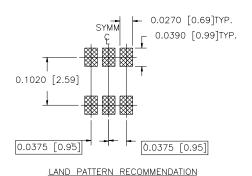




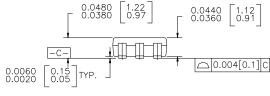
Scale 1:1 on letter size paper
Dimensions shown below are in:
inches [millimeters]

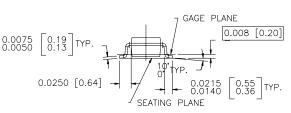
Part Weight per unit (gram): 0.0158





CONTROLLING DIMENSION IS INCH VALUES IN [] ARE MILLIMETERS





NOTES: UNLESS OTHERWISE SPECIFIED

1.0 STANDARD LEAD FINISH: 150 MICROINCHES 93.81 MICROMETERS) MINIMUM TIN / LEAD (SOLDER) ON COPPER.

 $2.0\ \mathsf{NO}\ \mathsf{JEDEC}\ \mathsf{REGISTRATION}\ \mathsf{AS}\ \mathsf{OF}\ \mathsf{JULY}\ 1996$

SUPER SOT 6 LEADS

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