Q-FLASH™ MEMORY

MT28F128J3, MT28F640J3, MT28F320J3

Features

- x8/x16 organization
- One hundred twenty-eight 128KB erase blocks (128Mb)
  Sixty-four 128KB erase blocks (64Mb)
  Thirty-two 128KB erase blocks (32Mb)
- VCC, VCCQ, and VPEN voltages:
  2.7V to 3.6V VCC operation
  2.7V to 3.6V, or 5V VPEN application programming
- Interface Asynchronous Page Mode Reads:
  150ns/25ns or 120ns/25ns read access time (128Mb)
  120ns/25ns or 115ns/25ns read access time (64Mb)
  110ns/25ns read access time (32Mb)
- Manufacturing ID (ManID)
  Intel® (0x89h)
  Micron® (0x2Ch)
- Industry-standard pinout
- Inputs and outputs are fully TTL-compatible
- Common Flash Interface (CFI) and Scalable Command Set
- Automatic write and erase algorithm
- 5.6µs-per-byte effective programming time using write buffer
- 128-bit protection register
  64-bit unique device identifier
  64-bit user-programmable OTP cells
- Enhanced data protection feature with VPEN = VSS
  Flexible sector locking
  Sector erase/program lockout during power transition
- Security OTP block feature
  Permanent block locking
  (Contact factory for availability)
- 100,000 ERASE cycles per block
- Automatic suspend options:
  Block Erase Suspend-to-Read
  Block Erase Suspend-to-Program
  Program Suspend-to-Read

Figure 1: 56-Pin TSOP Type I

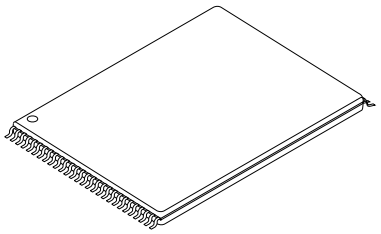
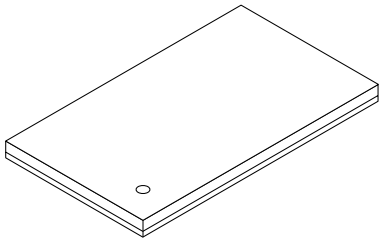


Figure 2: 64-Ball FBGA



Options	Marking
• Timing	
110ns (32Mb)	-11
115ns (64Mb)	-115
120ns (64Mb)	-12
120ns (128Mb)	-12
150ns (128Mb)	-15
• Operating Temperature Range	
Commercial Temperature (0°C to +85°C)	None
Extended Temperature (-40°C to +85°C)	ET
• Packages	
56-pin TSOP Type I	RG
64-ball FBGA (1.00mm pitch)	FS
• Manufacturing ID (ManID)	
Intel (0x89h)	None
Micron (0x2Ch)	M

Part Number Example:
MT28F640J3RG-12ET

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General Description

The MT28F128J3 is a nonvolatile, electrically block-erasable (Flash), programmable memory containing 134,217,728 bits organized as 16,777,218 bytes (8 bits) or 8,388,608 words (16 bits). This 128Mb device is organized as one hundred twenty-eight 128KB erase blocks.

The MT28F640J3 contains 67,108,864 bits organized as 8,388,608 bytes (8 bits) or 4,194,304 words (16 bits). This 64Mb device is organized as sixty-four 128KB erase blocks.

Similarly, the MT28F320J3 contains 33,554,432 bits organized as 4,194,304 bytes (8 bits) or 2,097,152 words (16 bits). This 32Mb device is organized as thirty-two 128KB erase blocks.

These three devices feature in-system block locking. They also have common Flash interface (CFI) that permits software algorithms to be used for entire families of devices. The software is device-independent, JEDEC ID-independent with forward and backward compatibility.

Additionally, the scalable command set (SCS) allows a single, simple software driver in all host systems to work with all SCS-compliant Flash memory devices. The SCS provides the fastest system/device data transfer rates and minimizes the device and system-level implementation costs.

To optimize the processor-memory interface, the device accommodates V_{PEN}, which is switchable during block erase, program, or lock bit configuration, or hard-wired to V_{CC}, depending on the application. V_{PEN} is treated as an input pin to enable erasing, programming, and block locking. When V_{PEN} is lower than the V_{CC} lockout voltage (V_{LKO}), all program functions are disabled. Block erase suspend mode enables the user to stop block erase to read data from or program data to any other blocks. Similarly, program suspend mode enables the user to suspend programming to read data or execute code from any unsuspended blocks.

V_{PEN} serves as an input with 2.7V, 3.3V, or 5V for application programming. V_{PEN} in this Q-Flash™ family can provide data protection when connected to ground. This pin also enables program or erase lockout during power transition.

Micron's even-sectored Q-Flash devices offer individual block locking that can lock and unlock a block using the sector lock bits command sequence.

Status (STS) is a logic signal output that gives an additional indicator of the internal state machine (ISM) activity by providing a hardware signal of both status and status masking. This status indicator minimizes central processing unit (CPU) overhead and system power consumption. In the default mode, STS acts as an RY/BY# pin. When LOW, STS indicates that the ISM is performing a block erase, program, or lock bit configuration. When HIGH, STS indicates that the ISM is ready for a new command.

Three chip enable (CE) pins are used for enabling and disabling the device by activating the device's control logic, input buffer, decoders, and sense amplifiers.

BYTE# enables the device to be used in x8 or x16 read/write mode; BYTE# = 0 selects an 8-bit mode, with address A0 selecting between the LOW and HIGH byte, while BYTE# = 1 selects a 16-bit mode. When BYTE# = 1, A1 becomes the lowest-order address line with A0 being a no connect.

RP# is used to reset the device. When the device is disabled and RP# is at Vcc, the standby mode is enabled. A reset time (^{t}RWH) is required after RP# switches HIGH until outputs are valid. Likewise, the device has a wake time (^{t}RS) from RP# high until writes to the command user interface (CUI) are recognized. When RP# is at GND, it provides write protection, resets the ISM, and clears the status register.

A variant of the MT28F320J3 also supports the new security block lock feature for additional code security. This feature provides an OTP function for the device. (Contact factory for availability.)

The MT28F320J3 and the MT28F640J3 are manufactured using the 0.18µm process technology, and the MT28F128J3 is manufactured using the 0.15µm process technology.

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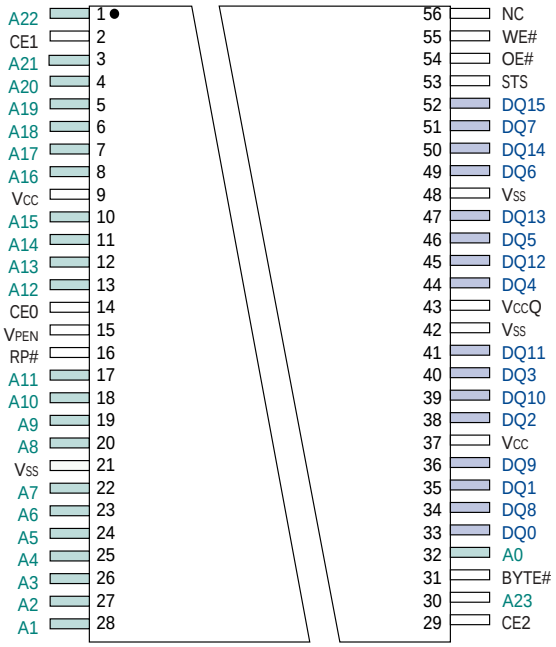
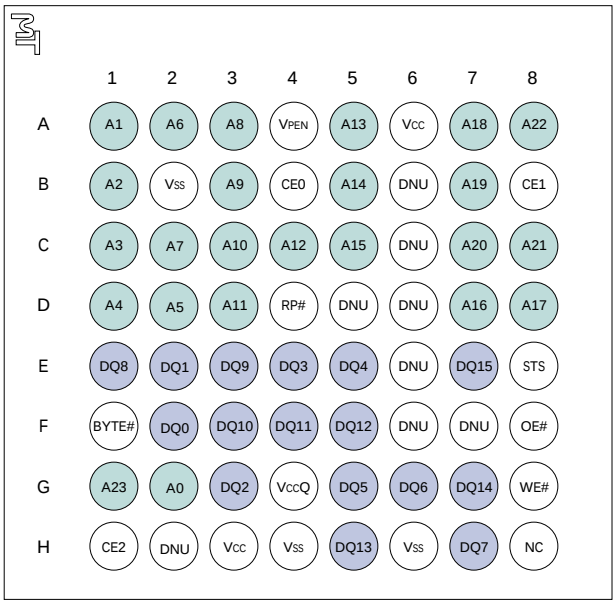
Figure 3: Pin and Ball Assignment Diagrams

56-Pin TSOP Type I



64-Ball FBGA



Top View
(Ball Down)

NOTE:

1. A22 only exists on the 64Mb and 128Mb devices. On the 32Mb, this pin/ball is a no connect (NC).
2. A23 only exists on the 128Mb device. On the 32Mb and 64Mb, this pin/ball is a no connect (NC).
3. The # symbol indicates signal is active LOW.

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Part Numbering Information

Micron's Flash devices are available with several different combinations of features (see Figure 4).

Valid combinations of features and their corresponding part numbers are listed in Table 1.

Figure 4: Part Number Chart

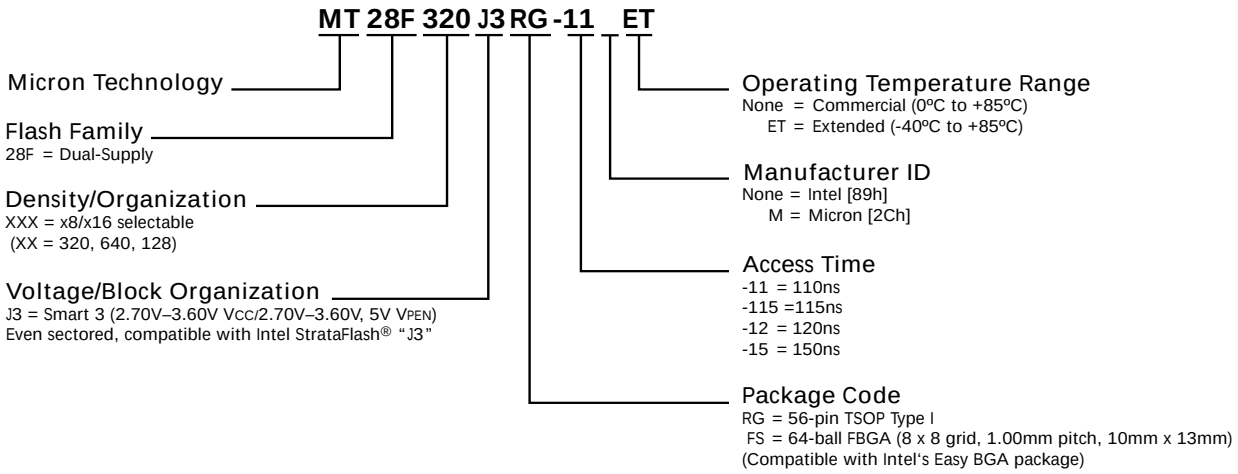

Table 1: Valid Part Number Combinations

PART NUMBER		
32Mb	**64Mb**	**128Mb**
MT28F320J3FS-11	MT28F640J3FS-12	MT28F128J3FS-15
MT28F320J3FS-11 M	MT28F640J3FS-12 M	MT28F128J3FS-15 M
MT28F320J3FS-11 ET	MT28F640J3FS-12 ET	MT28F128J3FS-15 ET
MT28F320J3FS-11 MET	MT28F640J3FS-12 MET	MT28F128J3FS-15 MET
MT28F320J3RG-11	MT28F640J3RG-12	MT28F128J3RG-15
MT28F320J3RG-11 M	MT28F640J3RG-12 M	MT28F128J3RG-15 M
MT28F320J3RG-11 ET	MT28F640J3RG-12 ET	MT28F128J3RG-15 ET
MT28F320J3RG-11 MET	MT28F640J3RG-12 MET	MT28F128J3RG-15 MET
	MT28F640J3FS-115	MT28F128J3FS-12
	MT28F640J3FS-115 M	MT28F128J3FS-12 M
	MT28F640J3FS-115 ET	MT28F128J3FS-12 ET
	MT28F640J3FS-115 MET	MT28F128J3FS-12 MET
	MT28F640J3RG-115	MT28F128J3RG-12
	MT28F640J3RG-115 M	MT28F128J3RG-12 M
	MT28F640J3RG-115 ET	MT28F128J3RG-12 ET
	MT28F640J3RG-115 MET	MT28F128J3RG-12 MET

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FBGA Device Marking

Due to the size of the package, Micron's standard part number is not printed on the top of each device. Instead, an abbreviated device mark comprised of a five-digit alphanumeric code is used. The abbreviated device marks are cross-referenced to Micron part numbers in Table 2.

Table 2: Cross-Reference for Abbreviated Device Marks

PART NUMBER	PRODUCT MARKING	ENGINEERING SAMPLE	QUALIFIED SAMPLE
MT28F320J3FS-11	FW201	FX201	FQ201
MT28F320J3FS-11 M	FW204	FX204	FQ204
MT28F320J3FS-11 ET	FW207	FX207	FQ207
MT28F320J3FS-11 MET	FW208	FX208	FQ208
MT28F640J3FS-115	FW505	FX505	FQ505
MT28F640J3FS-115 M	FW506	FX506	FQ506
MT28F640J3FS-115 ET	FW406	FX406	FQ406
MT28F640J3FS-115 MET	FW507	FX507	FQ507
MT28F640J3FS-12	FW202	FX202	FQ202
MT28F640J3FS-12 M	FW205	FX205	FQ205
MT28F640J3FS-12 ET	FW209	FX209	FQ209
MT28F640J3FS-12 MET	FW206	FX206	FQ206
MT28F128J3FS-12	FW508	FX508	FQ508
MT28F128J3FS-12 M	FW510	FX510	FQ510
MT28F128J3FS-12 ET	FW407	FX407	FQ407
MT28F128J3FS-12 MET	FW509	FX509	FQ509
MT28F128J3FS-15	FW203	FX203	FQ203
MT28F128J3FS-15 M	FW503	FX503	FQ503
MT28F128J3FS-15 ET	FW501	FX501	FQ501
MT28F128J3FS-15 MET	FW502	FX502	FQ502

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Figure 5: Functional Block Diagram (128Mb)

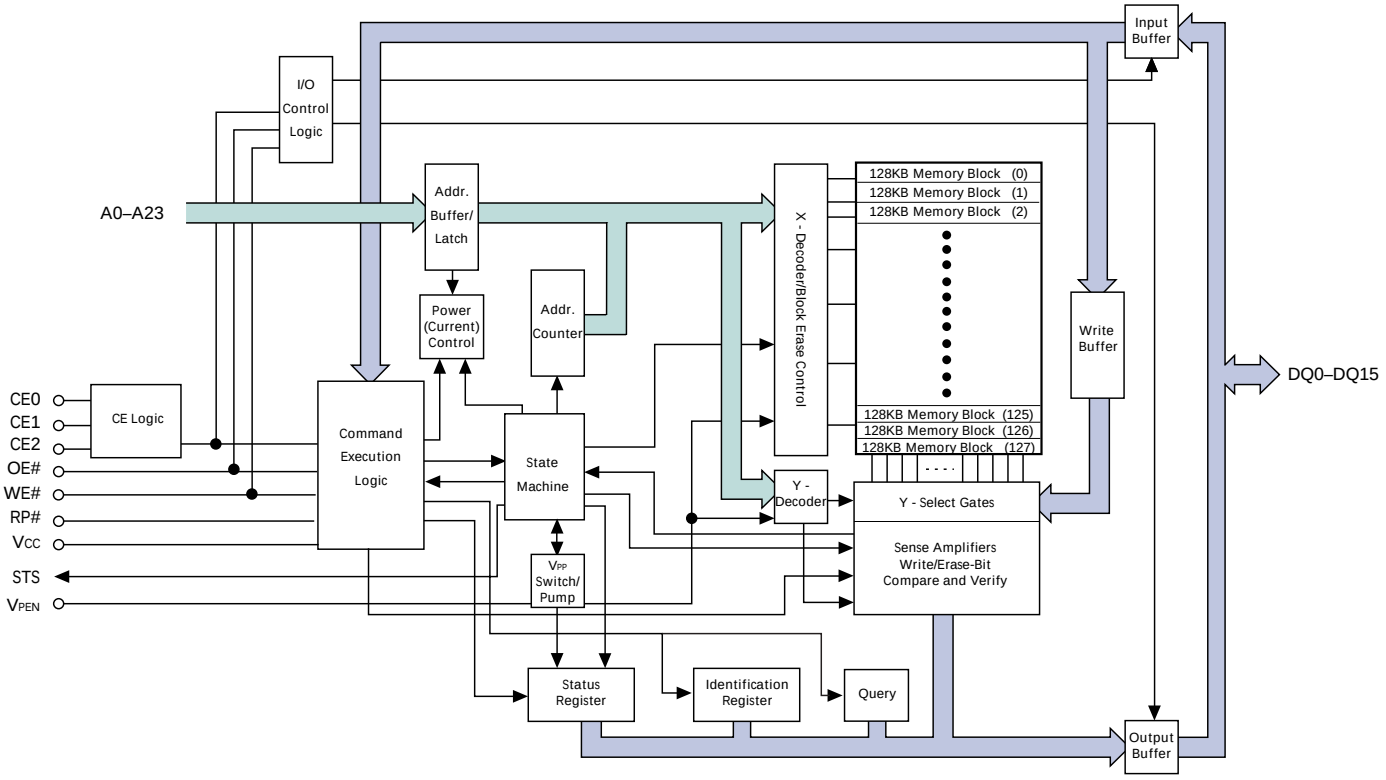

Figure 6: Functional Block Diagram (64Mb)

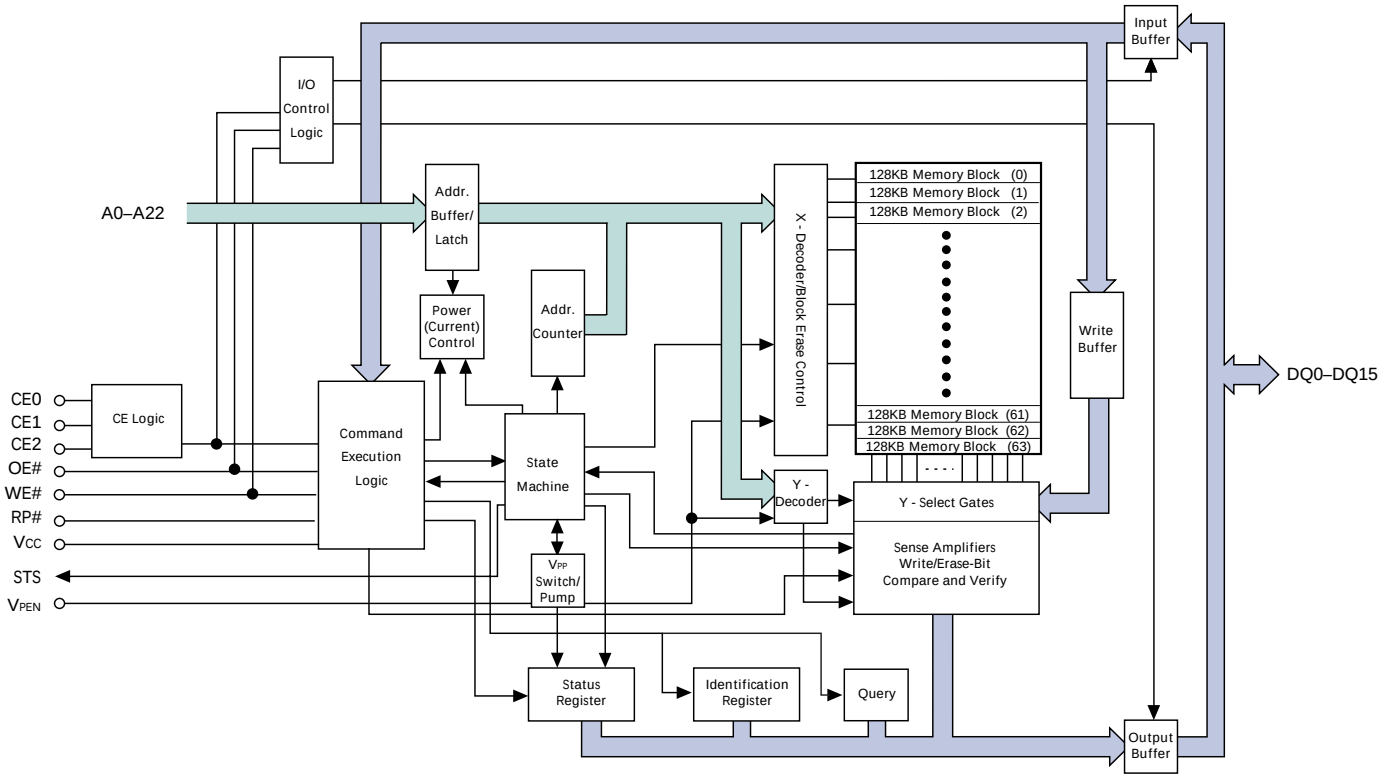

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Figure 7: Functional Block Diagram (32Mb)

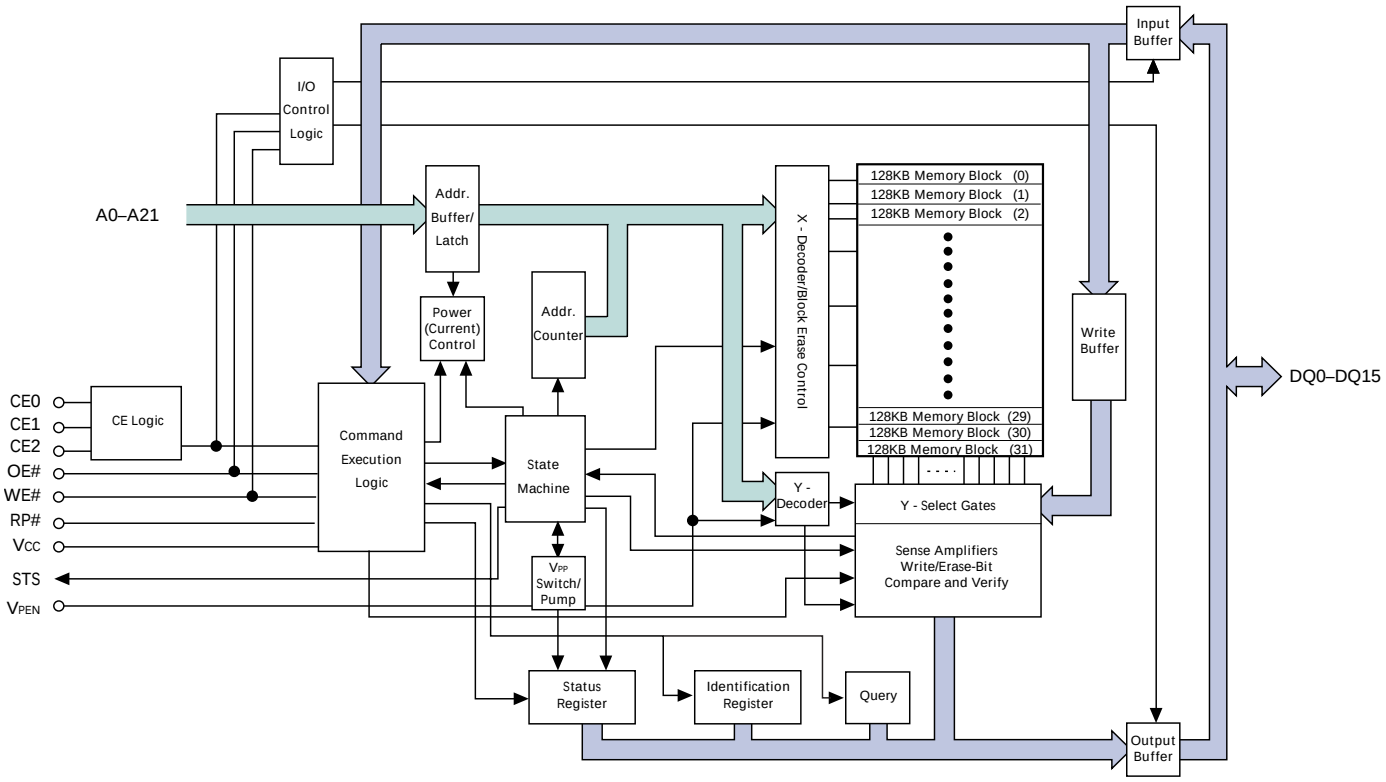

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Table 3: Pin/Ball Descriptions

56-PIN TSOP NUMBERS	64-BALL FBGA NUMBERS	SYMBOL	TYPE	DESCRIPTION
55	G8	WE#	Input	Write Enable: Determines if a given cycle is a WRITE cycle. If WE# is LOW, the cycle is either a WRITE to the command execution logic (CEL) or to the memory array. Addresses and data are latched on the rising edge of the WE# pulse.
14, 2, 29	B4, B8, H1	CE0, CE1, CE2	Input	Chip Enable: Three CE pins enable the use of multiple Flash devices in the system without requiring additional logic. The device can be configured to use a single CE signal by tying CE1 and CE2 to ground and then using CE0 as CE. Device selection occurs with the first edge of CE0, CE1, or CE2 (CEx) that enables the device. Device deselection occurs with the first edge of CEx that disables the device (see Table 4 on page 14).
16	D4	RP#	Input	Reset/Power-Down: When LOW, RP# clears the status register, sets the ISM to the array read mode, and places the device in deep power-down mode. All inputs, including CEx, are "Don't Care," and all outputs are High-Z. RP# must be held at V_{IH} during all other modes of operation.
54	F8	OE#	Input	Output Enables: Enables data ouput buffers when LOW. When OE# is HIGH, the output buffers are disabled.
32, 28, 27, 26, 25, 24, 23, 22, 20, 19, 18, 17, 13, 12, 11, 10, 8, 7, 6, 5, 4, 3, 1, 30	G2, A1, B1, C1, D1, D2, A2, C2, A3, B3, C3, D3, C4, A5, B5, C5, D7, D8, A7, B7, C7, C8, A8, G1	A0–A21/ (A22) (A23)	Input	Address inputs during READ and WRITE operations. A0 is only used in x8 mode and will be a NC in x16 mode (the input buffer is turned off when BYTE = HIGH). A22 (pin 1, ball A8) is only available on the 64Mb and 128Mb devices. A23 (pin 30, ball G1) is only available on the 128Mb device.
31	F1	BYTE#	Input	BYTE# low places the device in the x8 mode. BYTE# high places the device in the x16 mode and turns off the A0 input buffer. Address A1 becomes the lowest order address in x16 mode.
15	A4	V_{PEN}	Input	Necessary voltage for erasing blocks, programming data, or configuring lock bits. Typically, V_{PEN} is connected to V_{CC}. When $V_{PEN} \leq V_{PENLK}$, this pin enables hardware write protect.
33, 35, 38, 40, 44, 46, 49, 51, 34, 36, 39, 41, 45, 49, 51, 34, 36, 39, 41, 45, 47, 50, 52	F2, E2, G3, E4, E5, G5, G6, H7, E1, E3, F3, F4, F5, H5, G7, E7	DQ0–DQ15	Input/ Output	Data I/O: Data output pins during any READ operation or data input pins during a WRITE. DQ8–DQ15 are not used in byte mode (BYTE = LOW).
53	E8	STS	Output	Status: Indicates the status of the ISM. When configured in level mode (default), STS acts as a RY/BY# pin. When configured in its pulse mode, it can pulse to indicate program and/or erase completion. Tie STS to V_{CCQ} through a pull-up resistor.
43	G4	V_{CCQ}	Supply	V_{CCQ} controls the output voltages. To obtain output voltage compatible with system data bus voltages, connect V_{CCQ} to the system supply voltage.
9, 37	H3, A6	V_{CC}	Supply	Power Supply: 2.7V to 3.6V.
21, 42, 48	B2, H4, H6	V_{SS}	Supply	Ground.
56	H8	NC	—	No Connect: These may be driven or left unconnected. Pin 1 and ball A8 are NCs on the 32Mb device. Pin 30 and ball G1 are NCs on the 32Mb and 64Mb devices.

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Table 3: Pin/Ball Descriptions (continued)

56-PIN TSOP NUMBERS	64-BALL FBGA NUMBERS	SYMBOL	TYPE	DESCRIPTION
—	B6, C6, D5, D6, E6, F6, F7, H2	DNU	—	Do Not Use: Must float to minimize noise.

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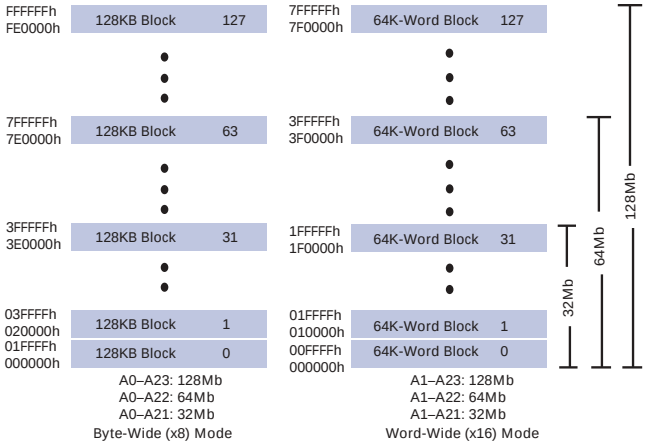
Memory Architecture

The MT28F128J3, MT28F640J3, and MT28F320J3 memory array architecture is divided into one hundred twenty-eight, sixty-four, or thirty-two 128KB blocks, respectively (see Figure 8). The internal architecture allows greater flexibility when updating data because individual code portions can be updated independently of the rest of the code.

Figure 8: Memory Map



Read

Information can be read from any block, query, identifier codes, or status register, regardless of the V_{PEN} voltage. The device automatically resets to read array mode upon initial device power-up or after exit from reset/power-down mode. To access other read mode commands (READ ARRAY, READ QUERY, READ IDENTIFIER CODES, or READ STATUS REGISTER), these commands should be issued to the CUI. Six control pins dictate the data flow in and out of the device: CE0, CE1, CE2, OE#, WE#, and RP#. In system designs using multiple Q-Flash devices, CE0, CE1, and CE2 (CEx) select the memory device (see Table 4). To drive data out of the device and onto the I/O bus, OE# must be active and WE# must be inactive (V_{IH}).

Table 4: Chip-Enable Truth Table

CE2	CE1	CE0	DEVICE
V_{IL}	V_{IL}	V_{IL}	Enabled
V_{IL}	V_{IL}	V_{IH}	Disabled
V_{IL}	V_{IH}	V_{IL}	Disabled
V_{IL}	V_{IH}	V_{IH}	Disabled
V_{IH}	V_{IL}	V_{IL}	Enabled
V_{IH}	V_{IL}	V_{IH}	Enabled
V_{IH}	V_{IH}	V_{IL}	Enabled
V_{IH}	V_{IH}	V_{IH}	Disabled

NOTE:

For single-chip applications, CE2 and CE1 can be connected to GND.

When reading information in read array mode, the device defaults to asynchronous page mode, thus providing a high data transfer rate for memory subsystems. In this state, data is internally read and stored in a high-speed page buffer. A0–A2 select data in the page buffer. Asynchronous page mode, with a page size of four words or eight bytes, is supported with no additional commands required.

Output Disable

The device outputs are disabled with OE# at a logic HIGH level (V_{IH}). Output pins DQ0–DQ15 are placed in High-Z.

Standby

CE0, CE1, and CE2 can disable the device (see Table 4) and place it in standby mode, which substantially reduces device power consumption. DQ0–DQ15 outputs are placed in High-Z, independent of OE#. If deselected during block erase, program, or lock bit configuration, the ISM continues functioning and consuming active power until the operation completes.

Reset/Power-Down

RP# puts the device into the reset/power-down mode when set to V_{IL}.

During read, RP# LOW deselects the memory, places output drivers in High-Z, and turns off internal circuitry. RP# must be held LOW for a minimum of $^{t}PLPH$. ^{t}RWH is required after return from reset mode until initial memory access outputs are valid. After this wake-up interval, normal operation is restored. The command execution logic (CEL) is reset to the read array mode and the status register is set to 80h.

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During block erase, program, or lock bit configuration, RP# LOW aborts the operation. In default mode, STS transitions LOW and remains LOW for a maximum time of ^{t}PLPH + ^{t}PHRH, until the RESET operation is complete. Any memory content changes are no longer valid; the data may be partially corrupted after a program or partially changed after an erase or lock bit configuration. After RP# goes to logic HIGH (V_{IH}), and after ^{t}RS, another command can be written.

It is important to assert RP# during system reset. After coming out of reset, the system expects to read from the Flash memory. During block erase, program, or lock bit configuration mode, automated Flash memories provide status information when accessed. When a CPU reset occurs with no Flash memory reset, proper initialization may not occur because the Flash memory may be providing status information instead of array data. Micron Flash memories allow proper initialization following a system reset through the use of the RP# input. RP# should be controlled by the same RESET# signal that resets the system CPU.

Read Query

The READ QUERY operation produces block status information, CFI ID string, system interface information, device geometry information, and extended query information.

Read Identifier Codes

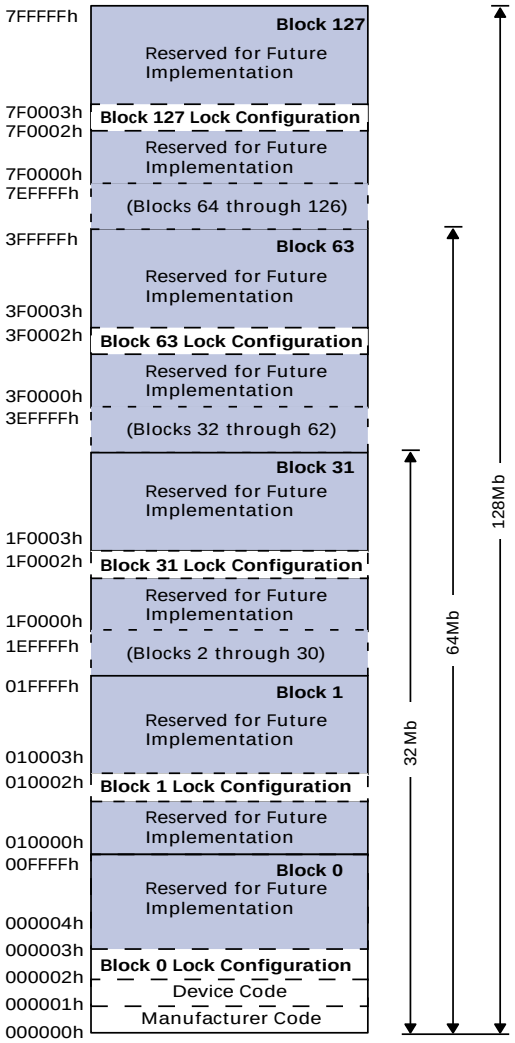
The READ IDENTIFIER CODES operation produces the manufacturer code, device code, and the block lock configuration codes for each block (see Figure 9). The block lock configuration codes identify locked and unlocked blocks.

Write

Writing commands to the CEL allows reading of device data, query, identifier codes, and reading and clearing of the status register. In addition, when V_{PEN} = V_{PENH}, block erasure, program, and lock bit configuration can also be performed.

The BLOCK ERASE command requires suitable command data and an address within the block. The BYTE/WORD PROGRAM command requires the command and address of the location to be written to. The CLEAR BLOCK LOCK BITS command requires the command and any address within the device. Set BLOCK LOCK BITS command requires the command and the block to be locked. The CEL does not occupy an addressable memory location. It is written to when the device is enabled and WE# is LOW. The address and data needed to execute a command are latched on the rising edge of WE# or the first edge of CEx that disables the device (see Table 4 on page 14). Standard microprocessor write timings are used.

Figure 9: Device Identifier Code Memory Map



NOTE:

When obtaining these identifier codes, A0 is not used in either x8 or x16 modes. Data is always given on the LOW byte in x16 mode (upper byte contains 00h).

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Bus Operation

All bus cycles to and from the Flash memory must conform to the standard microprocessor bus cycles. The local CPU reads and writes Flash memory in-system.

Table 5: Bus Operations

MODE	RP#	CE0, CE1, CE2[1]	OE#[2]	WE#[2]	ADDRESS	VPEN	DQ[3]	STS DEFAULT MODE	NOTES
Read Array	VIH	Enabled	VIL	VIH	X	X	DOUT	High-Z[4]	5, 6, 7
Output Disable	VIH	Enabled	VIH	VIH	X	X	High-Z	X	
Standby	VIH	Disabled	X	X	X	X	High-Z	X	
Reset/Power-down Mode	VIL	X	X	X	X	X	High-Z	High-Z[4]	
Read Identifier Codes	VIH	Enabled	VIL	VIH	See Figure 9	X		High-Z[4]	8
Read Query	VIH	Enabled	VIL	VIH	See Table 9	X		High-Z[4]	9
Read Status (ISM off)	VIH	Enabled	VIL	VIH	X	X			
Read Status (ISM On) DQ 7 DQ15–DQ8 DQ6–DQ0	VIH	Enabled	VIL	VIH	X	X	 DOUT High-Z High-Z		
Write	VIH	Enabled	VIH	VIL	X	VPENH	DIN	X	7, 10, 11

NOTE:

1. See Table 4 on page 14 for valid CE configurations.
2. OE# and WE# should never be enabled simultaneously.
3. DQ refers to DQ0–DQ7 if BYTE# is LOW and DQ0–DQ15 if BYTE# is HIGH.
4. High-Z is VOH with an external pull-up resistor.
5. Refer to DC Characteristics. When VPEN ≤ VPENLK, memory contents can be read, but not altered.
6. X can be VIL or VIH for control and address pins, and VPENLK or VPENH for VPEN. See DC Characteristics for VPENLK and VPENH voltages.
7. In default mode, STS is VOL when the ISM is executing internal block erase, program, or lock bit configuration algorithms. It is VOH when the ISM is not busy, in block erase suspend mode (with programming inactive), program suspend mode, or reset/power-down mode.
8. See Read Identifier Codes section for read identifier code data.
9. See Read Query Mode Command section for read query data.
10. Command writes involving block erase, program, or lock bit configuration are reliably executed when VPEN = VPENH and VCC is within specification.
11. Refer to Table 6 on page 17 for valid DIN during a WRITE operation.

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Command Definitions

When the VPEN voltage is < VPENLK, only READ operations from the status register, query, identifier codes, or blocks are enabled. Placing VPENH on VPEN enables BLOCK ERASE, PROGRAM, and LOCK BIT CONFIGURATION operations. Device operations are selected by writing specific commands into the CEL, as seen in Table 6.

Table 6: Micron Q-Flash Memory Command Set Definitions[1]

Notes appear on following page

COMMAND	SCALABLE OR BASIC COMMAND SET[2]	BUS CYCLES REQ'D	FIRST BUS CYCLE			SECOND BUS CYCLE			NOTES
			OPER[3]	ADDR[4]	DATA[5, 6]	OPER[3]	ADDR[4]	DATA[5, 6]	
READ ARRAY	SCS/BCS	1	WRITE	X	FFh				
READ IDENTIFIER CODES	SCS/BCS	≥2	WRITE	X	90h	READ	IA	ID	7
READ QUERY	SCS	≥2	WRITE	X	98h	READ	QA	QD	
READ STATUS REGISTER	SCS/BCS	2	WRITE	X	70h	READ	X	SRD	8
CLEAR STATUS REGISTER	SCS/BCS	1	WRITE	X	50h				
WRITE TO BUFFER	SCS/BCS	> 2	WRITE	BA	E8h	WRITE	BA	N	9, 10, 11
WORD/BYTE PROGRAM	SCS/BCS	2	WRITE	X	40h or 10h	WRITE	PA	PD	12, 13
BLOCK ERASE	SCS/BCS	2	WRITE	BA	20h	WRITE	BA	D0h	11, 12
BLOCK ERASE/ PROGRAM SUSPEND	SCS/BCS	1	WRITE	X	B0h				12, 14
BLOCK ERASE/ PROGRAM RESUME	SCS/BCS	1	WRITE	X	D0h				12
CONFIGURATION	SCS	2	WRITE	X	B8h	WRITE	X	CC	
SET BLOCK LOCK BITS	SCS	2	WRITE	X	60h	WRITE	BA	01h	
CLEAR BLOCK LOCK BITS	SCS	2	WRITE	X	60h	WRITE	X	D0h	15
PROTECTION PROGRAM		2	WRITE	X	C0h	WRITE	PA	PD	

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NOTE:

1. Commands other than those shown in Table 6 on page 17 are reserved for future device implementations and should not be used.
2. The SCS is also referred to as the extended command set.
3. Bus operations are defined in Table 5 on page 16.
4. X = Any valid address within the device
   BA = Address within the block
   IA = Identifier code address; see Figure 9 on page 15 and Table 18 on page 26
   QA = Query data base address
   PA = Address of memory location to be programmed
5. ID = Data read from identifier codes
   QD = Data read from query data base
   SRD = Data read from status register; see Table 19 on page 27 for a description of the status register bits
   PD = Data to be programmed at location PA; data is latched on the rising edge of WE#
   CC = Configuration code
6. The upper byte of the data bus (DQ8–DQ15) during command WRITEs is a "Don't Care" in x16 operation.
7. Following the READ IDENTIFIER CODES command, READ operations access manufacturer, device, and block lock codes. See Block Status Register section for read identifier code data.
8. If the ISM is running, only DQ7 is valid; DQ15–DQ8 and DQ6–DQ0 are placed in High-Z.
9. After the WRITE-to-BUFFER command is issued, check the XSR to make sure a buffer is available for writing.
10. The number of bytes/words to be written to the write buffer = *n* + 1, where *n* = byte/word count argument. Count ranges on this device for byte mode are *n* = 00h to *n* = 1Fh and for word mode, *n* = 0000h to *n* = 000Fh. The third and consecutive bus cycles, as determined by *n*, are for writing data into the write buffer. The CONFIRM command (D0h) is expected after exactly *n* + 1 WRITE cycles; any other command at that point in the sequence aborts the WRITE-to-BUFFER operation. Please see Figure 11 on page 34, WRITE-to-BUFFER Flowchart, for additional information.
11. The WRITE-to-BUFFER or ERASE operation does not begin until a CONFIRM command (D0h) is issued.
12. Attempts to issue a block erase or program to a locked block will fail.
13. Either 40h or 10h is recognized by the ISM as the byte/word program setup.
14. Program suspend can be issued after either the WRITE-to-BUFFER or WORD/BYTE PROGRAM operation is initiated.
15. The CLEAR BLOCK LOCK BITS operation simultaneously clears all block lock bits.

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READ ARRAY Command

The device defaults to read array mode upon initial device power-up and after exiting reset/power-down mode. The read configuration register defaults to asynchronous read page mode. Until another command is written, the READ ARRAY command also causes the device to enter read array mode. When the ISM has started a block erase, program, or lock bit configuration, the device does not recognize the READ ARRAY command until the ISM completes its operation, unless the ISM is suspended via an ERASE or PROGRAM SUSPEND command. The READ ARRAY command functions independently of the V_{PEN} voltage.

READ QUERY MODE Command

This section is related to the definition of the data structure or "data base" returned by the CFI QUERY command. System software should retain this structure to gain critical information such as block size, density, x8/x16, and electrical specifications. When this information has been obtained, the software knows which command sets to use to enable Flash writes or block erases, and otherwise control the Flash component.

Query Structure Output

The query "data base" enables system software to obtain information about controlling the Flash component. The device's CFI-compliant interface allows the host system to access query data. Query data are always located on the lowest-order data outputs (DQ0–DQ7) only. The numerical offset value is the address relative to the maximum bus width supported by the device. On this family of devices, the query table device starting address is a 10h, which is a word address for x16 devices.

For a x16 organization, the first two bytes of the query structure, "Q" and "R" in ASCII, appear on the low byte at word addresses 10h and 11h. This CFI-compliant device outputs 00h data on upper bytes, thus making the device output ASCII "Q" on the LOW byte (DQ7–DQ0) and 00h on the HIGH byte (DQ15–DQ8). At query addresses containing two or more bytes of information, the least significant data byte is located at the lower address, and the most significant data byte is located at the higher address. This is summarized in Table 7. A more detailed example is provided in Table 8.

Table 7: Summary of Query-Structure Output as a Function of Device and Mode

DEVICE TYPE/MODE	QUERY START LOCATION IN MAXIMUM DEVICE BUS WIDTH ADDRESSES	QUERY DATA WITH MAXIMUM DEVICE BUS WIDTH ADDRESSING			QUERY DATA WITH BYTE ADDRESSING		
		HEX OFFSET	HEX CODE	ASCII VALUE	HEX OFFSET	HEX CODE	ASCII VALUE
x16 device x16 mode	10h	10 11 12	0051 0052 0059	Q R Y	20 21 22	51 00 52	Q Null R
x16 device x8 mode	N/A[1]	N/A[1]			20 21 22	51 51 52	Q Q R

NOTE:

1. The system must drive the lowest-order addresses to access all the device's array data when the device is configured in x8 mode. Therefore, word addressing where these lower addresses are not toggled by the system is "Not Applicable" for x8-configured devices.

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Query Structure Overview

The QUERY command makes the Flash component display the CFI query structure or data base. The structure subsections and address locations are outlined in Table 9.

Table 8: Example: Query Structure Output of x16- and x8-Capable Devices

WORD ADDRESSING			BYTE ADDRESSING		
OFFSET	HEX CODE	VALUE	OFFSET	HEX CODE	VALUE
A16–A1	DQ15–DQ0		A7–A0	DQ7–DQ0	
0010h	0051	Q	20h	51	Q
0011h	0052	R	21h	51	Q
0012h	0059	Y	22h	52	R
0013h	P_ID LO	PrVendor	23h	52	R
0014h	P_ID HI	ID#	24h	59	Y
0015h	P LO	PrVendor	25h	59	Y
0016h	P HI	TblAdr	26h	P_ID LO	PrVendor
0017h	A_ID LO	AltVendor	27h	P_ID LO	PrVendor
0018h	A_ID HI	ID#	28h	P_ID HI	ID#
. . .	. . .	. . .	. . .	. . .	. . .

Table 9: Query Structure[1]

OFFSET	SUBSECTION NAME	DESCRIPTION
00h		Manufacturer compatibility code
01h		Device code
(BA+2)h[2]	Block Status Register	Block-specific information
04–0Fh	Reserved	Reserved for vendor-specific information
10h	CFI Query Identification String	Reserved for vendor-specific information
18h	System Interface Information	Command-set ID and vendor data offset
27h	Device Geometry Definition	Flash device layout
P[3]	Primary Extended Query Table	Vendor-defined additional information specific to the primary vendor algorithm

NOTE:

1. Refer to the Query Structure Output section and offset 28h for the detailed definition of offset address as a function of device bus width and mode.
2. BA = Block address beginning location (i.e., 020000h is block two's beginning location when the block size is 64K-word).
3. Offset 15 defines "P," which points to the Primary Extended Query Table.

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CFI Query Identification String

The CFI query identification string verifies whether the component supports the CFI specification. Additionally, it indicates the specification version and supported vendor-specified command set(s).

Table 10: Block Status Register

OFFSET	LENGTH	DESCRIPTION	ADDRESS[1]	VALUE
(BA+2)h[1]	1	Block Lock Status Register	(BA+2)h	00 or 01
		BSR0 Block Lock Status 0 = Unlocked 1 = Locked	(BA+2)h	(Bit 0) 0 or 1
		BSR1–7 Reserved for Future Use	(BA+2)h	(Bit 1–7) 0

NOTE:
1. BA = the beginning location of a block address (i.e., 010000h is block one's [64K-word] beginning location in word mode).

Table 11: CFI Identification

OFFSET	LENGTH	DESCRIPTION	ADDRESS	HEX CODE	VALUE
10h	3	Query-unique ASCII string "QRY"	10h 11h 12h	51 52 59	Q R Y
13h	2	Primary vendor command set and control interface ID code. 16-bit ID code for vendor-specified algorithms	13h 14h	01 00	
15h	2	Extended query table primary algorithm	15h 16h	31 00	
17h	2	Alternate vendor command set and control interface ID code; 0000h means no second vendor-specified algorithm exists	17h 18h	00 00	
19h	2	Secondary algorithm extended query table address; 0000h means none exists	19h 1Ah	00 00	

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System Interface Information

Table 12 provides useful information about optimizing system interface software.

Table 12: System Interface Information

OFFSET	LENGTH	DESCRIPTION	ADDRESS	HEX CODE	VALUE
18h	1	V_{CC} logic supply minimum program/erase voltage Bits 0–3 BCD 100mV Bits 4–7 BCD volts	18h	27	2.7V
1Ch	1	V_{CC} logic supply maximum program/erase voltage Bits 0–3 BCD 100mV Bits 4–7 BCD volts	1Ch	36	3.6V
1Dh	1	V_{PP} [programming] supply minimum program/erase voltage Bits 0–3 BCD 100mV Bits 4–7 Hex volts	1Dh	00	0.0V
1Eh	1	V_{PP} [programming] supply maximum program/erase voltage Bits 0–3 BCD 100mV Bits 4–7 Hex volts	1Eh	00	0.0V
1Fh	1	"n" such that typical single word program timeout = 2^nµs	1Fh	07	128µs
20h	1	"n" such that typical max. buffer write timeout = 2^nms	20h	07	128µs
21h	1	"n" such that typical block erase timeout = 2^nµs	21h	0A	1s
22h	1	"n" such that typical full chip erase timeout = 2^nms	22h	00	N/A
23h	1	"n" such that word program timeout = 2^n times typical	23h	04	2ms
24h	1	"n" such that typical max. buffer write timeout = 2^n times typical	24h	04	2ms
25h	1	"n" such that maximum block erase timeout = 2^n times typical	25h	04	16s
26h	1	"n" such that maximum chip erase timeout = 2^n times typical	26h	00	N/A

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Device Geometry Definition

Tables 13 and 14 provide important details about the device geometry.

Table 13: Device Geometry Definitions

OFFSET	LENGTH	DESCRIPTION	CODE (see table 14 below)		
27h	1	"n" such that device size= 2^n in number of bytes	27h		
28h	2	Flash device interface: x8 async, x16 async, x8/x16 async; 28:00 29:00, 28:01 29:00, 28:02 29:00	28h 29h	02 00	x8/x16
2Ah	2	"n" such that maximum number of bytes in write buffer = 2n	2Ah 2Bh	05 00	32
2Ch	1	Number of erase block regions within device: 1. x = 0 means no erase blocking; the device erases in "bulk" 2. x specifies the number of device or partition regions with one or more contiguous same-size erase blocks 3. Symmetrically blocked partitions have one blocking region 4. Partition size = (total blocks) x (individual block size)	2Ch	01	1
2Dh	4	Erase Block Region 1 Information Bits 0–15 = y; y + 1 = number of identical-size erase blocks Bits 16–31 = z; region erase block(s) size are z x 256 bytes	2Dh 2Eh 2Fh 30h		

Table 14: Device Geometry Definition Codes

ADDRESS	32Mb	64Mb	128Mb
27h	16	17	18
28h	02	02	02
29h	00	00	00
2Ah	05	05	05
2Bh	00	00	00
2Ch	01	01	01
2Dh	1F	3F	7F
2Eh	00	00	00
2Fh	00	00	00
30h	02	02	02

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Primary Vendor-Specific Extended-Query Table

Table 15 includes information about optional Flash features and commands and other similar information.

Table 15: Primary Vendor-Specific Extended-Query

OFFSET[1] P = 31h	DESCRIPTION (OPTIONAL FLASH FEATURES AND COMMANDS)	ADDRESS	HEX CODE	VALUE
(P+0)h (P+1)h (P+2)h	Primary extended query table Unique ASCII string, PRI	31h 32h 33h	50 52 49	P R I
(P+3)h	Major version number, ASCII	34h	31	1
(P+4)h	Minor version number, ASCII	35h	31	1
(P+5)h (P+6)h (P+7)h (P+8)h	Optional feature and command support (1 = yes, 0 = no) bits 9–31are reserved; undefined bits are "0." If bit 31 is "1," then another 31-bit field of optional features follows at the end of the bit 30 field. Bit 0 Chip erase supported = no = 0 Bit 1 Suspend erase supported = yes = 1 Bit 2 Suspend program supported = yes = 1 Bit 3 Legacy lock/unlock supported = no = 0 Bit 4 Queued erase supported = no = 0 Bit 5 Instant Individual block locking supported = no = 0 Bit 6 Protection bits supported = yes = 1 Bit 7 Page mode read supported = yes = 1	36h 37h 38h 39h	C6h 00 00 00	
(P+9)h	Supported functions after suspend: read array, status, query Other supported operations: Bits 1–7 Reserved; undefined bits are "0" Bit 0 Program supported after erase suspend = yes = 1	3Ah	01	
(P+A)h (P+B)h	Block status register mask Bits 2–15 Reserved; undefined bits are "0" Bit 0 Block lock bit status register active = yes = 1 Bit 1 Block lock down bit status active = no = 0	3Bh 3Ch	01 00	
(P+C)h	V_{CC} logic supply highest-performance program/erase voltage Bits 0–3 BCD value in 100mV Bits 4–7 BCD value in volts	3Dh	33	3.3V
(P+D)h	V_{PP} optimum program/erase supply voltage Bits 0–3 BCD value in 100mV Bits 4–7 Hex value in volts	3Eh	00	0.0V

NOTE:

1. The variable "P" is a pointer which is defined at CFI offset 15h.

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Table 16: Protection Register Information

OFFSET[1] P = 31h	DESCRIPTION (Optional Flash Features and Commands)	ADDRESS	HEX	VALUE CODE
(P+E)h	Number of protection register fields in JEDEC ID space. "00h" indicates that 256 protection bytes are available.	3Fh	01	01
(P+F)h (P+10)h (P+11)h (P+12)h	Protection Field 1: Protection Description This field describes user-available, one-time programmable (OTP) protection register bytes. Some are pre-programmed with device-unique serial numbers; others are user-programmable. Bits 0–15 point to the protection register lock byte, the section's first byte. The following bytes are factory-pre-programmed and user-programmable. Bits 0–7 Lock/bytes JEDEC-plane physical low address Bits 8–15 Lock/bytes JEDEC-plane physical high address Bits 16–23 "n" such that 2n = factory pre-programmed bytes Bits 24–31 "n" such that 2n = user-programmable bytes	40h	00	00h

NOTE:
1. The variable "P" is a pointer which is defined at CFI offset 15h.

Table 17: Burst READ Information

OFFSET[1] P = 31h	DESCRIPTION (Optional Flash Features and Commands)	ADDRESS	HEX	VALUE CODE
(P+13)h	Page Mode Read Capability Bits 0–7 = "n" such that 2n Hex value represents the number of read page bytes. See offset 28h for device word width to determine page mode data output width. 00h indicates no read page buffer.	44h	03	8 byte
(P+14)h	Number of synchronous mode read configuration fields that follow. 00h indicates no burst capability.	45h	00	
(P+15)h	Reserved for future use.	46h		

NOTE:
1. The variable "P" is a pointer which is defined at CFI offset 15h.

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READ IDENTIFIER CODES Command

Writing the READ IDENTIFIER CODES command initiates the IDENTIFIER CODE operation. Following the writing of the command, READ cycles from addresses shown in Figure 9 on page 15 retrieve the manufacturer, device, and block lock configuration codes (see Table 18 on page 26 for identifier code values). Page mode READs are not supported in this read mode. To terminate the operation, write another valid command. The READ IDENTIFIER CODES command functions independently of the VPEN voltage. This command is valid only when the ISM is off or the device is suspended. See Table 18 on page 26 for read identifier codes.

READ STATUS REGISTER Command

The status register may be read at any time by writing the READ STATUS REGISTER command to determine the successful completion of programming, block erasure, or lock bit configuration. After writing this command, all subsequent READ operations output data from the status register until another valid command is written. Page mode READs are not supported in this read mode.

The status register contents are latched on the falling edge of OE# or the first edge of CEx that enables the device (seeTable 4 on page 14). To update the status register latch, OE# must toggle to VIH or the device must be disabled before further READs. The READ STATUS REGISTER command functions independently of the VPEN voltage. During a program, block erase, set block lock bits, or clear block lock bits command sequence, only SR7 is valid until the ISM completes or suspends the operation. Device I/O pins DQ0–DQ6 and DQ8–DQ15 are placed in High-Z. When the operation completes or suspends (check status register bit 7), all contents of the status register are valid during a READ.

Table 18: Identifier Codes

CODE	ADDRESS[1]	DATA
Manufacturer Compatibility Code[2] Intel ManID Micron ManID	X00000h	 (00) 89 (00) 2C
Device Code • 32Mb • 64Mb • 128Mb	X00001h	 (00) 16 (00) 17 (00) 18
Block Lock Configuration • Block is Unlocked • Block is Locked • Reserved for Future Use	XX0002h[3]	 DQ0 = 0 DQ0 = 1 DQ1–DQ7

NOTE:

1. A0 is not used in either x8 or x16 modes when obtaining the identifier codes. The lowest-order address line is A1. Data is always presented on the low byte in x16 mode (upper byte contains 00h).
2. Different ManID devices are ordered via separate part numbers. See Figure 4 on page 8 for details.
3. X selects the specific block's lock configuration code. See Figure 8 on page 14 for the device identifier code memory map.

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Table 19: Status Register Definitions

ISMS	ESS	ECLBS	PSLBS	VPENS	PSS	DPS	R
7	6	5	4	3	2	1	0

HIGH-Z WHEN BUSY?	STATUS REGISTER BITS	NOTES
No	SR7 = WRITE STATE MACHINE STATUS (ISMS) 1 = Ready 0 = Busy	Check STS or SR7 to determine block erase, program, or lock bit configuration completion. SR6–SR0 are not driven while SR7 = 0.
Yes	SR6 = ERASE SUSPEND STATUS (ESS) 1 = Block Erase Suspended 0 = Block Erase in Progress/Completed	
Yes	SR5 = ERASE AND CLEAR LOCK BITS STATUS (ECLBS) 1 = Error in Block Erasure or Clear Block Bits 0 = Successful Block Erase or Clear Lock Bits	If both SR5 and SR4 are "1s" after a block erase or lock but configuration attempt, an improper command sequence was entered.
Yes	SR4 = PROGRAM AND SET LOCK BIT STATUS (PSLBS) 1 = Error in Programming or Setting Block Lock Bits 0 = Successful Program or Set Block Lock Bits	
Yes	SR3 = PROGRAMMING VOLTAGE STATUS (VPENS) 1 = Low Programming Voltage Detected, Operation Aborted 0 = Programming Voltage OK	SR3 does not provide a continuous voltage level indication. The ISM interrogates and indicates the programming voltage level only after block erase, program, set block lock bits, or clear block lock bits command sequences.
Yes	SR2 = PROGRAM SUSPEND STATUS (PSS) 1 = Program Suspended 0 = Program in Progress/Completed	
Yes	SR1 DEVICE PROTECTSTATUS (DPS) 1 = Block Lock Bit Detected, Operation Aborted 0 = Unlock	SR1 does not provide a continuous indication of block lock bit values. The ISM interrogates the block lock bits only after block erase, program, or lock bit configuration command sequences. It informs the system, depending on the attempted operation, if the block lock bit is set. Read the block lock configuration codes using the READ IDENTIFIER CODES command to determine block lock bits status. SR0 is reserved for future use and should be masked when polling the status register.
Yes	SR0 = RESERVED FOR FUTURE ENHANCEMENTS	

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CLEAR STATUS REGISTER Command

The ISM sets the status register bits SR5, SR4, SR3, and SR1 to "1s." These bits, which indicate various failure conditions, can only be reset by the CLEAR STATUS REGISTER command. Allowing system software to reset these bits can perform several operations (such as cumulatively erasing or locking multiple blocks or writing several bytes in sequence). To determine if an error occurred during the sequence, the status register may be polled. To clear the status register, the CLEAR STATUS REGISTER command (50h) is written. The CLEAR STATUS REGISTER command functions independently of the applied V_{PEN} voltage and is only valid when the ISM is off or the device is suspended.

BLOCK ERASE Command

The BLOCK ERASE command is a two-cycle command that erases one block. First, a block erase setup is written, followed by a block erase confirm. This command sequence requires an appropriate address within the block to be erased. The ISM handles all block preconditioning, erase, and verify. Time tWB after the two-cycle block erase sequence is written, the device automatically outputs status register data when read. The CPU can detect block erase completion by analyzing the output of the STS pin or status register bit SR7. Toggle OE# or CEx to update the status register. Upon block erase completion, status register bit SR5 should be checked to detect any block erase error. When an error is detected, the status register should be cleared before system software attempts corrective actions. The CEL remains in read status register mode until a new command is issued. This two-step setup command sequence ensures that block contents are not accidentally erased. An invalid block erase command sequence results in status register bits SR4 and SR5 being set to "1." Also, reliable block erasure can only occur when V_{CC} is valid and $V_{PEN} = V_{PENH}$. Note that SR3 and SR5 are set to "1" if block erase is attempted while $V_{PEN} \leq V_{PENLK}$. Successful block erase requires that the corresponding block lock bit be cleared. Similarly, SR1 and SR5 are set to "1" if block erase is attempted when the corresponding block lock bit is set.

BLOCK ERASE SUSPEND Command

The BLOCK ERASE SUSPEND command allows block erase interruption in order to read or program data in another block of memory. Writing the BLOCK ERASE SUSPEND command immediately after starting the block erase process requests that the ISM suspend the block erase sequence at an appropriate point in the algorithm. When reading after the BLOCK ERASE SUSPEND command is written, the device outputs status register data. Polling status register bit SR7, followed by SR6, shows when the BLOCK ERASE operation has been suspended. In the default mode, STS also transitions to V_{OH}. ^{t}LES defines the block erase suspend latency. At this point, a READ ARRAY command can be written to read data from blocks other than that which is suspended. During erase suspend to program data in other blocks, a program command sequence can also be issued. During a PROGRAM operation with block erase suspended, status register bit SR7 returns to "0" and STS output (in default mode) transitions to V_{OL}. However, SR6 remains "1" to indicate block erase suspend status. Using the PROGRAM SUSPEND command, a program operation can also be suspended. Resuming a SUSPENDED programming operation by issuing the Program Resume command enables the suspended programming operation to continue. To resume the suspended erase, the user must wait for the programming operation to complete before issuing the Block ERASE RESUME command. While block erase is suspended, the only other valid commands are READ QUERY, READ STATUS REGISTER, CLEAR STATUS REGISTER, CONFIGURE, and BLOCK ERASE RESUME. After a BLOCK ERASE RESUME command to the Flash memory is completed, the ISM continues the block erase process. Status register bits SR6 and SR7 automatically clear and STS (in default mode) returns to V_{OL}. After the ERASE RESUME command is completed, the device automatically outputs status register data when read. V_{PEN} must remain at V_{PENH} (the same V_{PEN} level used for block erase) during block erase suspension. Block erase cannot resume during block erase suspend until PROGRAM operations are complete.

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WRITE-to-BUFFER Command

The write-to-buffer command sequence is initiated to program the Flash device via the write buffer. A buffer can be loaded with a variable number of bytes, up to the buffer size, before writing to the Flash device. First, the WRITE-to-BUFFER SETUP command is issued, along with the block address (see Figure 11 on page 34). Then, the extended status register (XSR; see Table 20) information is loaded and XSR7 indicates "buffer available" status. If XSR7 = 0, the write buffer is not available. To retry, issue the Write-to-Buffer setup command with the block address and continue monitoring XSR7 until XSR7 = 1. When XSR7 transitions to "1," the buffer is ready for loading new data. Then the part is given a word/byte count with the block address. On the next write, a device start address is given, along with the write buffer data. Depending on the count, subsequent writes provide additional device addresses and data. All subsequent addresses must lie within the start address plus the count.

The device internally programs many Flash cells in parallel. Due to this parallel programming, maximum programming performance and lower power are obtained by aligning the start address at the beginning of a write buffer boundary (i.e., A0–A4 of the start address = 0).

When the final buffer data is given, a WRITE CONFIRM command is issued, thus programming the ISM to begin copying the buffer data to the Flash array. If the device receives a command other than WRITE CONFIRM, an invalid command/sequence error is generated and status register bits SR5 and SR4 are set to "1." For additional BUFFER WRITEs, issue another WRITE-to-BUFFER SETUP command and check XSR7.

If an error occurs during a write, the device stops writing, and status register bit SR4 is set to a "1" to indicate a program failure. The ISM only detects errors for "1s" that do not successfully program to "0s." When a program error is detected, the status register should be cleared. Note that the device does not accept any more WRITE-to-BUFFER commands any time SR4 and/or SR5 is set. In addition, if the user attempts to program past an erase block boundary with a WRITE-to-BUFFER command, the device aborts the WRITE-to-BUFFER operation and generates an invalid command/sequence error, and status register bits SR5 and SR4 are set to "1."

Reliable BUFFERED WRITEs can only occur when $V_{PEN} = V_{PENH}$. If a BUFFERED WRITE is attempted while $V_{PEN} \leq V_{PENLK}$, status register bits SR4 and SR3 are set to "1." Buffered write attempts with invalid V_{CC} and V_{PEN} voltages produce spurious results and should not be attempted. Finally, the corresponding block lock bit should be reset for successful programming. When a BUFFERED WRITE is attempted while the corresponding block lock bit is set, SR1 and SR4 are set to "1."

Table 20: Extended Status Register Definitions (XSR)

WBS	RESERVED
7	6–0

HIGH-Z WHEN BUSY?	STATUS REGISTER BITS	NOTES
No	XSR7 = WRITE BUFFER STATUS (WBS) 1 = Write Buffer Available 0 = Write Buffer Not Available	After a BUFFER WRITE command, ZXSR7 = 1 indicates that a write buffer is available.
Yes	XSR6–XSR0 = RESERVED FOR FUTURE ENHANCEMENTS	SR6–SR0 are reserved for future use and should be masked when polling the status register.

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BYTE/WORD PROGRAM Commands

A two-cycle command sequence executes a byte/word program setup. This program setup (standard 40h or alternate 10h) is written, followed by a second write that specifies the address and data (latched on the rising edge of WE#). Next, the ISM takes over to internally control the programming and program verify algorithms. When the program sequence is written, the device automatically outputs status register data when read (see Figure 12 on page 35). The CPU can detect the completion of the program event by analyzing the STS pin or status register bit SR7.

Upon program completion, status register bit SR4 should be checked. The status register should be cleared if a program error is detected. The ISM only detects errors for "1s" that do not successfully program to "0s." The CEL remains in read status register mode until it receives another command.

Reliable byte/word programs can only occur when V_{CC} and V_{PEN} are valid. Status register bits SR4 and SR3 are set to "1" if a byte/word program is attempted while $V_{PEN} \leq V_{PENLK}$. The corresponding block lock bit should be cleared for successful byte/word programs. If BYTE/WORD is attempted while the corresponding block lock bit is set, SR1 and SR4 are set to "1."

PROGRAM SUSPEND Command

The PROGRAM SUSPEND command enables program interruption to read data in other Flash memory locations. After starting the programming process, writing the PROGRAM SUSPEND command requests that the ISM suspend the program sequence at a predetermined point in the algorithm. When the PROGRAM SUSPEND command is written, the device continues to output status register data when read. Polling status register bit SR7 can determine when the programming operation has been suspended. When SR7 = 1, SR2 is also set to "1" to indicate that the device is in the program suspend mode. STS in RY/BY# level mode also transitions to V_{OH}. Note that ^{t}LPS defines the program suspend latency.

Hence, a READ ARRAY command can be written to read data from unsuspended locations. While programming is suspended, the only other valid commands are READ QUERY, READ STATUS REGISTER, CLEAR STATUS REGISTER, CONFIGURE, and PROGRAM RESUME. When the PROGRAM RESUME command is written, the ISM continues the programming process. Status register bits SR2 and SR7 automatically clear and STS in RY/BY# mode returns to V_{OL}. After the PROGRAM RESUME command is written, the device automatically outputs status register data when read. V_{PEN} must remain at V_{PENH} and V_{CC} must remain at valid V_{CC} levels (the same V_{PEN} and V_{CC} levels used for programming) while in program suspend mode. Refer to Figure 13 on page 36 (PROGRAM SUSPEND/RESUME Flowchart).

SET READ CONFIGURATION Command

Q-Flash memory does not support the SET READ CONFIGURATION command. The devices default to the asynchronous page mode. If this command is given, the operation of the device will not be affected.

READ Configuration

Micron's Q-Flash devices support both asynchronous page mode and standard word/byte READs without configuration requirement. Status register and identifier only support standard word/byte single READ operations.

STS CONFIGURATION Command

Using the CONFIGURATION command, the STS pin can be configured to different states. Once configured, the STS pin remains in that configuration until another configuration command is issued, RP# is asserted low, or the device is powered down. Initially, the STS pin defaults to RY/BY# operation where RY/BY# goes LOW to indicate that the state machine is busy. When HIGH, RY/BY# indicates that either the state machine is ready for a new operation or it is suspended. Table 21 on page 31, Configuration Coding Definitions, shows the possible STS configurations. To change the STS pin to other modes, the CONFIGURATION command is given, followed by the desired configuration code. The three alternate configurations are all pulse modes and may be used as a system interrupt. With these configurations, bit 0 controls erase complete interrupt pulse, and bit 1 controls program complete interrupt pulse. Providing the 00h configuration code with the CONFIGURATION command resets the STS pin to the default RY/BY# level mode. Table 21 on page 31 describes possible configurations and usage. The CONFIGURATION command can only be given when the device is not busy or suspended. When configured in one of the pulse modes, the STS pin pulses LOW with a typical pulse width of 250ns. Check SR7 for device status. An invalid configuration code results in status register bits SR4 and SR5 being set to "1."

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Table 21: Configuration Coding Definitions[1]

DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
RESERVED						PULSE ON PROGRAM COMPLETE[2]	PULSE ON ERASE COMPLETE[2]

DQ1–DQ0 = STS Configuration Codes	NOTES
00 = Default, RY/BY# level mode (device ready) indication	Used to control HOLD to a memory controller to prevent accessing a Flash memory subsystem while any Flash device's ISM is busy.
01 = Pulse on Erase Complete	Used to generate a system interrupt pulse when any Flash device is an array has completed a BLOCK ERASE or sequence of queued BLOCK ERASEs; helpful for reformatting blocks after file system free space reclamation or "clean-up."
10 = Pulse on Program Complete	Used to generate a system interrupt pulse when any Flash device in an array has completed a PROGRAM operation. Provides highest performance for enabling continuous BUFFER WRITE operations.
11 = Pulse on Erase or Program Complete	Used to generate system interrupts to trigger enabling of Flash arrays when either ERASE or PROGRAM operations are completed and a common interrupt service routine is desired.

NOTE:
1. An invalid configuration code will result in both SR4 and SR5 being set.
2. When the device is configured in one of the pulse modes, the STS pin pulses LOW with a typical pulse width of 250ns.

SET BLOCK LOCK BITS Command

A flexible block locking and unlocking scheme is enabled via a combination of block lock bits. The block lock bits gate PROGRAM and ERASE operations. Using the SET BLOCK LOCK BITS command, individual block lock bits can be set. This command is invalid when the ISM is running or when the device is suspended. SET BLOCK LOCK BITS commands are executed by a two-cycle sequence. The set block lock bits setup, along with appropriate block address, is followed by the set block lock bits confirm and an address within the block to be locked. The ISM then controls the set lock bit algorithm. When the sequence is written, the device automatically outputs status register data when read (see Figure 16 on page 39). The CPU can detect the completion of the set block lock bit event by analyzing the STS pin output or status register bit SR7. Upon completion of set block lock bits operation, status register bit SR4 should be checked for error. If an error is detected, the status register should be cleared. The CEL remains in read status register mode until a new command is issued. This two-step sequence of setup followed by execution ensures that lock bits are not accidentally set. An invalid SET BLOCK LOCK BITS command results in status register bits SR4 and SR5 being set to "1."

Also, reliable operation occurs only when V_{CC} and V_{PEN} are valid. When $V_{PEN} \le V_{PENLK}$, lock bit contents are protected against any data change.

CLEAR BLOCK LOCK BITS Command

The CLEAR BLOCK LOCK BITS command can clear all set block lock bits in parallel. This command is invalid when the ISM is running or the device is suspended. The CLEAR BLOCK LOCK BITS command is executed by a two-cycle sequence. First, a clear block lock bits setup is written, followed by a CLEAR BLOCK LOCK BITS CONFIRM command. Then the device automatically outputs status register data when read (see Figure 16 on page 39). The CPU can detect completion of the clear block lock bits event by analyzing the STS pin output or the status register bit SR7. When the operation is completed, status register bit SR5 should be checked. If a clear block lock bits error is detected, the status register should be cleared. The CEL remains in read status register mode until another command is issued.

This two-step setup sequence ensures that block lock bits are not accidentally cleared. An invalid CLEAR BLOCK LOCK BITS command sequence results in status register bits SR4 and SR5 being set to "1." Also, a reliable CLEAR BLOCK LOCK BITS operation can only occur when V_{CC} and V_{PEN} are valid. If a clear block lock bits operation is attempted when $V_{PEN} \le$

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VPENLK, SR3 and SR5 are set to "1." If a CLEAR BLOCK LOCK BITS operation is aborted due to VPEN or VCC transitioning out of valid range, block lock bit values are left in an undetermined state. To initialize block lock bit contents to known values, a repeat of CLEAR BLOCK LOCK BITS is required.

PROTECTION REGISTER PROGRAM Command

The 3V Q-Flash memory includes a 128-bit protection register to increase the security of a system design. For example, the number contained in the protection register can be used for the Flash component to communicate with other system components, such as the CPU or ASIC, to prevent device substitution. The 128 bits of the protection register are divided into two 64-bit segments. One of the segments is programmed at the Micron factory with a unique and unchangeable 64-bit number. The other segment is left blank for customers to program as needed. After the customer segment is programmed, it can be locked to prevent reprogramming.

Reading the Protection Register

The protection register is read in the identification read mode. The device is switched to identification read mode by writing the READ IDENTIFIER command (90h). When in this mode, READ cycles from addresses shown in Table 22 on page 33 or Table 23 on page 33 retrieve the specified information. To return to read array mode, the READ ARRAY command (FFh) must be written.

Programming the Protection Register

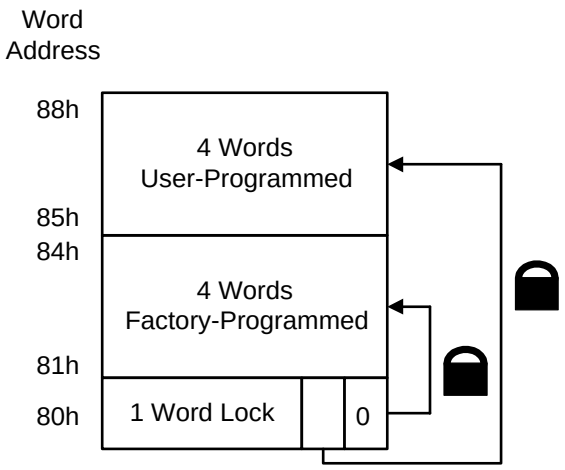
The protection register bits are programmed with two-cycle PROTECTION PROGRAM commands.

The 64-bit number is programmed 16 bits at a time for word-wide parts and eight bits at a time for byte-wide parts. First, the PROTECTION PROGRAM SETUP command, C0h, is written. The next write to the device latches in addresses and data, and programs the specified location. The allowable addresses are shown in Table 22 on page 33 and Table 23 on page 33. Any attempt to address PROTECTION PROGRAM commands outside the defined protection register address space results in a status register error (program error bit SR4 is set to "1"). Attempting to program a locked protection register segment results in a status register error (program error bit SR4 and lock error bit SR1 are set to "1").

Locking the Protection Register

By programming bit 1 of the PR-LOCK location to "0," the user-programmable segment of the protection register is lockable. To protect the unique device number, bit 0 of this location is programmed to "0" at the Micron factory. Bit 1 is set using the PROTECTION PROGRAM command to program "FFFDh" to the PR-LOCK location. When these bits have been programmed, no further changes can be made to the values stored in the protection register. PROTECTION PROGRAM commands to a locked section will result in a status register error (program error bit SR4 and lock error bit SR1 are set to "1"). Note that the protection register lockout state is not reversible.

Figure 10: Protection Register Memory Map



NOTE:

A0 is not used in x16 mode when accessing the protection register map (see Table 22 on page 33 for x16 addressing). A0 is used for x8 mode (see Table 23 on page 33 for x8 addressing).

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Table 22: Word-Wide Protection Register Addressing

WORD	USE	A8	A7	A6	A5	A4	A3	A2	A1
LOCK	Both	1	0	0	0	0	0	0	0
0	Factory	1	0	0	0	0	0	0	1
1	Factory	1	0	0	0	0	0	1	0
2	Factory	1	0	0	0	0	0	1	1
3	Factory	1	0	0	0	0	1	0	0
4	User	1	0	0	0	0	1	0	1
5	User	1	0	0	0	0	1	1	0
6	User	1	0	0	0	0	1	1	1
7	User	1	0	0	0	1	0	0	0

Table 23: Byte-Wide Protection Register Addressing

BYTE	USE	A8	A7	A6	A5	A4	A3	A2	A1	A0
LOCK	Both	1	0	0	0	0	0	0	0	0
0	Factory	1	0	0	0	0	0	0	1	0
1	Factory	1	0	0	0	0	0	0	1	1
2	Factory	1	0	0	0	0	0	1	0	0
3	Factory	1	0	0	0	0	0	1	0	1
4	Factory	1	0	0	0	0	0	1	1	0
5	Factory	1	0	0	0	0	0	1	1	1
6	Factory	1	0	0	0	0	1	0	0	0
7	Factory	1	0	0	0	0	1	0	0	1
8	User	1	0	0	0	0	1	0	1	0
9	User	1	0	0	0	0	1	0	1	1
A	User	1	0	0	0	0	1	1	0	0
B	User	1	0	0	0	0	1	1	0	1
C	User	1	0	0	0	0	1	1	1	0
D	User	1	0	0	0	0	1	1	1	1
E	User	1	0	0	0	1	0	0	0	0
F	User	1	0	0	0	1	0	0	0	1

NOTE:

All address lines not specified in the above tables must be “0” when accessing the protection register (i.e., A22–A9 = 0).

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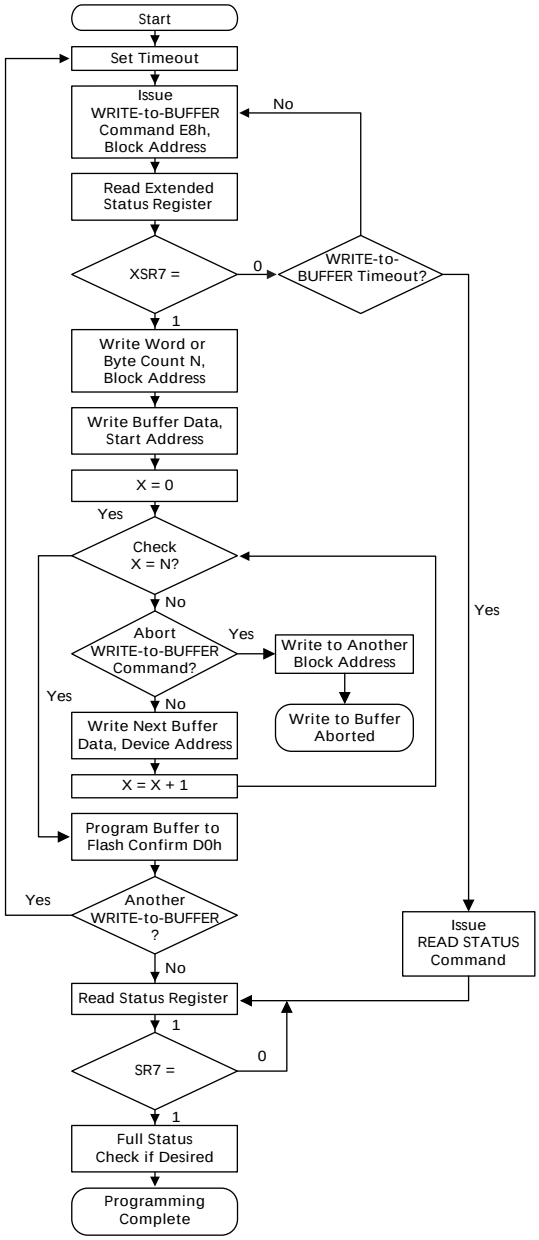
Figure 11: WRITE-to-BUFFER Flowchart



BUS OPERATION	COMMAND	COMMENTS	NOTES
WRITE	WRITE-to-BUFFER	Data = E8h Block Address	
READ		XSR7 = Valid Addr = Block Address	
STANDBY		Check XSR7 1 = Write Buffer Available 0 = Write Buffer Not Available	
WRITE		Data = N = Word/Byte Count N = 0 Corresponds to Count = 1 Addr = Block Address	1, 2
WRITE		Data = Write Buffer Data Addr = Device Start Address	3, 4
WRITE		Data = Write Buffer Data Addr = Device Address	5, 6
WRITE	Program Buffer to Flash Confirm	Data = D0h Addr = Block Address	
READ		Status register data with the device enabled, OE# LOW updates the SR Addr = Block Address	7
STANDBY		Check SR7 1 = ISM Ready 0 = ISM Busy	
Full status check can be done after all erase and write sequences complete. Write FFh after the last operation to reset the device to read array mode.			

NOTE:

1. Byte or word count values on DQ0–DQ7 are loaded into the count register. Count ranges on this device for byte mode are *n* = 00h to 1Fh and for word mode are *n* = 0000h to 000Fh.
2. The device now outputs the status register when read (XSR is no longer available).
3. Write buffer contents will be programmed at the device start address or destination Flash address.
4. Align the start address on a write buffer boundary for maximum programming performance (i.e., A4–A0 of the start address = 0).
5. The device aborts the WRITE-to-BUFFER command if the current address is outside of the original block address.
6. The status register indicates an "improper command sequence" if the WRITE-to-BUFFER command is aborted. Follow this with a CLEAR STATUS REGISTER command.
7. Toggling OE# (LOW to HIGH to LOW) updates the status register. This can be done in place of issuing the READ STATUS REGISTER command.

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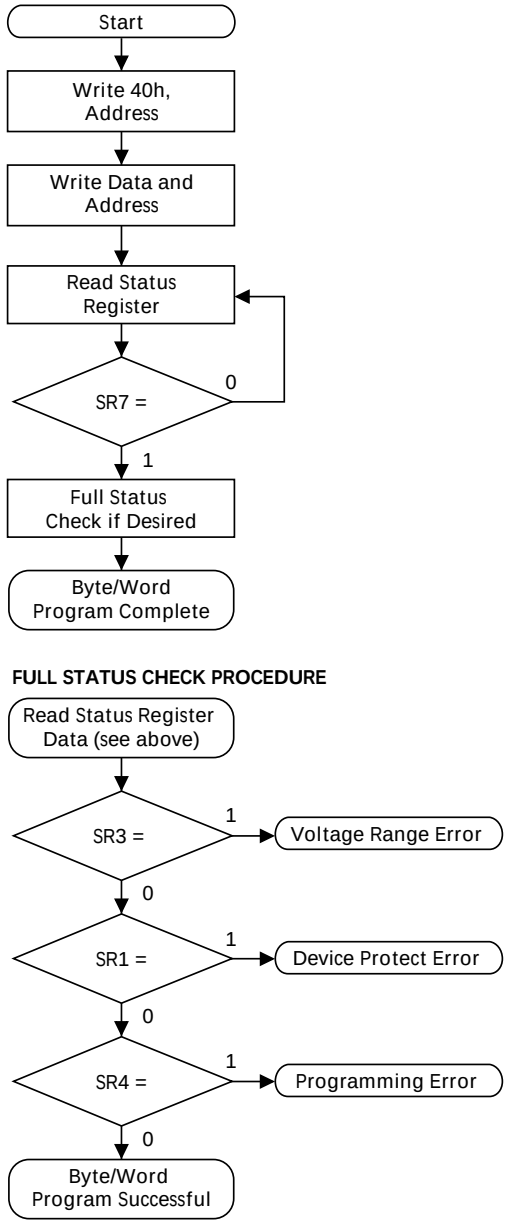
Figure 12: BYTE/WORD PROGRAM Flowchart



BUS OPERATION	COMMAND	COMMENTS
WRITE	SETUP BYTE/ WORD PROGRAM	Data = 40h Addr = Location to be programmed
WRITE	BYTE/WORD PROGRAM	Data = Data to be programmed Addr = Location to be programmed
READ		Status Register Data
STANDBY		Check SR7 1 = ISM Ready 0 = ISM Busy
Toggling OE# (LOW to HIGH to LOW) updates the status register. This can be done in place of issuing the READ STATUS REGISTER command. Repeat for subsequent programming operations. After each program operation or after a sequence of programming operations, an SR full status check can be done. Write FFh after the last program operation to place the device in read array mode.		

BUS OPERATION	COMMAND	COMMENTS
WRITE	SETUP BYTE/ WORD PROGRAM	Check SR3 1 = Programming to Voltage Error Detect
WRITE	BYTE/WORD PROGRAM	Check SR1 1 = Device Protect Detect RP# = V_{IH}, Block Lock Bit is Set Only required for systems implementing lock bit configuration
READ		Status Register Data
STANDBY		Check SR4 1 = Programming Error
Toggling OE# (LOW to HIGH to LOW) updates the status register. This can be done in place of issuing the READ STATUS REGISTER command. Repeat for subsequent programming operations. SR4, SR3, and SR1 are only cleared by the Clear Status Register command in cases where multiple locations are programmed before full status is checked. If an error is detected, clear the status register before attempting retry or other error recovery.		

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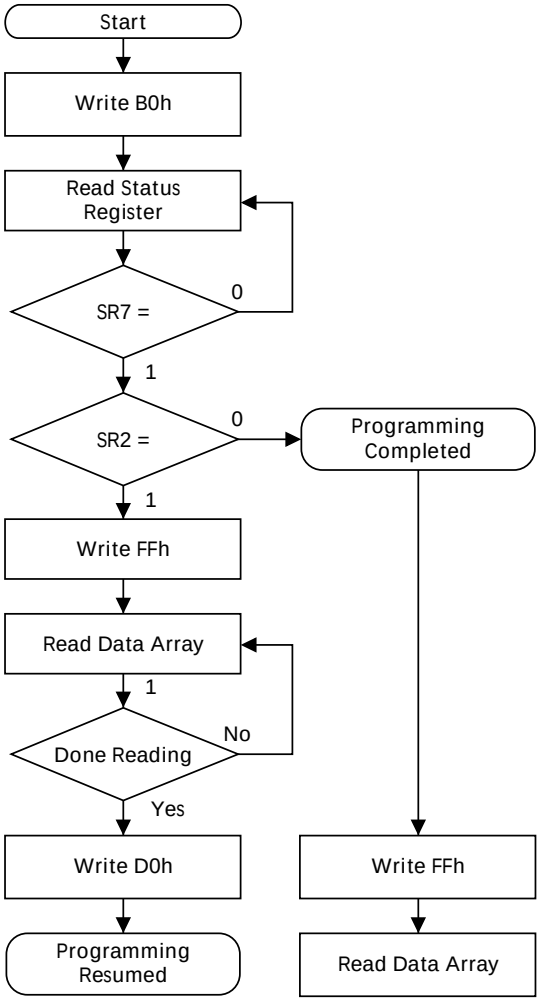
Figure 13: PROGRAM SUSPEND/RESUME Flowchart



BUS OPERATION	COMMAND	COMMENTS
WRITE	PROGRAM SUSPEND	Data = B0h Addr = X
READ		Status Register Data Addr = X
STANDBY		Check SR7 1 = ISM Ready 0 = ISM Busy
STANDBY		Check SR6 1 = Programming Suspend 0 = Programming Completed
WRITE	READ ARRAY	Data = FFh Addr = X
READ		Read array locations other than that being programmed
WRITE	PROGRAM RESUME	Data = D0h Addr =X

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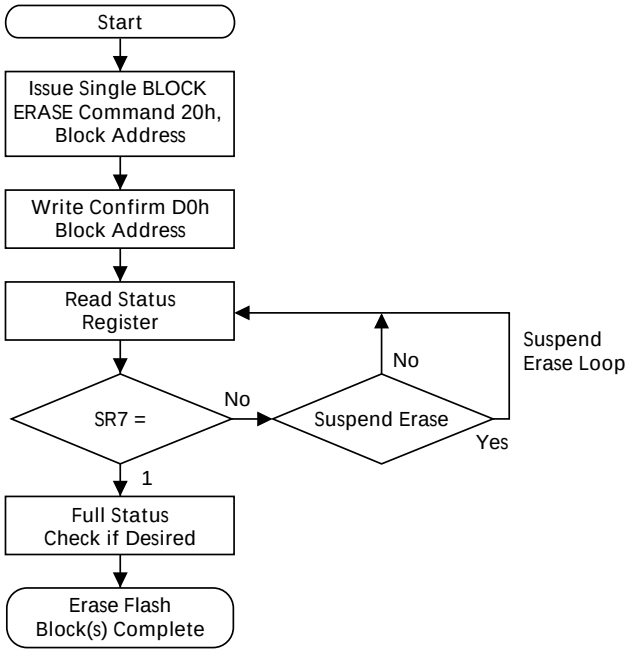
Figure 14: BLOCK ERASE Flowchart



BUS OPERATION	COMMAND	COMMENTS
WRITE	ERASE BLOCK	Data = 20h Addr = Block Address
WRITE	ERASE CONFIRM	Data = D0h Addr = Block Address
READ		Status register data with the device enabled; OE# LOW updates SR Addr = X
STANDBY		Check SR7 1 = ISM Ready 0 = ISM Busy

The erase confirm byte must follow erase setup.

This device does not support erase queuing.

Full status check can be done after all erase and write sequences complete. Write FFh after the last operation to reset the device to read array mode.

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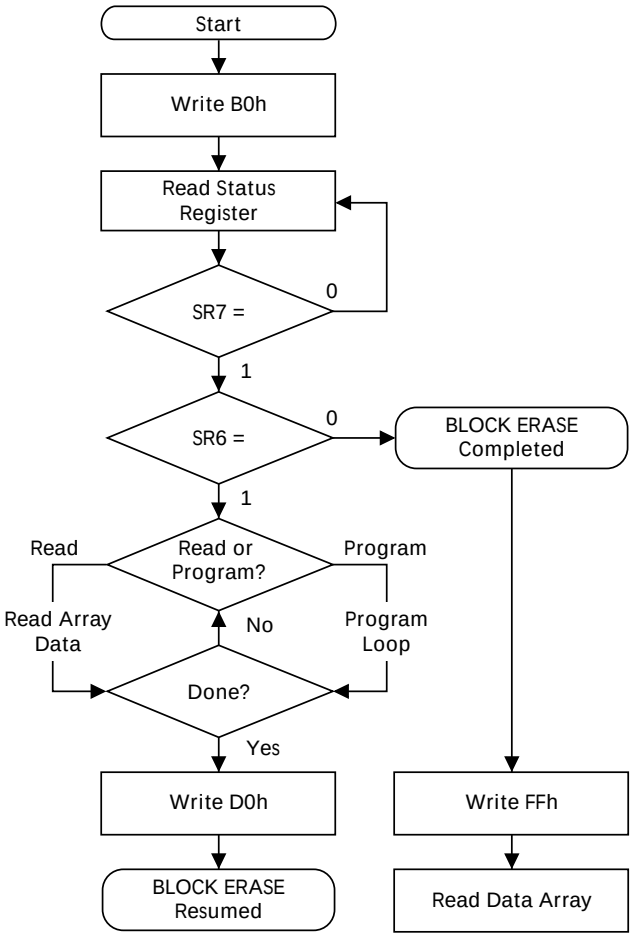
Figure 15: BLOCK ERASE SUSPEND/ RESUME Flowchart



BUS OPERATION	COMMAND	COMMENTS
WRITE	ERASE SUSPEND	Data = B0h Addr = X
READ		Status Register Data Addr = X
STANDBY		Check SR7 1 = ISM Ready 0 = ISM Busy
STANDBY		Check SR6 1 = Block Erase Suspend 0 = Block Erase Completed
WRITE	ERASE RESUME	Data = D0h Addr = X

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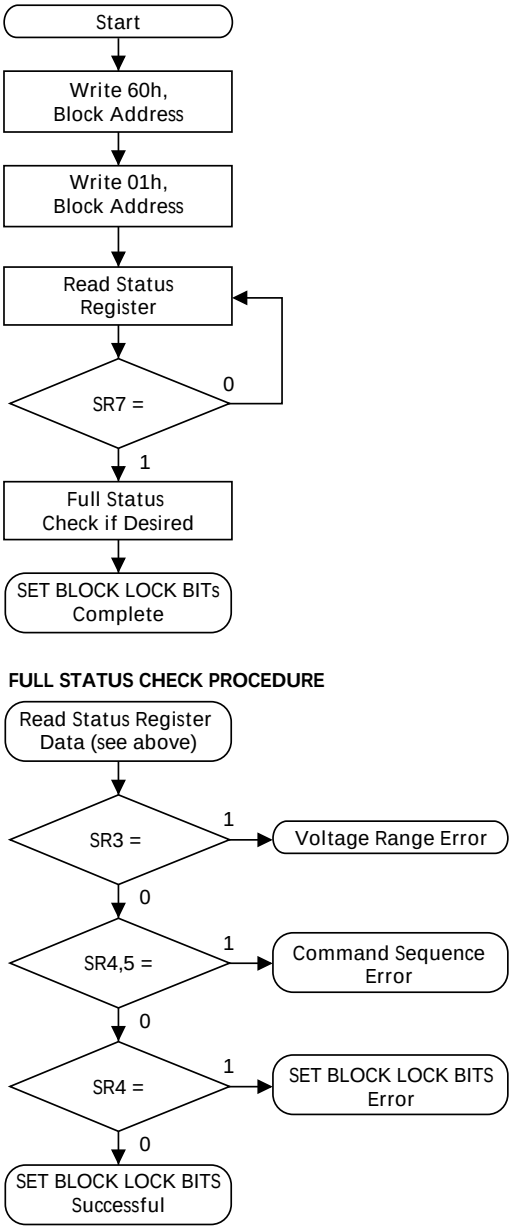
Figure 16: SET BLOCK LOCK BITS Flowchart



BUS OPERATION	COMMAND	COMMENTS
WRITE	SET BLOCK LOCK BITS SETUP	Data = 60h Addr = Block Address
WRITE	SET BLOCK LOCK BITS CONFIRM	Data = 01h Addr = Block Address
READ		Status Register Data
STANDBY		Check SR7 1 = ISM Ready 0 = ISM Busy
Repeat for subsequent lock bit operations. Full status check can be done after each lock bit set operation or after a sequence of lock bit set operations. Write FFh after the last lock bit set operation to place device in read array mode.		

BUS OPERATION	COMMAND	COMMENTS
STANDBY		Check SR3 1= Programming Voltage Error Detect
STANDBY		Check SR4, SR5 Both 1 = Command Sequence Error
STANDBY		Check SR4 1 = Set Block Lock Bits Error
SR5, SR4, and SR3 are only cleared by the Clear Status Register command in cases where multiple lock bits are set before full status is checked. If an error is detected, clear the status register before attempting retry or other error recovery.		

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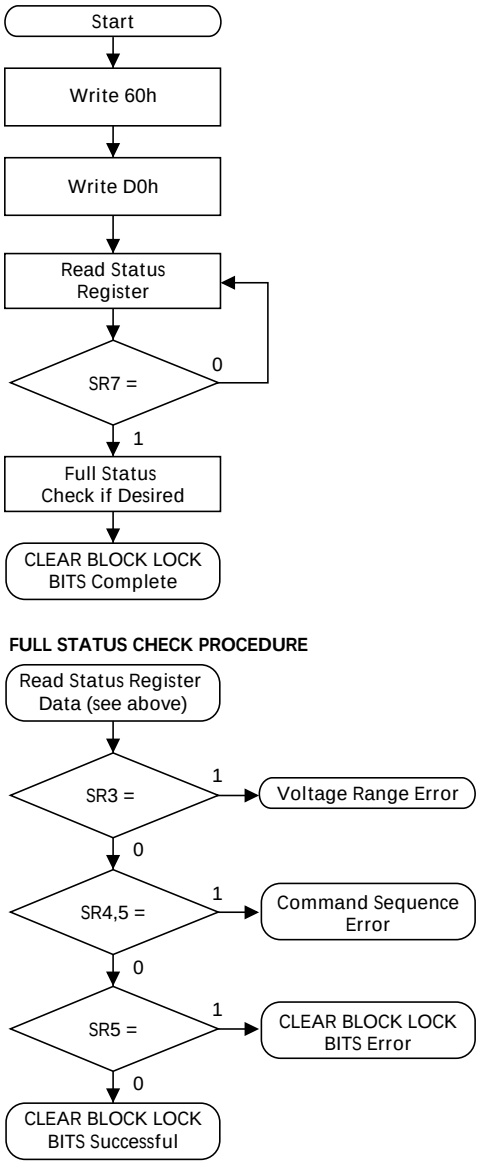
Figure 17: CLEAR BLOCK LOCK BITS Flowchart



BUS OPERATION	COMMAND	COMMENTS
WRITE	CLEAR BLOCK LOCK BITS SETUP	Data = 60h Addr = X
WRITE	CLEAR BLOCK LOCK BITS CONFIRM	Data = D0h Addr = X
READ		Status Register Data
STANDBY		Check SR7 1 = ISM Ready 0 = ISM Busy
Write FFh after the CLEAR BLOCK LOCK BITS operation to place device in read array mode.		

BUS OPERATION	COMMAND	COMMENTS
STANDBY		Check SR3 1= Programming Voltage Error Detect
STANDBY		Check SR4, SR5 Both 1 = Command Sequence Error
STANDBY		Check SR4 1 = Clear Block Lock Bits Error
SR5, SR4, and SR3 are only cleared by the Clear Status Register command. If an error is detected, clear the status register before attempting retry or other error recovery.		

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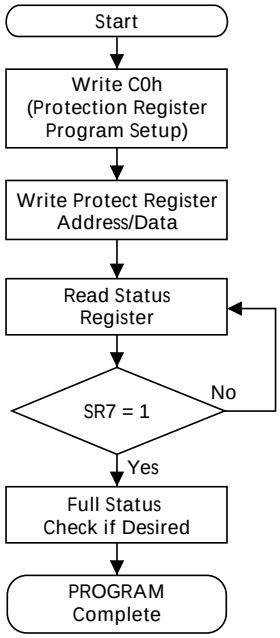
Figure 18: PROTECTION REGISTER PROGRAMMING Flowchart



BUS OPERATION	COMMAND	COMMENTS
WRITE	PROTECTION PROGRAM SETUP	Data = C0h
WRITE	PROTECTION PROGRAM	Data = Data to Program Addr = Location to Program
READ		Status Register Data Toggle CE# or OE# to update status register data
STANDBY		Check SR7 1 = ISM Ready 0 = ISM Busy

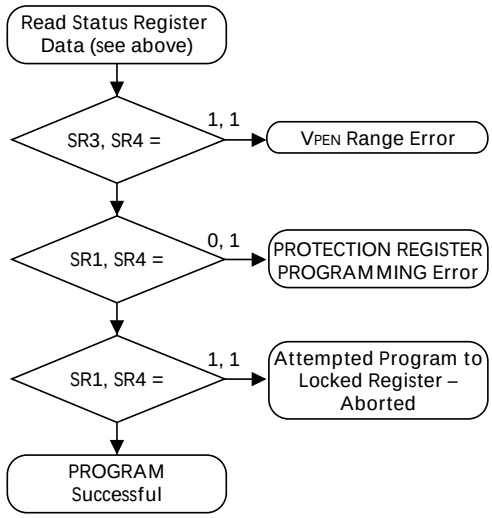
PROTECTION PROGRAM operations can only be addressed within the protection register address space. Addresses outside the defined space will return an error.

Repeat for subsequent programming operations.

SR full status check can be done after each program or after a sequence of program operations.

Write FFh after the last program operation to reset device to read array mode.

FULL STATUS CHECK PROCEDURE



BUS OPERATION	COMMAND	COMMENTS SR1	SR3	SR4	
STANDBY		0	1	1	VPEN LOW
STANDBY		0	1	1	Protection Register Program Error
STANDBY		1	0	1	Register Locked: Aborted

SR3, if set during a program attempt, MUST be cleared before further attempts are allowed by the ISM.

SR1, SR3, and SR4 are only cleared by the CLEAR STATUS REGISTER command, in cases of multiple protection register program operations, before full status is checked.

If an error is detected, clear the status register before attempting retry or other error recovery.

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Design Considerations

Five-Line Output Control

Micron provides five control inputs (CE0, CE1, CE2, OE#, and RP#) to accommodate multiple memory connections in large memory arrays. This control provides the lowest possible memory power dissipation and ensures that data bus contention does not occur.

To efficiently use these control inputs, an address decoder should enable the device (see Table 4 on page 14) while OE# is connected to all memory devices and the system's READ# control line. This ensures that only selected memory devices have active outputs while deselected memory devices are in standby mode. During system power transitions, RP# should be connected to the system POWERGOOD signal to prevent unintended writes. POWERGOOD should also toggle during system reset.

STS and Block Erase, Program, and Lock Bit Configuration

Polling

As an open drain output, STS should be connected to V_{CCQ} by a pull-up resistor to provide a hardware method of detecting block erase, program, and lock bit configuration completion. It is recommended that a 2.5KΩ resistor be used between STS# and V_{CCQ}. In default mode, it transitions low after block erase, program, or lock bit configuration commands and returns to High-Z when the ISM has finished executing the internal algorithm. See the CONFIGURATION command for alternate configurations of the STS pin. STS can be connected to an interrupt input of the system CPU or controller. STS is active at all times. In default mode, it is also High-Z when the device is in block erase suspend (with programming inactive), program suspend, or reset/power-down mode.

Power Supply Decoupling

Device decoupling is required for Flash memory power switching characteristics. There are three supply current issues to consider: standby current levels, active current levels, and transient peaks produced by falling and rising edges of CEx and OE#. Transient current magnitudes depend on the device outputs' capacitive and inductive loading. Two-line control and proper decoupling capacitor selection suppresses transient voltage peaks. Because Micron Q-Flash memory devices draw their power from three V_{CC} pins (these devices do not include a V_{PP} pin), it is recommended that systems without separate power and ground planes attach a 0.1µF ceramic capacitor between each of the device's three V_{CC} pins (this includes V_{CCQ}) and GND. These high-frequency, low-inductance capacitors should be placed as close as possible to package leads on each Micron Q-Flash memory device. Additionally, for every eight devices, a 4.7µF electrolytic capacitor should be placed between V_{CC} and GND at the array's power supply connection.

Reducing Overshoots and Undershoots When Using Buffers or Transceivers

Overshoots and undershoots can sometimes cause input signals to exceed Flash memory specifications as faster, high-drive devices such as transceivers or buffers drive input signals to Flash memory devices. Many buffer/transceiver vendors now carry bus-interface devices with internal output-damping resistors or reduced-drive outputs. Internal output-damping resistors diminish the nominal output drive currents, while still leaving sufficient drive capability for most applications. These internal output-damping resistors help reduce unnecessary overshoots and undershoots by diminishing output-drive currents. When considering a buffer/transceiver interface design to Flash, devices with internal output-damping resistors or reduced-drive outputs should be used to minimize overshoots and undershoots.

V_{CC}, V_{PEN}, and RP# Transitions

If V_{PEN} or V_{CC} falls outside of the specified operating ranges, or RP# is not set to V_{IH}, block erase, program, and lock bit configuration are not guaranteed. If RP# transitions to V_{IL} during block erase, program, or lock bit configuration, STS (in default mode) will remain LOW for a maximum time of $^{t}PLPH + {}^{t}PHRH$, until the RESET operation is complete and the device enters reset/power-down mode. The aborted operation may leave data partially corrupted after programming, or partially altered after an erase or lock bit configuration. Therefore, block erase and lock bit configuration commands must be repeated after normal operation is restored. Device power-off or RP# = V_{IL} clears the status register. The CEL latches commands issued by system software and is not altered by V_{PEN} or CEx transitions, or ISM actions. Its state is read array mode upon power-up, upon exiting reset/power-down mode, or after V_{CC} transitions below V_{LKO}. V_{CC} must be kept at or above V_{PEN} during V_{CC} transitions.

After block erase, program, or lock bit configuration, and after V_{PEN} transitions to V_{PENLK}, the CEL must be placed in read array mode via the READ ARRAY com-

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mand if subsequent access to the memory array is desired. During V_{PEN} transitions, V_{PEN} must be kept at or below V_{CC}.

Power-Up/Down Protection

During power transition, the device itself provides protection against accidental block erasure, programming, or lock bit configuration. Internal circuitry resets the CEL to read array mode at power-up. A system designer must watch out for spurious writes for V_{CC} voltages above V_{LKO} when V_{PEN} is active. Because WE# must be low and the device enabled (see Table 4 on page 14) for a command write, driving WE# to V_{IH} or disabling the device inhibits WRITEs. The CEL's two-step command sequence architecture provides added protection against data alteration. In-system block lock and unlock capability protects the device against inadvertent programming. The device is disabled when RP# = V_{IL} regardless of its control inputs. Keeping V_{PEN} below V_{PENLK} prevents inadvertent data change.

Power Dissipation

Designers must consider battery power consumption not only during device operation, but also for data retention during system idle time. Flash memory's non-volatility increases usable battery life because data is retained when system power is removed.

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Absolute Maximum Ratings*

Temperature under bias expanded:.....-40ºC to +85ºC
Storage Temperature.....-65ºC to +125ºC
For $V_{CC}Q$ = +2.7V to +3.6V
Voltage on any pin:.....-2.0V to +4.5V**
Short Circuit Output Current: .....100mA†

*Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**All specified voltages are with respect to GND. Minimum DC voltage is -0.5V on input/output pins and -0.2V on V_{CC} and V_{PEN} pins. During transitions, this level may undershoot to -2.0V for periods <20ns. Maximum DC voltage on input/output pins, V_{CC}, and V_{PEN} is V_{CC} +0.5V which, during transitions, may overshoot to V_{CC} +2.0V for periods <20ns.

†Output shorted for no more than one second. No more than one output shorted at a time.

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Table 24: Temperature and Recommended DC Operating Conditions

Commercial temperature ($0^{\circ}C \le T_A \le +85^{\circ}C$); extended temperature ($-40^{\circ}C \le T_A \le +85^{\circ}C$)

PARAMATER	SYMBOL	MIN	MAX	UNITS	NOTES
V_{CC} Supply Voltage (2.7V–3.6V)	V_{CC}	2.7	3.6	V	
V_{CCQ} Supply Voltage (2.7V–3.6V)	V_{CCQ}	2.7	3.6	V	
Input and V_{PEN} Load Current V_{CC} = V_{CC} (Max); V_{CCQ} = V_{CCQ} (MAX) V_{IN} = V_{CCQ} or GND	I_{LI}		±1	µA	1
Output Leakage Current V_{CC} = V_{CC} (Max); V_{CCQ} = V_{CCQ} (MAX) V_{IN} = V_{CCQ} or GND	I_{LO}		±10	µA	1
Input Low Voltage	V_{IL}	-0.2	0.8	V	2
Input High Voltage	V_{IH}	2	V_{CCQ} + 0.5	V	2
Output Low Voltage (2.7V–3.6V) V_{CCQ} = V_{CCQ} (MIN) I_{OL} = 2mA	V_{OL}		0.4	V	2, 3
V_{CCQ} = V_{CCQ} (MIN) I_{OL} = 100µA			0.2	V	
Output High Voltage (2.7V–3.6V) V_{CCQ} = V_{CCQ} (MIN) I_{OH} = -2.5mA	V_{OH}	0.85 x V_{CCQ}		V	2
V_{CCQ} = V_{CCQ} (MIN) I_{OH} = -100µA		V_{CCQ} – 0.2		V	

NOTE:

1. All currents are in RMS unless otherwise noted. These currents are valid for all product versions (packages and speeds).
2. Sampled, not 100 percent tested.
3. Includes STS.

Table 25: Capacitance

T_A = +25ºC; f = 1MHz

PARAMETER/CONDITION			SYMBOL	TYP	MAX	UNITS
Input Capacitance			C	5	8	pF
Output Capacitance	BYTE#	32Mb and 64Mb	C_{OUT}	10	12	pF
		128Mb		14	16	pF
	All other pins		C_{OUT}	5	12	pF

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Table 26: Recommended DC Electrical Characteristics

Notes appear on page 47; commercial temperature (0ºC ≤ T_A ≤ +85ºC); extended temperature (-40ºC ≤ T_A ≤ +85ºC)

DESCRIPTION	CONDITIONS	SYM	DENSITY	TYP	MAX	UNITS	NOTES
V_{CC} Standby Current	CMOS Inputs; V_{CC} = V_{CC} (MAX); Device is enabled; RP# = V_{CCQ} ±0.2V	I_{CC1}	32Mb	75	120	µA	1, 2, 3
			64Mb	75			
			128Mb	50			
	TTL inputs; V_{CC} = V_{CC} (MAX): Device is enabled; RP# = V_{IH}		32Mb	100	2,000	µA	
			64Mb	100			
			128Mb	90			
V_{CC} Power-Down Current	RP# = GND ±0.2V; I_{OUT} (STS) = 0mA	I_{CC2}	32Mb	75	120	µA	
			64Mb	75			
			128Mb	50			
V_{CC} Page Mode Read Current	CMOS inputs; V_{CC} = V_{CC} (MAX); V_{CCQ} = V_{CCQ} (MAX) using standard 4-word page mode READs; Device is enabled; f = 5 MHz; I_{OUT} = 0mA	I_{CC3}	All	3	10	mA	1, 3
	CMOS inputs; V_{CC} = V_{CC} (MAX); V_{CCQ} = V_{CCQ} (MAX) using standard 4-word page mode READs; Device is enabled; f = 33 MHz; I_{OUT} = 0mA			8	15		
V_{CC} Asynchronous Mode Read Current	CMOS inputs; V_{CC} = V_{CC} (MAX); V_{CCQ} = V_{CCQ} (MAX) using standard word/byte single READs; Device is enabled; f = 5 MHz; I_{OUT} = 0mA	I_{CC4}	All	9	50	mA	1, 3
V_{CC} Program or Set Lock Bits Current	CMOS inputs, V_{PEN} = V_{CC}	I_{CC5}	32Mb	24	60	mA	1, 4
			64Mb	24	60		
			128Mb	17	60		
	TTL inputs, V_{PEN} = V_{CC}		32Mb	24	70		
			64Mb	24	70		
			128Mb	17	70		
V_{CC} Block Erase or Clear Block Lock Bits Current	CMOS inputs, V_{PEN} = V_{CC}	I_{CC6}	32Mb	26	70	mA	1, 4
			64Mb	26	70		
			128Mb	17	70		
	TTL inputs, V_{PEN} = V_{CC}		32Mb	26	80		
			64Mb	26	80		
			128Mb	17	80		
V_{CC} Program Suspend or Block Erase Suspend Current	Device is disabled	I_{CC7}	All		10	mA	1

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Table 26: Recommended DC Electrical Characteristics

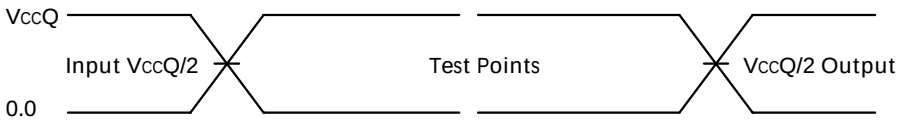
Notes appear on page 47; commercial temperature (0ºC ≤ T_A ≤ +85ºC); extended temperature (-40ºC ≤ T_A ≤ +85ºC)

DESCRIPTION	CONDITIONS	SYM	DENSITY	TYP	MAX	UNITS	NOTES
V_{PEN} Lockout during PROGRAM, ERASE, and LOCK BIT Operations		V_{PENLK}	All		1	V	5, 6, 7
V_{PEN} during BLOCK ERASE, PROGRAM, or LOCK BIT Operations		V_{PENH}	All		3.6	V	6, 7, 9
V_{CC} Lockout Voltage		V_{LKO}	All	2.2		V	8

NOTE:

1. All currents are in RMS unless otherwise noted. These currents are valid for all product versions (packages and speeds).
2. Includes STS.
3. CMOS inputs are either V_{CC} ±0.2V or V_{SS} ±0.2V. TTL inputs are either V_{IL} or V_{IH} with a minimum of -0.2V.
4. Sampled, not 100 percent tested.
5. I_{CCWS} and I_{CCES} are specified with the device deselected. If the device is read or written while in erase suspend mode, the device's current draw is I_{CCR} or I_{CCW}.
6. Block erase, programming, and lock bit configurations are inhibited when $V_{PEN} \leq V_{PENLK}$, and they are not guaranteed in the range between V_{PENLK} (MAX) and V_{PENH} (MIN), or above V_{PENH} (MAX).
7. Typically, V_{PEN} is connected to V_{CC}.
8. Block erase, programming, and lock bit configurations are inhibited when $V_{CC} < V_{LKO}$, and they are not guaranteed in the range between V_{LKO} (MIN) and V_{CC} (MIN), or above V_{CC} (MAX).
9. V_{PENH} (MIN) = 2.7V.

Figure 19: Transient Input/Output Reference Waveform for VccQ = 2.7V – 3.6V



NOTE:

AC test inputs are driven at VccQ for a logic 1 and 0.0V for a logic 0. Input timing begins, and output timing ends, at VccQ/2V (50 percent of VccQ). Input rise and fall times (10 percent to 90 percent) < 5ns.

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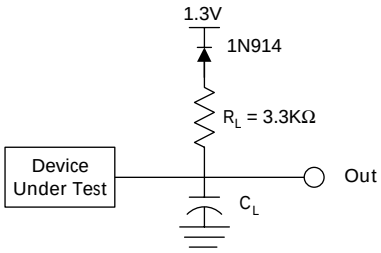
Figure 20: Transient Equivalent Test Load Circuit



NOTE:
C_L includes jig capacitance.

Table 27: Test Configuration Loading Value

TEST CONFIGURATION	C_L (pF)
VccQ = Vcc = 2.7V – 3.6V	30

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Table 28: AC Characteristics–Read-Only Operations

Notes: 1, 2, 4; commercial temperature (0ºC ≤ T_A ≤ +85ºC); extended temperature (-40ºC ≤ T_A ≤ +85ºC)

PARAMETER	SYMBOL	DENSITY	Vcc = 2.7V–3.6V VccQ = 2.7V–3.6V		UNITS	NOTES
			MIN	MAX		
Read/Write Cycle Time	^tRC	32Mb	110		ns	
		64Mb	120/115		ns	
		128Mb	150/120		ns	
Address to Output Delay	^tAA	32Mb		110	ns	
		64Mb		120/115	ns	
		128Mb		150/120	ns	
CEx to Output Delay	^tACE	32Mb		110	ns	
		64Mb		120/115	ns	
		128Mb		150/120	ns	
OE# to Non-Array Output Delay	^tAOE	All		50	ns	3, 5
OE# to Array Output Delay	^tAOA	All		25	ns	5
RP# High to Output Delay	^tRWH	32Mb		150	ns	
		64Mb		180	ns	
		128Mb		210	ns	
CEx to Output in Low-Z	^tOEC	All	0		ns	6
OE# to Output in Low-Z	^tOEO	All	0		ns	6
CEx HIGH to Output in High-Z	^tODC	All		35	ns	6
OE# HIGH to Output in High-Z	^tODO	All		15	ns	6
Output Hold from Address, CEx, or OE# Change, whichever occurs first	^tOH	All	0		ns	6
CEx LOW to BYTE# HIGH or LOW	^tCB	All		10	ns	6
BYTE# to Output Delay	^tABY	All		1,000	ns	
BYTE# to Output in High-Z	^tODB	All		1,000	ns	6
CEx HIGH to CEx LOW	^tCWH	All	0		ns	6
Page Address Access Time	^tAPA	All		25	ns	6

NOTE:

1. CEx LOW is defined as the first edge of CE0, CE1, or CE2 that enables the device. CEx HIGH is defined at the first edge of CE0, CE1, or CE2 that disables the device (see Table 4).
2. See AC Input/Output Reference Waveforms for the maximum allowable input slew rate.
3. OE# may be delayed up to ^tACE–^tAOE after the first edge of CEx that enables the device (see Table 4) without impact on ^tACE .
4. See Figure 19 on page 47, Transient Input/Output Reference Waveform, for VccQ = 2.7V – 3.6V, and Figure 20 on page 48, Transient Equivalent Testing Load Circuit, for testing characteristics.
5. When reading the Flash array, a faster ^tAOE applies. Non-array READs refer to status register READs, QUERY READs, or DEVICE IDENTIFIER READs.
6. Sampled, not 100 percent tested.

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Figure 21: Page Mode and Standard Word/Byte READ Operations

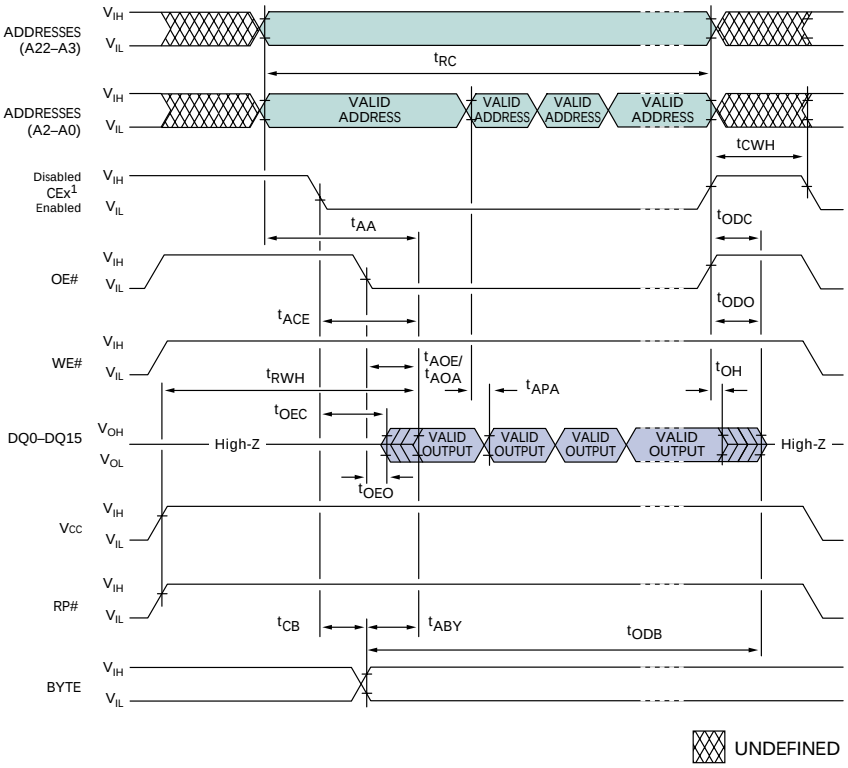

Table 29: Timing Parameters

SYMBOL	Vcc = 2.7V–3.6V VccQ = 2.7V–3.6V MIN	MAX	UNITS
tRC (32Mb)	110		ns
tRC (64Mb)	120/115		ns
tRC (128Mb)	150/120		ns
tAA (32Mb)		110	ns
tAA (64Mb)		120/115	ns
tAA (128Mb)		150/120	ns
tACE (32Mb)		110	ns
tACE (64Mb)		120/115	ns
tACE (128Mb)		150/120	ns
tAOE		50	ns
tAOA		25	ns
tRWH (32Mb)		150	ns

SYMBOL	Vcc = 2.7V–3.6V VccQ = 2.7V–3.6V MIN	MAX	UNITS
tRWH (64Mb)		180	ns
tRWH (128Mb)		210	ns
tOEC	0		ns
tOEO	0		ns
tODC		35	ns
tODO		15	ns
tOH	0		ns
tCB		10	ns
tABY		1,000	ns
tODB		1,000	ns
tCWH	0		ns
tAPA		25	ns

NOTE:
1. CEx LOW is defined as the first edge of CE0, CE1, or CE2 that enables the device. CEx HIGH is defined as the first edge of CE0, CE1, or CE2 that disables the device.

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Table 30: AC Characteristics—WRITE Operations

Notes: 1, 2, 3; commercial temperature (0ºC ≤ T_A ≤ +85ºC), extended temperature (-40ºC ≤ T_A ≤ +85ºC)

PARAMETER	SYMBOL	32Mb, 64Mb, 128Mb		UNITS	NOTES
		MIN	MAX		
RP# High Recovery to WE# (CEx) Going LOW	^tRS	1		µs	4
CEx (WE#) LOW to WE# (CEx) Going LOW	^tCS (^tWS)	0		ns	5
Write Pulse Width	^tWP (^tCP)	70		ns	5
Data Setup to WE# (CEx) Going HIGH	^tDS	50		ns	6
Address Setup to WE# (CEx) Going HIGH	^tAS	55		ns	6
CEx (WE#) Hold from WE# (CEx) HIGH	^tCH (^tWH)	0		ns	
Data Hold from WE# (CEx) HIGH	^tDH	0		ns	
Address Hold from WE# (CEx) HIGH	^tAH	0		ns	
Write Pulse Width HIGH	^tWPH (^tCPH)	30		ns	7
V_{PEN} Setup to WE# (CEx) Going HIGH	^tVPS	0		ns	4
Write Recovery Before Read	^tWR	35		ns	8
WE# (CEx) HIGH to STS Going LOW	^tSTS		200	ns	9
V_{PEN} Hold from Valid SRD, STS Going HIGH	^tVPH	0		ns	4, 9, 10
WE# (CEx) HIGH to Status Register Busy	^tWB		200	ns	4

NOTE:

1. CEx LOW is defined as the first edge of CE0, CE1, or CE2 that enables the device. CEx HIGH is defined as the first edge of CE0, CE1, or CE2 that disables the device.
2. Read timing characteristics during BLOCK ERASE, PROGRAM, and LOCK BIT CONFIGURATION operations are the same as during read-only operations. Refer to AC Characteristics – Read-Only Operations.
3. A WRITE operation can be initiated and terminated with either CEX or WE#.
4. Sampled, not 100 percent tested.
5. Write pulse width (^tWP) is defined from CEx or WE# going LOW (whichever goes LOW last) to CEx or WE# going HIGH (whichever goes HIGH first).
6. Refer to Table 6 on page 17 for valid A_{IN} and D_{IN} for block erase, program, or lock bit configuration.
7. Write pulse width high (^tWPH) is defined from CEx or WE# going HIGH (whichever goes HIGH first) to CEx or WE# going LOW (whichever goes LOW first).
8. For array access, ^tAA is required in addition to ^tWR for any accesses after a WRITE.
9. STS timings are based on STS configured in its RY/BY# default mode.
10. V_{PEN} should be held at V_{PENH} until determination of block erase, program, or lock bit configuration success (SR1/3/4/5 = 0).

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Table 31: Block Erase, Program and Lock Bit Configuration Performance

Notes: 1, 2, 3; commercial temperature ($0^{o}c \le t_A \le +85^{o}c$), extended temperature ($-40^{o}C \le T_A \le +85^{o}C$)

PARAMETER	SYM	32Mb 64Mb		128Mb		UNITS	NOTES
		TYP	MAX[8]	TYP	MAX[8]		
Write Buffer Byte Program Time (Time to Program 32 bytes/16 words)	$^{t}WED1$	200	654	180	654	µs	4, 5, 6, 7
Byte/Word Program Time (Using WORD/BYTE PROGRAM Command)	$^{t}WED2$	12.5	630	11.2	630	µs	4
Block Program Time (Using WRITE-to-BUFFER Command)	$^{t}WED3$	0.8	1.7	0.7	1.7	sec	4
Block Erase Time	$^{t}WED4$	0.75	5	0.75	5	sec	4
Set Lock Bits Time	$^{t}WED5$	14	75	10	75	µs	4
Clear Block Lock Bits Time	$^{t}WED6$	0.5	0.7	0.5	0.7	sec	5
Program Suspend Latency Time to Read	^{t}LPS	25	30	25	30	µs	
Erase Suspend Latency Time to Read	^{t}LES	26	35	25	35	µs	

NOTE:

1. Typical values measured at $T_A = +25^{o}C$ and nominal voltages. Assumes corresponding lock bits are not set. Subject to change based on device characterization.
2. These performance numbers are valid for all speed versions.
3. Sampled, but not 100 percent tested.
4. Excludes system-level overhead.
5. These values are valid when the buffer is full, and the start address is aligned on a 32-byte boundary.
6. Effective per-byte program time is 5.6µs/byte (typical).
7. Effective per-word program time is 11.2µs/word (typical).
8. MAX values are measured at worst-case temperature and V_{CC} corner after 100,000 cycles.

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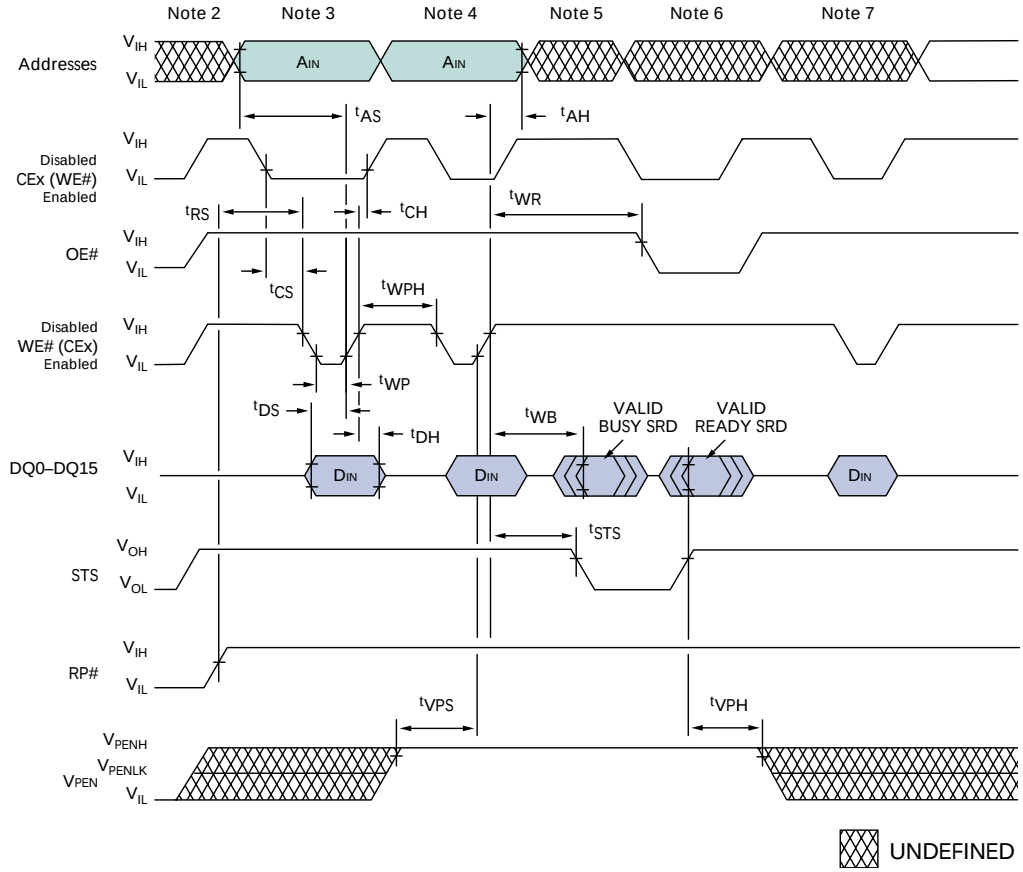
Figure 22: WRITE Operations



Timing Parameters

SYMBOL	32Mb/64Mb/128Mb MIN	32Mb/64Mb/128Mb MAX	UNITS
t_{RS}	1		µs
t_{CS}	0		ns
t_{WP}	70		ns
t_{DS}	50		ns
t_{AS}	55		ns
t_{CH}	0		ns
t_{DH}	0		ns

SYMBOL	32Mb/64Mb/128Mb MIN	32Mb/64Mb/128Mb MAX	UNITS
t_{AH}	0		ns
t_{WPH}	30		ns
t_{VPS}	0		ns
t_{WR}	35		ns
t_{STS}		200	ns
t_{VPH}	0		ns
t_{WB}		200	ns

NOTE:

1. CEx low is defined as the first edge of CE0, CE1, or CE2 that enables the device. CEx high is defined at the first edge of CE0, CE1, or CE2 that disables the device (see Table 4 on page 14). STS is shown in its default mode (RY/BY#).
2. VCC power-up and standby.
3. Write block erase, write buffer, or program setup.
4. Write block erase or write buffer confirm, or valid address and data.
5. Automated erase delay.
6. Read status register or query data.
7. WRITE READ ARRAY command.

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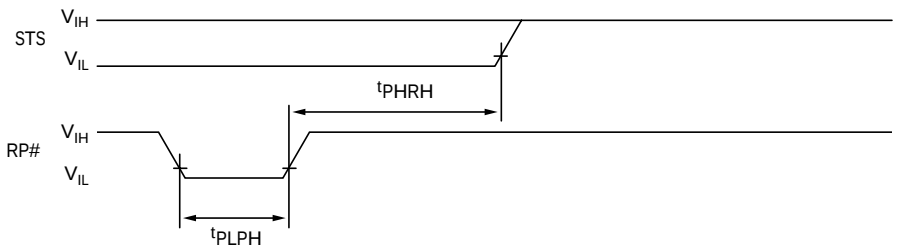
Table 32: RESET Specifications

Note 1; commercial temperature (0ºC ≤ T_A ≤ +85ºC), extended temperature (-40ºC ≤ T_A ≤ +85ºC)

PARAMETER	SYMBOL	32Mb/64Mb/128Mb		UNITS	NOTES
		MIN	MAX		
RP# Pulse Low Time (If RP# is tied to VCC, this specification is not applicable)	^tPLPH	35		µs	2
RP# High to Reset during Block Erase, Program, or Lock Bit Configuration	^tPHRH		100	ns	3

Figure 23: RESET Operation[4]



NOTE:

1. STS is shown in its default mode (RY/BY#).
2. These specifications are valid for all product versions (packages and speeds).
3. If RP# is asserted while a BLOCK ERASE, PROGRAM, or LOCK BIT CONFIGURATION operation is not executing, then the minimum required RP# pulse LOW time is 100ns.
4. A reset time, ^tRWH, is required from the latter of STS (in RY/BY# mode) or RP# going HIGH until outputs are valid.

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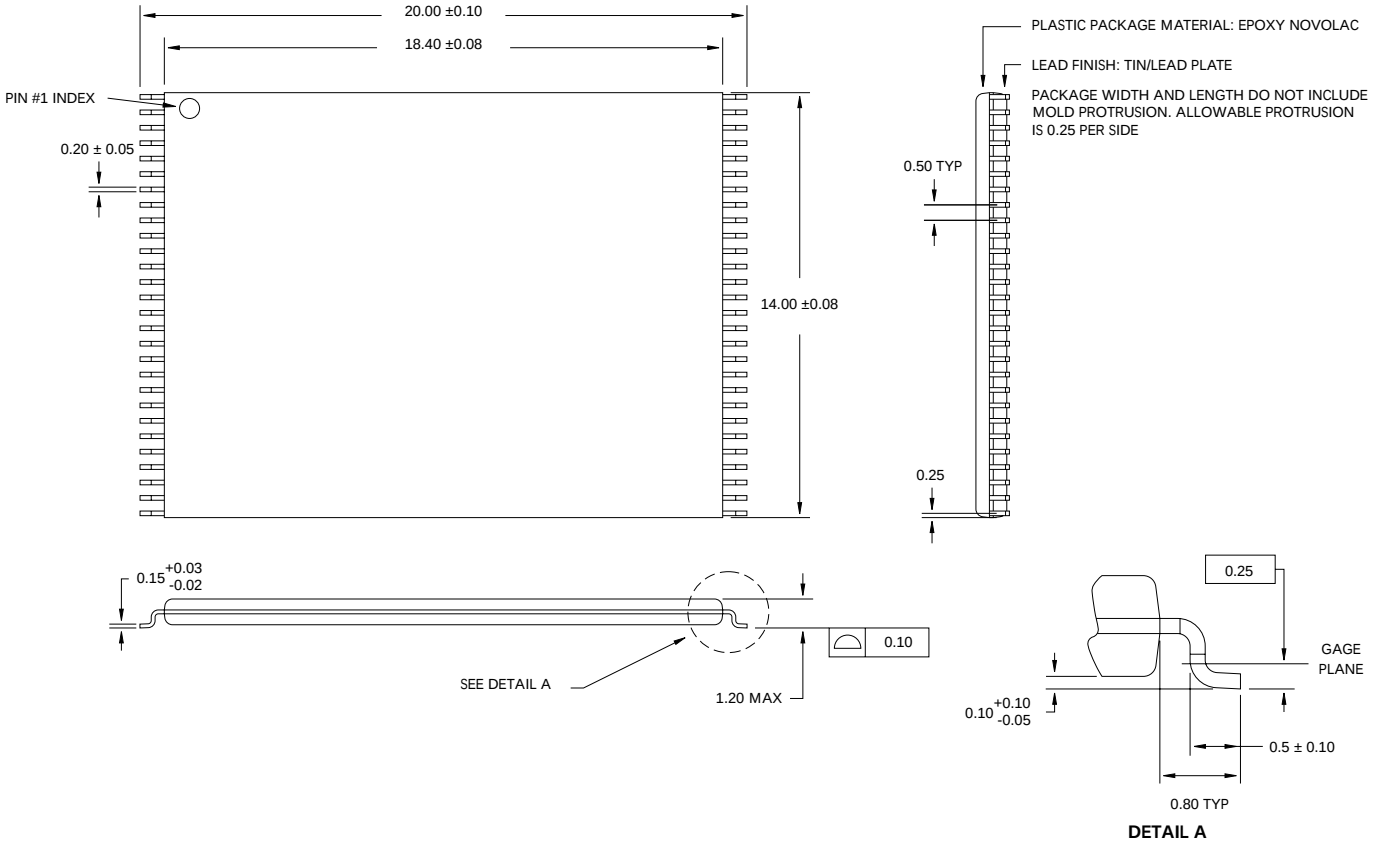
Figure 24: 56-Pin TSOP Type 1



NOTE:

1. All dimensions in millimeters.
2. Package width and length do not include mold protrusion; allowable mold protrusion is 0.25mm per side.

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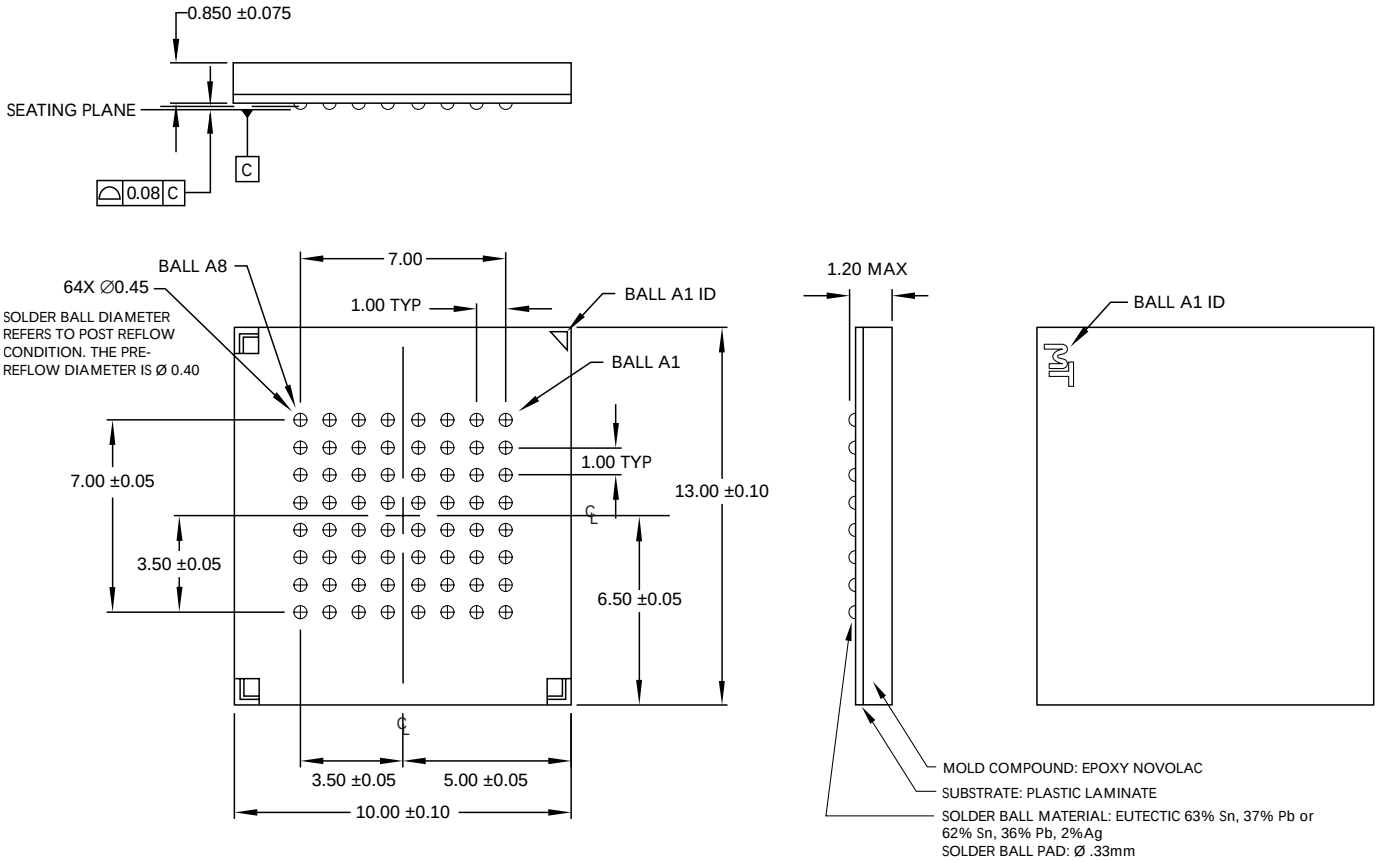
Figure 25: 64-Ball FBGA



NOTE:

All dimensions in millimeters.

Data Sheet Designation

No Marking: This data sheet contains minimum and maximum limits specified over the complete power supply and temperature range for production devices. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.

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Revision History

Rev. I 6/03
- Removed PRELIMINARY designation from the MT28F128J3
- Removed “F” option

Rev. H 5/03
- Addition of speed grades: -115 (64Mb) and -12 (128Mb)
- Addition of optional Micron ManID (0x2Ch)
- Updated $I_{CC}1$, $I_{CC}2$, $I_{CC}3$, $I_{CC}4$, $I_{CC}5$, and $I_{CC}6$ currents
- Update to Capacitance table and WRITE Operations table
- Removal of RESUME Operations timing diagram
- Clarification of address decode on Identifier Code Space
- Updated 56-pin TSOP I package drawing
- Changed CFI Table address 36h to 6Ch

Rev. 7 ..... 11/02
- Removed PRELIMINARY designation from the MT28F320J3
- Fixed a typographical error on the 64-ball FBGA package drawing

Rev. 6 ..... 8/02
- Updated commercial temperature range
- Updated Configuration Coding Definitions table
- Removed 3.0V–3.6V VccQ voltage range option
- Updated V_{LKO}, V_{PENLK}, ^{t}AOA, ^{t}ODC, ^{t}APA, ^{t}CH (^{t}WH), ^{t}STS, and ^{t}WB
- Added RESUME Operations timing diagram

Rev. 5 ..... 3/03
- Updated MT28F320J3 information

Rev. 4 ..... 2/02
- Added $V_{CC}Q$ = 4.5V–5.5V parameter for 32Mb and 64Mb devices
- Updated erase and program timing parameters
- Removed Block Erase Status bit

Rev. 3 ..... 6/01
- Updated package drawing and corresponding notes

Rev. 2 ..... 5/01
- Added 128Mb device information
- Added 64-ball FBGA (1.0mm pitch) package

Original document, Rev. 1, Advance 12/00

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