FAIRCHILD
SEMICONDUCTOR®

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74VHC240
Octal Buffer/Line Driver with 3-STATE Outputs

General Description

The VHC240 is an advanced high speed CMOS octal bus buffer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. The VHC240 is an inverting 3-STATE buffer having two active-LOW output enables. This device is designed to drive buslines or buffer memory address registers.

An input protection circuit ensures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery backup. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

- High Speed: t_{PD} = 3.6ns (typ) at T_A = 25°C
- Low power dissipation: I_{CC} = 4 μA (max) @ T_A = 25°C
- High noise immunity: V_{NIH} = V_{NIL} = 28% V_{CC} (min)
- Power down protection is provided on all inputs
- Low noise: V_{OLP} = 0.9V (max)
- Pin and function compatible with 74HC240

Ordering Code:

Order Number	Package Number	Package Description
74VHC240M	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74VHC240SJ	M20D	Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74VHC240MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74VHC240N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.
Pb-Free package per JEDEC J-STD-020B.

Logic Symbol
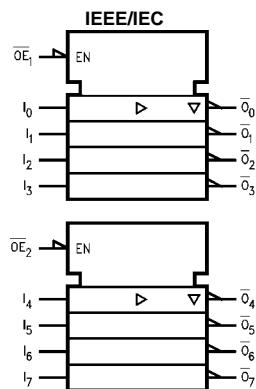
Connection Diagram

www.fairchildsemi.com
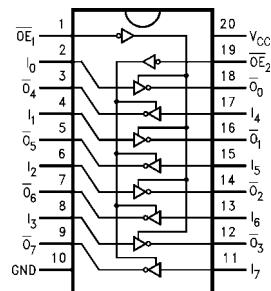
Pin Descriptions

Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	3-STATE Output Enable Inputs
I_0–I_7	Inputs
$\overline{O}_0$–$\overline{O}_7$	Outputs 3-STATE Outputs

Truth Tables

Inputs		Outputs
$\overline{OE}_1$	I_n	(Pins 12, 14, 16, 18)
L	L	H
L	H	L
H	X	Z

Inputs		Outputs
$\overline{OE}_1$	I_n	(Pins 3, 5, 7, 9)
L	L	H
L	H	L
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−0.5V to +7.0V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} + 0.5V
Input Diode Current (I_{IK})	−20 mA
Output Diode Current (I_{OK})	±20 mA
DC Output Current (I_{OUT})	±25 mA
DC V_{CC}/GND Current (I_{CC})	±75 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

Supply Voltage (V_{CC})	2.0V to 5.5V
Input Voltage (V_{IN})	0V to +5.5V
Output Voltage (V_{OUT})	0V to V_{CC}
Operating Temperature (T_{OPR})	−40°C to +85°C
Input Rise and Fall Time (t_r, t_f)	
V_{CC} = 3.3V ± 0.3V	0 ns/V ~ 100 ns/V
V_{CC} = 5.0V ± 0.5V	0 ns/V ~ 20 ns/V

Note 1: Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside databook specifications.

Note 2: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	T_A = −40°C to +85°C Min	T_A = −40°C to +85°C Max	Units	Conditions	
V_{IH}	HIGH Level	2.0	1.50			1.50		V		
	Input Voltage	3.0 − 5.5	0.7 V_{CC}			0.7 V_{CC}				
V_{IL}	LOW Level	2.0			0.50		0.50	V		
	Input Voltage	3.0 − 5.5			0.3 V_{CC}		0.3 V_{CC}			
V_{OH}	HIGH Level	2.0	1.9	2.0		1.9		V	$V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = −50 μA
	Output Voltage	3.0	2.9	3.0		2.9				
		4.5	4.4	4.5		4.4				
		3.0	2.58			2.48		V		I_{OH} = −4 mA
		4.5	3.94			3.80				I_{OH} = −8 mA
V_{OL}	LOW Level Output	2.0		0.0	0.1		0.1		$V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 50 μA
	Voltage	3.0		0.0	0.1		0.1	V		
		4.5		0.0	0.1		0.1			
		3.0			0.36		0.44	V		I_{OL} = 4 mA
		4.5			0.36		0.44			I_{OL} = 8 mA
I_{OZ}	3-STATE Output	5.5			±0.25		±2.5	μA	$V_{IN} = V_{IH}$ or V_{IL}	
	Off-State Current								$V_{OUT} = V_{CC}$ or GND	
I_{IN}	Input Leakage Current	0 − 5.5			±0.1		±1.0	μA	V_{IN} = 5.5V or GND	
I_{CC}	Quiescent Supply Current	5.5			4.0		40.0	μA	$V_{IN} = V_{CC}$ or GND	

Noise Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = 25°C Typ	T_A = 25°C Limits	Units	Conditions
V_{OLP} (Note 3)	Quiet Output Maximum Dynamic V_{OL}	5.0	0.6	0.9	V	C_L = 50 pF
V_{OLV} (Note 3)	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.6	−0.9	V	C_L = 50 pF
V_{IHD} (Note 3)	Minimum HIGH Level Dynamic Input Voltage	5.0		3.5	V	C_L = 50 pF
V_{ILD} (Note 3)	Maximum LOW Level Dynamic Input Voltage	5.0		1.5	V	C_L = 50 pF

Note 3: Parameter guaranteed by design.

AC Electrical Characteristics

Symbol	Parameter	V$_{CC}$ (V)	T$_A$ = 25°C			T$_A$ = −40°C to +85°C		Units	Conditions	
			Min	Typ	Max	Min	Max			
t$_{PLH}$ t$_{PHL}$	Propagation Delay Time	3.3 ± 0.3		5.3	7.5	1.0	9.0	ns		C$_L$ = 15 pF
				7.8	11.0	1.0	12.5			C$_L$ = 50 pF
		5.0 ± 0.5		3.6	5.5	1.0	6.5	ns		C$_L$ = 15 pF
				5.1	7.5	1.0	8.5			C$_L$ = 50 pF
t$_{PZL}$ t$_{PZH}$	3-STATE Output Enable Time	3.3 ± 0.3		6.6	10.6	1.0	12.5	ns	R$_L$ = 1 kΩ	C$_L$ = 15 pF
				9.1	14.1	1.0	16.0			C$_L$ = 50 pF
		5.0 ± 0.5		4.7	7.3	1.0	8.5	ns		C$_L$ = 15 pF
				6.2	9.3	1.0	10.5			C$_L$ = 50 pF
t$_{PLZ}$ t$_{PHZ}$	3-STATE Output Disable Time	3.3 ± 0.3		10.3	14.0	1.0	16.0	ns	R$_L$ = 1 kΩ	C$_L$ = 50 pF
		5.0 ± 0.5	6.7		9.2	1.0	10.5			C$_L$ = 50 pF
t$_{OSLH}$ t$_{OSHL}$	Output to Output Skew	3.3 ± 0.3			1.5		1.5	ns	(Note 4)	C$_L$ = 50 pF
		5.0 ± 0.5			1.0		1.0			C$_L$ = 50 pF
C$_{IN}$	Input Capacitance			4	10		10	pF	V$_{CC}$ = Open	
C$_{OUT}$	Output Capacitance			6				pF	V$_{CC}$ = 5.0V	
C$_{PD}$	Power Dissipation Capacitance			17				pF	(Note 5)	

Note 4: Parameter guaranteed by design. t$_{OSLH}$ = |t$_{PLHmax}$ − t$_{PLHmin}$|; t$_{OSHL}$ = |t$_{PHLmax}$ − t$_{PHLmin}$|

Note 5: C$_{PD}$ is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I$_{CC}$ (opr.) = C$_{PD}$ * V$_{CC}$ * f$_{IN}$ + I$_{CC}$/8 (per bit).

Physical Dimensions inches (millimeters) unless otherwise noted
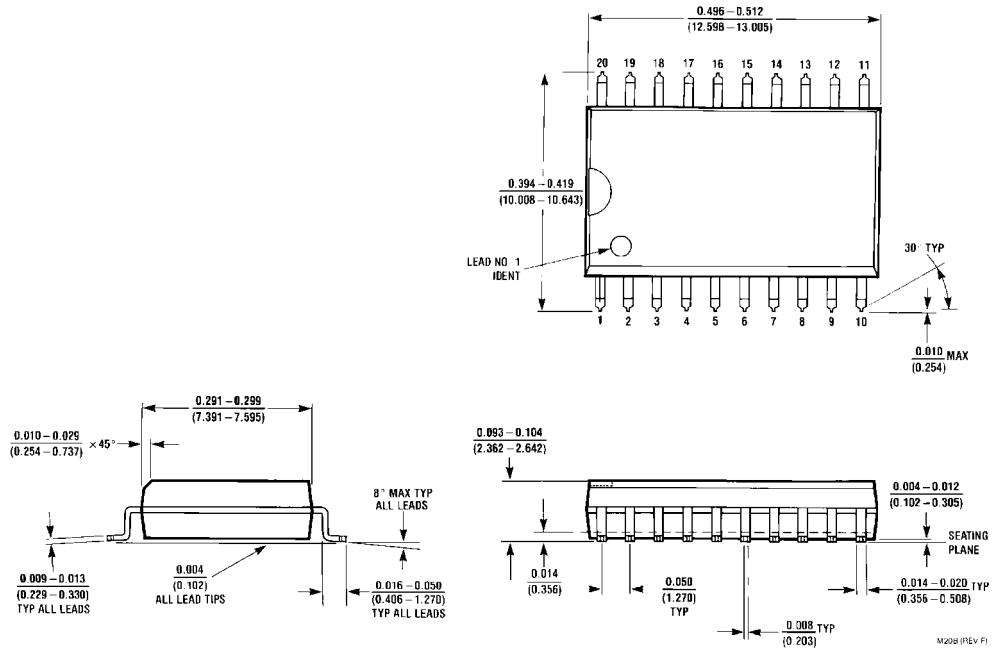
20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

12.6±0.10
-A-

0.40 TYP

20   11

7.8

3.9

5.3±0.10
-B-

PIN #1 IDENT.   1   10

△ 0.2 C B A
ALL LEAD TIPS

20 19   12 11

5.01 TYP

9.27 TYP

(2.13 TYP)

1   2   9 10

1.27 TYP   0.6 TYP

LAND PATTERN RECOMMENDATION

ALL LEAD TIPS
△ 0.1 C

2.1 MAX.

1.8±0.1

-C-

0.15±0.05

1.27 TYP   0.35-0.51

⊕ 0.12 Ⓜ C A
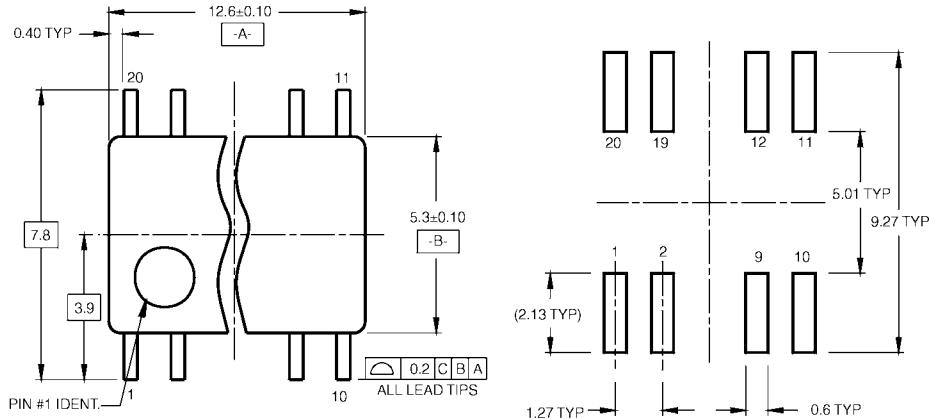
DIMENSIONS ARE IN MILLIMETERS
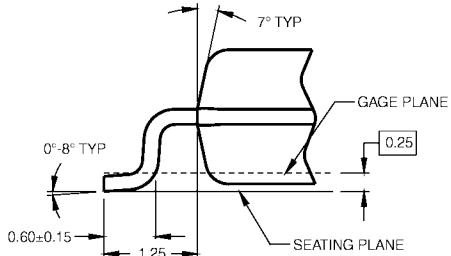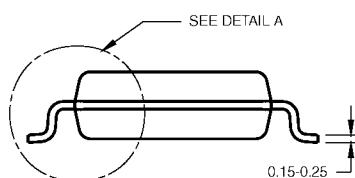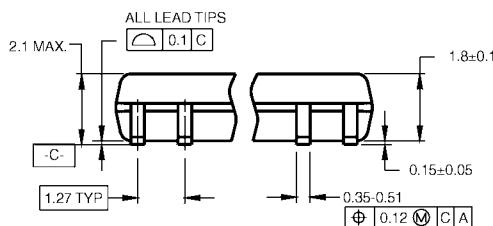
NOTES:
A. CONFORMS TO EIAJ EDR-7320 REGISTRATION,
   ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD
   FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

SEE DETAIL A

0.15-0.25

7° TYP

GAGE PLANE

0°-8° TYP

0.25

0.60±0.15

1.25

SEATING PLANE

DETAIL A

Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

6.5±0.1
-A-
-0.20
20
11
-C-
4.4±0.1 -B-
6.4
3.2
1
10
PIN #1 IDENT.
0.2 C B A
ALL LEAD TIPS

4.16   7.72
1.78
0.42
0.65
LAND PATTERN RECOMMENDATION

0.1 C
ALL LEAD TIPS
0.90 +0.15 -0.10
1.2 max
0.1±0.05
-C-
0.65
0.19-0.30
0.10 M A B S C S
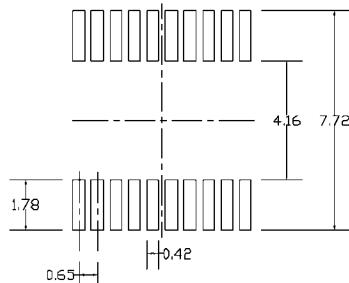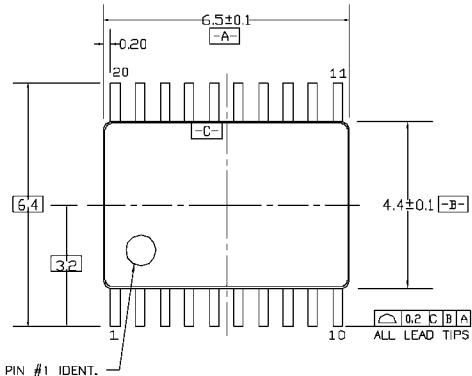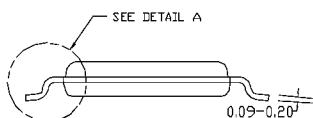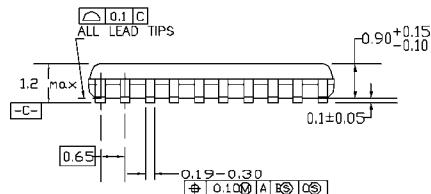
DIMENSIONS ARE IN MILLIMETERS

NOTES:

  A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.

  B. DIMENSIONS ARE IN MILLIMETERS.

  C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.

  D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

SEE DETAIL A
0.09-0.20
12.00°
R0.09min
GAGE PLANE
0 - 8°
0.25
SEATING PLANE
0.6±0.1
R0.09min
1.00
DETAIL A
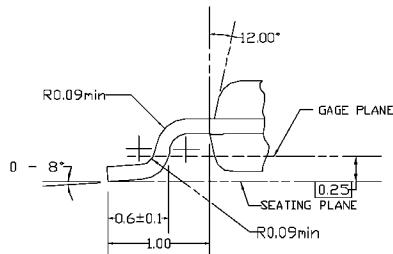
MTC20REV D1

20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC20

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)
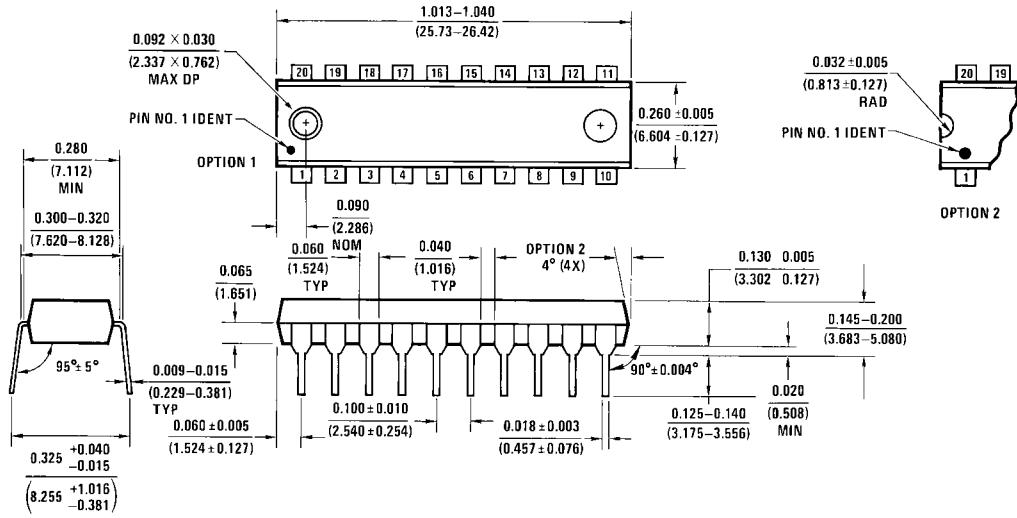
20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N20A

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