FAIRCHILD SEMICONDUCTOR®

February 2006

FDMS2572

N-Channel UltraFET Trench® MOSFET

150V, 4.5A, 47mΩ

General Description

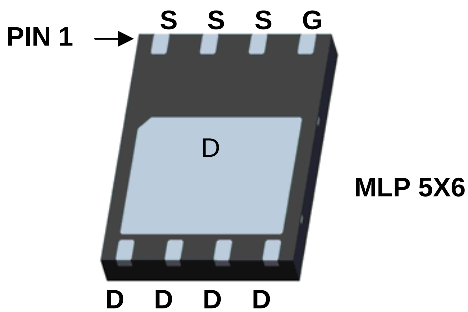
UltraFET devices combine characteristics that enable benchmark efficiency in power conversion applications. Optimized for low $r_{DS(on)}$, low ESR, low total and Miller gate charge, these devices are ideal for high frequency DC to DC converters.

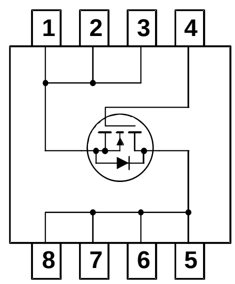
Applications

- Distributed Power Architectures and VRMs
- Primary Switch for 24V and 48V Systems
- High Voltage Synchronous Rectifier

Features

- Max $r_{DS(on)}$ = 47mΩ at V_{GS} = 10V, I_D = 4.5A
- Typ Qg = 31nC at V_{GS} = 10 V
- Low Miller Charge
- Optimized efficiency at high frequencies





Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DS}	Drain-Source Voltage		150	V
V_{GS}	Gate-Source Voltage		±20	V
I_D	Drain Current – Continuous	(Note 1a)	4.5	A
	– Pulsed		30	
P_D	Power Dissipation for Single Operation	(Note 1a)	2.8	W
		(Note 1b)	1.1	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		–55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	44	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1b)	115	

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDMS2572	FDMS2572	7''	12mm	3000 units

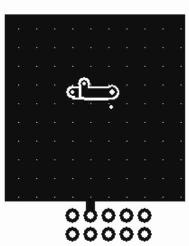
Electrical Characteristics

T_A = 25°C unless otherwise noted

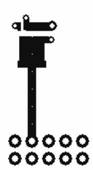
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Drain-Source Avalanche Ratings (Note 1)						
W_{DSS}	Single Pulse Drain-Source Avalanche Energy	V_{DD} = 75 V, I_D = 15 A, L=1mH			112	mJ
I_{AR}	Drain-Source Avalanche Current				15	A
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	150			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C		180		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 120 V, V_{GS} = 0 V			1	μA
I_{GSS}	Gate–Body Leakage	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	2	3.0	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C		–9.8		mV/°C
$r_{DS(on)}$	Static Drain–Source On–Resistance	V_{GS} = 10 V, I_D = 4.5 A V_{GS} = 6 V, I_D = 4.5 A V_{GS} = 10 V, I_D = 4.5 A, T_J = 125°C		36 39 69	47 53 103	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D =4.5 A		14		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 75 V, V_{GS} = 0 V, f = 1.0 MHz		1960		pF
C_{oss}	Output Capacitance			130		pF
C_{rss}	Reverse Transfer Capacitance			30		pF
R_G	Gate Resistance	f = 1.0 MHz		1.3		Ω
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = 75 V, I_D = 1 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		11	20	ns
t_r	Turn–On Rise Time			8	16	ns
$t_{d(off)}$	Turn–Off Delay Time			38	61	ns
t_f	Turn–Off Fall Time			31	50	ns
Q_g	Total Gate Charge	V_{DS} = 75 V, I_D = 4.5 A, V_{GS} = 10 V		31	43	nC
Q_{gs}	Gate–Source Charge			9		nC
Q_{gd}	Gate–Drain Charge			7		nC
Drain–Source Diode Characteristics						
V_{SD}	Drain–Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 2.2 A (Note 2)		0.7	1.0	V
t_{rr}	Diode Reverse Recovery Time	I_F = 4.5 A, d_{iF}/d_t = 100 A/µs		67		nS
Q_{rr}	Diode Reverse Recovery Charge			130		nC

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 44°C/W when mounted on a 1in^2 pad of 2 oz copper



b) 115 °C/W when mounted on a minimum pad of 2 oz copper
Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

Typical Characteristics

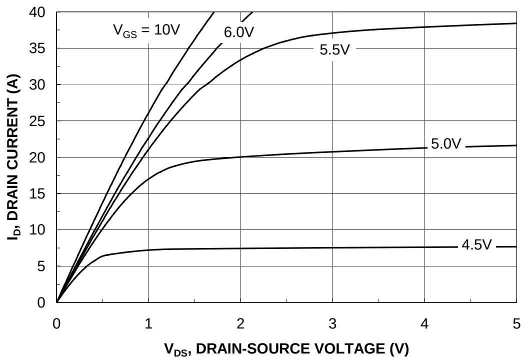


Figure 1. On-Region Characteristics.

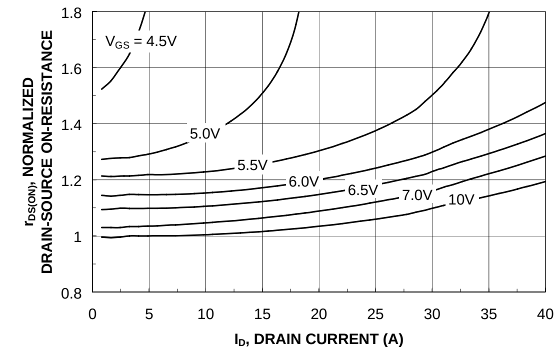


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

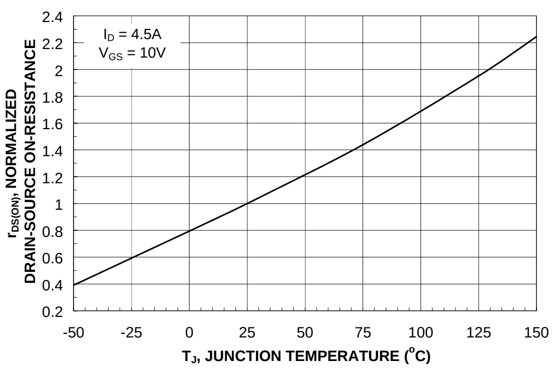


Figure 3. On-Resistance Variation with Temperature.

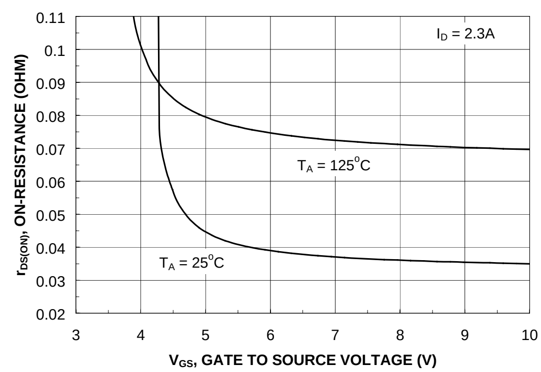


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

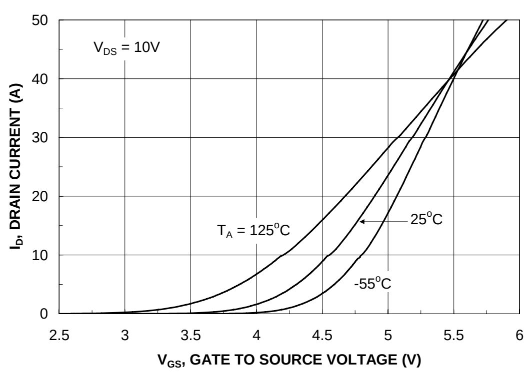


Figure 5. Transfer Characteristics.

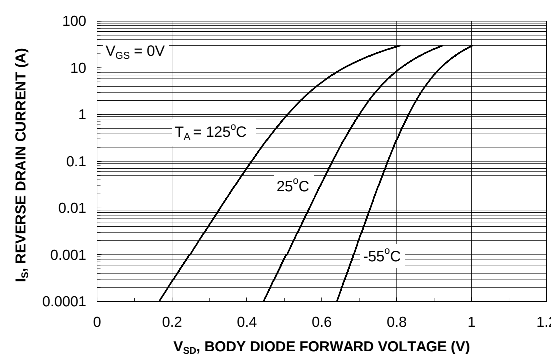


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

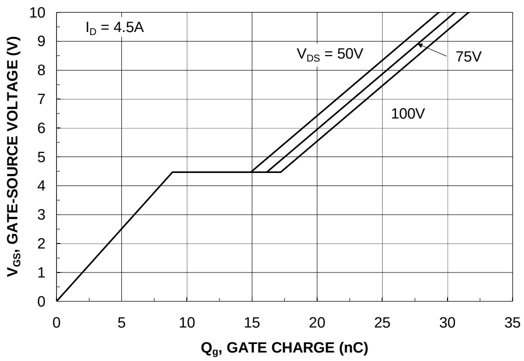


Figure 7. Gate Charge Characteristics.

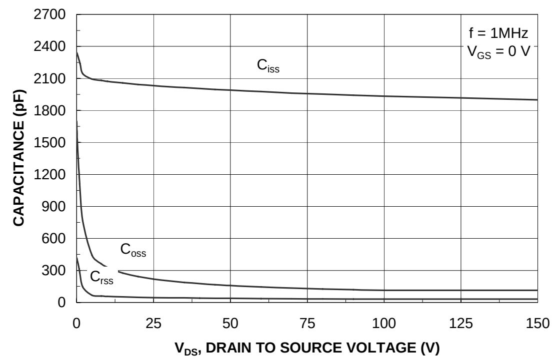


Figure 8. Capacitance Characteristics.

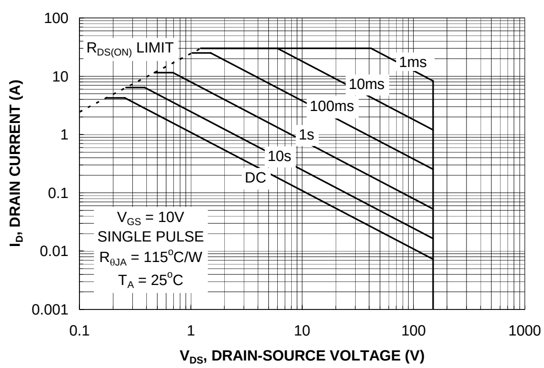


Figure 9. Maximum Safe Operating Area.

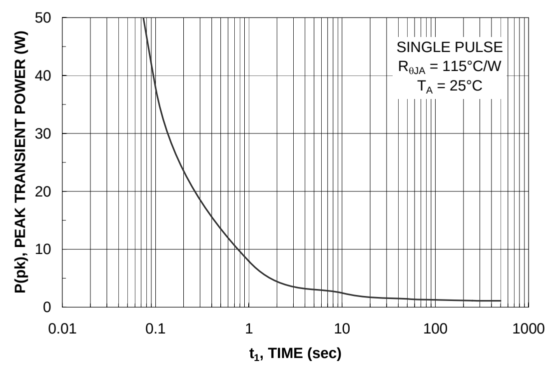


Figure 10. Single Pulse Maximum Power Dissipation.

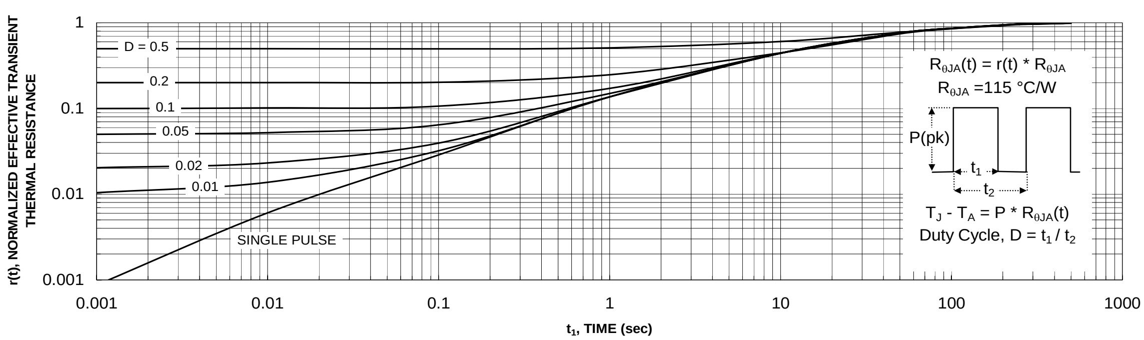
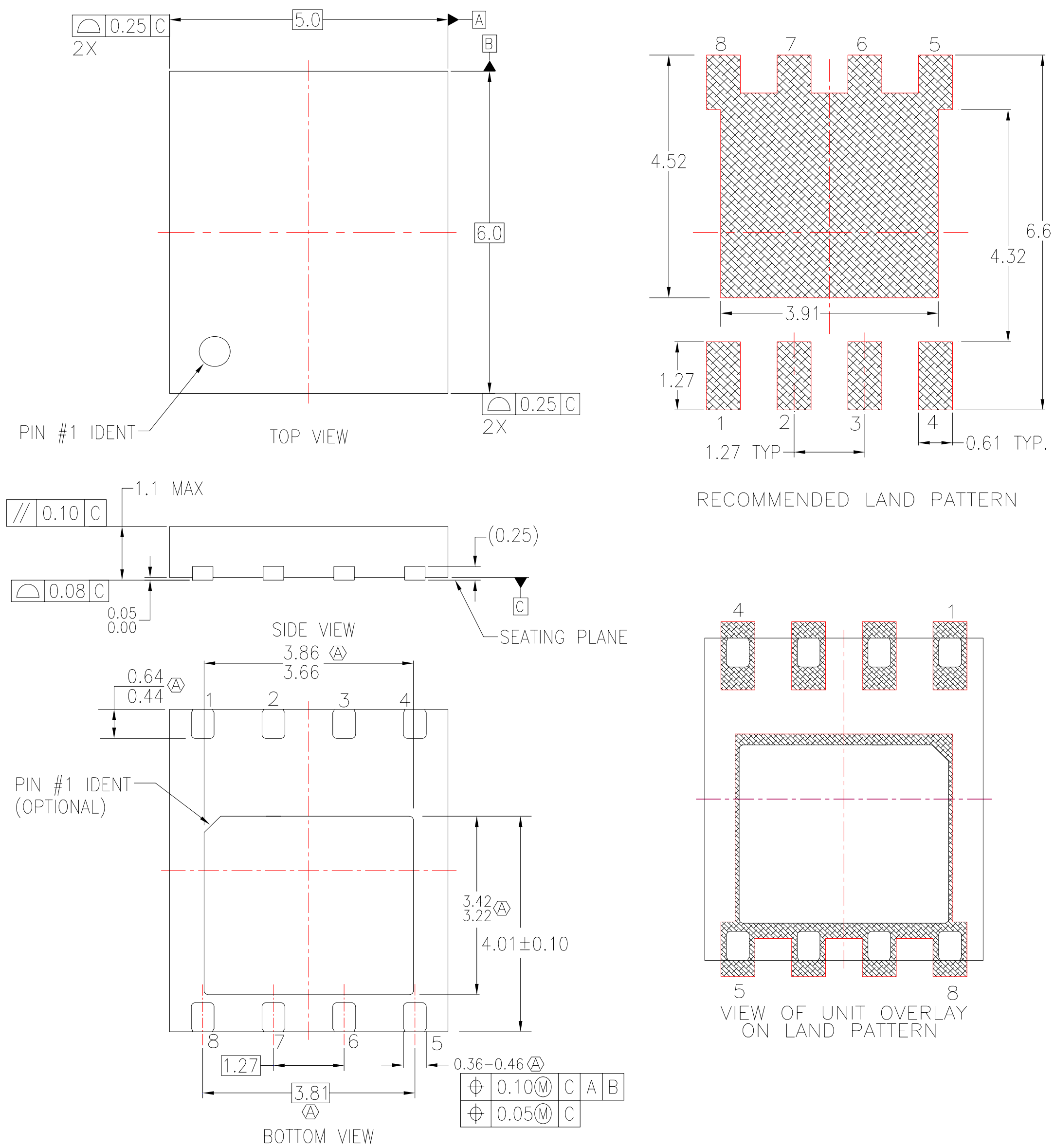


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

Dimensional Outline and Pad Lay-out



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