

# STS4DPF30L

## DUAL P-CHANNEL 30V - 0.07 Ω - 4A SO-8 STripFET<sup>™</sup> POWER MOSFET

PRELIMINARY DATA

ТҮРЕ	V <sub>DSS</sub>	R <sub>DS(on)</sub>	ID
STS4DPF30L	30 V	<0.08 Ω	4 A

- TYPICAL R<sub>DS</sub>(on) = 0.07 Ω
- STANDARD OUTLINE FOR EASY AUTOMATED SURFACE MOUNT ASSEMBLY
- LOW THRESHOLD DRIVE

#### DESCRIPTION

This Power MOSFET is the latest development of STMicroelectronis unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low onresistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

#### **APPLICATIONS**

- BATTERY MANAGEMENT IN NOMADIC EQUIPMENT
- POWER MANAGEMENT IN CELLULAR PHONES
- DC-DC CONVERTER



#### **INTERNAL SCHEMATIC DIAGRAM**



#### **ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	30	V
Vdgr	Drain-gate Voltage ( $R_{GS}$ = 20 k $\Omega$ )	30	V
V <sub>GS</sub>	Gate- source Voltage	± 16	V
I <sub>D</sub>	Drain Current (continuous) at $T_C = 25^{\circ}C$ Single Ope Drain Current (continuous) at $T_C = 100^{\circ}C$ Single Op		A A
I <sub>DM</sub> (●)	Drain Current (pulsed)	16	A
P <sub>tot</sub>	Total Dissipation at $T_C = 25^{\circ}C$ Dual Operation Total Dissipation at $T_C = 25^{\circ}C$ Single Operation	2.0 1.6	W W
) Pulse wid		te: For the P-CHANNEL MOSFET actual pol	larity of voltages a

current has to be reversed

April 2002

This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

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#### THERMAL DATA

Rthj-amb	(*)Thermal Resistance Junction-ambient	Single Operation	78	°C/W
		Dual Operating	62.5	°C/W
Tj	Thermal Operating Junction-ambient		-55 to150	°C
T <sub>stg</sub>	Storage Temperature		-55 to 150	°C

(\*) When Mounted on 1 inch<sup>2</sup> FR-4 board, 2 oz of Cu and t  $\leq$  10 sec.

## **ELECTRICAL CHARACTERISTICS** (T<sub>CASE</sub> = 25 °C UNLESS OTHERWISE SPECIFIED)

#### OFF

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
V <sub>(BR)</sub> DSS	Drain-source Breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0	30			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0)	$V_{DS}$ = Max Rating $V_{DS}$ = Max Rating T <sub>C</sub> = 125°C			1 10	μΑ μΑ
I <sub>GSS</sub>	Gate-body Leakage Current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 16 V			±100	nA

#### ON (\*)

Symbol	Parameter	Test Conditions		Min.	Тур.	Max.	Unit
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}$	I <sub>D</sub> = 250 μA	1			V
R <sub>DS(on)</sub>	Static Drain-source On Resistance	V <sub>GS</sub> = 10 V V <sub>GS</sub> = 4.5 V	I <sub>D</sub> = 2 A I <sub>D</sub> = 2 A		0.070 0.085	0.08 0.10	Ω Ω

#### DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
g <sub>fs</sub> (*)	Forward Transconductance	$V_{DS}$ = 15V $I_D$ = 2 A		10		S
C <sub>iss</sub> C <sub>oss</sub> C <sub>rss</sub>	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25V, f = 1 \text{ MHz}, V_{GS} = 0$		1350 490 130		pF pF pF

## ELECTRICAL CHARACTERISTICS (continued)

## SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
t <sub>d(on)</sub> t <sub>r</sub>	Turn-on Delay Time Rise Time			25 35		ns ns
Qg Qgs Qgd	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD}$ = 24 V I <sub>D</sub> = 4 A V <sub>GS</sub> = 5 V (See test circuit, Figure 2)		12.5 5 3	16	nC nC nC

#### SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
t <sub>d(off)</sub> t <sub>f</sub>	Turn-off Delay Time Fall Time	$ \begin{array}{ll} V_{DD} = 15 \ V & I_D = 2 \ A \\ R_G = 4.7 \Omega, & V_{GS} = 4.5 \ V \\ (\text{Resistive Load, Figure 1}) \end{array} $		125 35		ns ns

#### SOURCE DRAIN DIODE

Symbol	Parameter	Test C	onditions	Min.	Тур.	Max.	Unit
I <sub>SD</sub> I <sub>SDM</sub> (●)	Source-drain Current Source-drain Current (pulsed)					4 16	A A
V <sub>SD</sub> (*)	Forward On Voltage	I <sub>SD</sub> = 4 A	$V_{GS} = 0$			1.2	V
t <sub>rr</sub> Q <sub>rr</sub> I <sub>RRM</sub>	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 4 A$ $V_{DD} = 15 V$ (See test circu	di/dt = 100A/µs T <sub>j</sub> = 150°C lit, Figure 3)		45 36 1.6		ns nC A

(\*)Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
(•)Pulse width limited by safe operating area.

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**Fig. 1:** Switching Times Test Circuits For Resistive Load



Fig. 3: Test Circuit For Diode Recovery Behaviour



#### Fig. 2: Gate Charge test Circuit



DIM.		mm			inch	
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
А			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
С	0.25		0.5	0.010		0.019
c1			45	(typ.)		
D	4.8		5.0	0.188		0.196
Е	5.8		6.2	0.228		0.244
е		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
М			0.6			0.023
S			8 (r	nax.)		





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