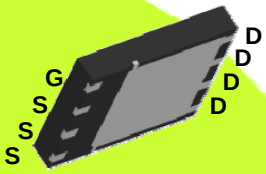
N-Channel

CICLON NexFET™ Power MOSFETs

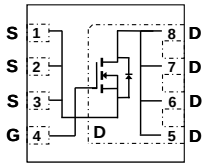
CSD16321Q5

Features

- Optimized for 5V gate drive
- Ultra Low Qg & Qgd
- Low Thermal Resistance
- Avalanche Rated
- Pb Free Terminal Plating
- RoHS Compliant



QFN 5mm x 6mm Plastic Package



Top View

Product Summary

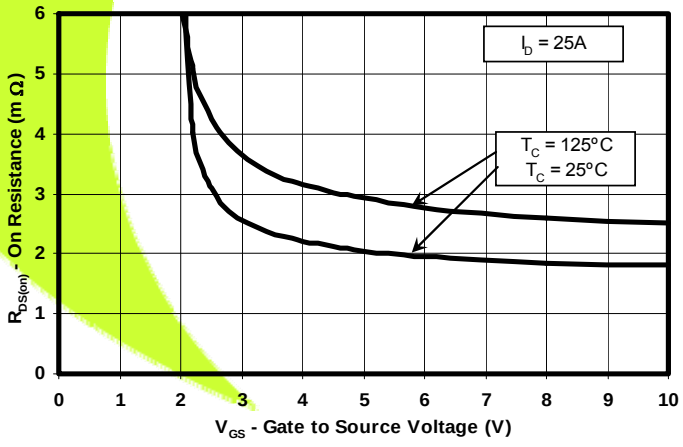
V_{DS}	25		V
Q_g	14		nC
Q_{gd}	2.5		nC
$R_{DS(on)}$	V_{GS} = 3.0V	2.8	mΩ
	V_{GS} = 4.5V	2.1	mΩ
	V_{GS} = 8.0V	1.9	mΩ
V_{th}	1.1		V

Maximum Values (T_A = 25°C unless otherwise stated)

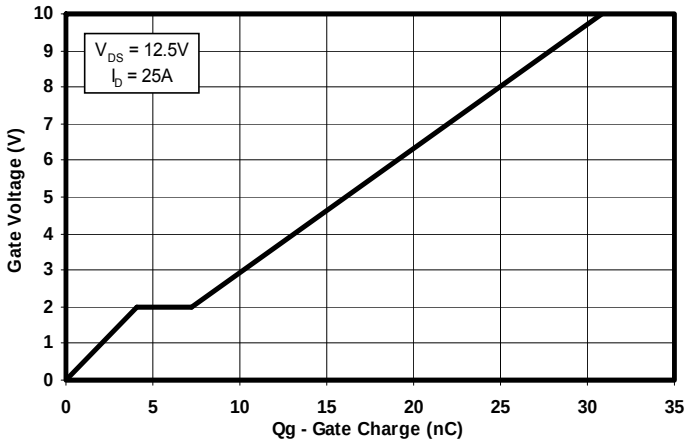
Symbol	Parameter	Value	Units
V_{DS}	Drain to Source Voltage	25	V
V_{GS}	Gate to Source Voltage	+10 / -6	V
I_D	Continuous Drain Current, T_C = 25°C	100	A
	Continuous Drain Current[1]	31	A
I_{DM}	Pulsed Drain Current, T_A = 25°C[2]	200	A
P_D	Power Dissipation[1]	3.1	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 to 150	°C
E_{AS}	Avalanche Energy, single pulse I_D =66A, L = 0.1mH, R_G = 25Ω	218	mJ

1. $R_{\theta JA}$ = 39°C/W on 1in² Cu (2 oz.) on 0.060" thick FR4 PCB.
2. See Figure 10

$R_{DS(ON)}$ vs. V_{GS}



Gate Charge



Ordering Information

Type	Package	Package Media	Qty	Ship
CSD16321Q5	QFN 5X6 Plastic Package	13 inch reel	2500	Tape and Reel

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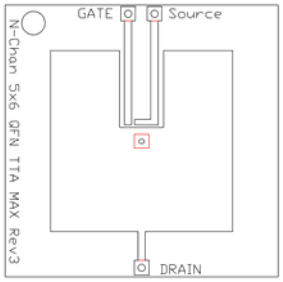
Electrical Characteristics (T_A = 25°C unless otherwise stated)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Static Characteristics						
BV_{DSS}	Drain to Source Voltage	V_{GS} = 0V, I_D = 250µA	25	—	—	V
I_{DSS}	Drain to Source Leakage Current	V_{GS} = 0V, V_{DS} = 20V	—	—	1	µA
I_{GSS}	Gate to Source Leakage Current	V_{DS} = 0V, V_{GS} = 10V	—	—	100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 250µA	0.9	1.1	1.4	V
$R_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 3.0V, I_D = 25A	—	2.8	3.5	mΩ
		V_{GS} = 4.5V, I_D = 25A	—	2.1	2.6	mΩ
		V_{GS} = 8.0V, I_D = 25A	—	1.9	2.4	mΩ
g_{fs}	Transconductance	V_{DS} = 12.5V, I_D = 25A	—	150	—	S
Dynamic Characteristics						
C_{ISS}	Input Capacitance	V_{GS} = 0V, V_{DS} = 12.5V, f = 1MHz	—	2360	3100	pF
C_{OSS}	Output Capacitance		—	1700	2200	pF
C_{RSS}	Reverse Transfer Capacitance		—	115	150	pF
R_g	Series Gate Resistance		—	1.2	—	Ω
Q_g	Gate Charge Total (4.5V)	V_{DS} = 12.5V, I_D = 25A	—	14	19	nC
Q_{gd}	Gate Charge Gate to Drain		—	2.5	—	nC
Q_{gs}	Gate Charge Gate to Source		—	4.0	—	nC
$Q_{g(th)}$	Gate Charge at Vth		—	2.1	—	nC
Q_{OSS}	Output Charge	V_{DS} = 15V, V_{GS} = 0V	—	36	—	nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = 12.5V, V_{GS} = 4.5V I_D = 25A, R_G = 2.7 Ω	—	11	—	ns
t_r	Rise Time		—	19	—	ns
$t_{d(off)}$	Turn Off Delay Time		—	40	—	ns
t_f	Fall Time		—	30	—	ns
Diode Characteristics						
V_{SD}	Diode Forward Voltage	I_S = 25A, V_{GS} = 0V	—	0.8	1.0	V
Q_{rr}	Reverse Recovery Charge	V_{dd}=13V, I_F = 25A, di/dt = 300A/µs	—	33	—	nC
t_{rr}	Reverse Recovery Time	V_{dd}=13V, I_F = 25A, di/dt = 300A/µs	—	32	—	ns

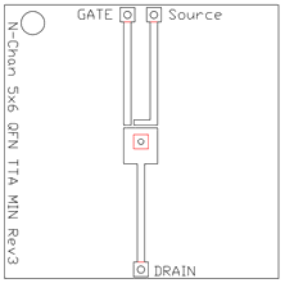
Thermal Characteristics (T_A = 25°C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Units
Thermal Characteristics					
$R_{\theta JC}$	Thermal Resistance Junction to Case[3]	—	—	1.1	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient[3,4]	—	—	50	°C/W

3. $R_{\theta jc}$ is determined with the device mounted on a 1in square 2 oz. Cu pad on a 1.5x1.5 in .060in thick FR4 board. $R_{\theta jc}$ is guaranteed by design while $R_{\theta ca}$ is determined by the user's board design.
4. Device mounted on FR4 Material with 1in^2 of 2 oz. Cu.



Max $R_{\theta ja}$ = 48°C/W when mounted on 1in^2 of 2 oz. Cu.



Max $R_{\theta ja}$ = 115°C/W when mounted on min pad area of 2 oz. Cu.

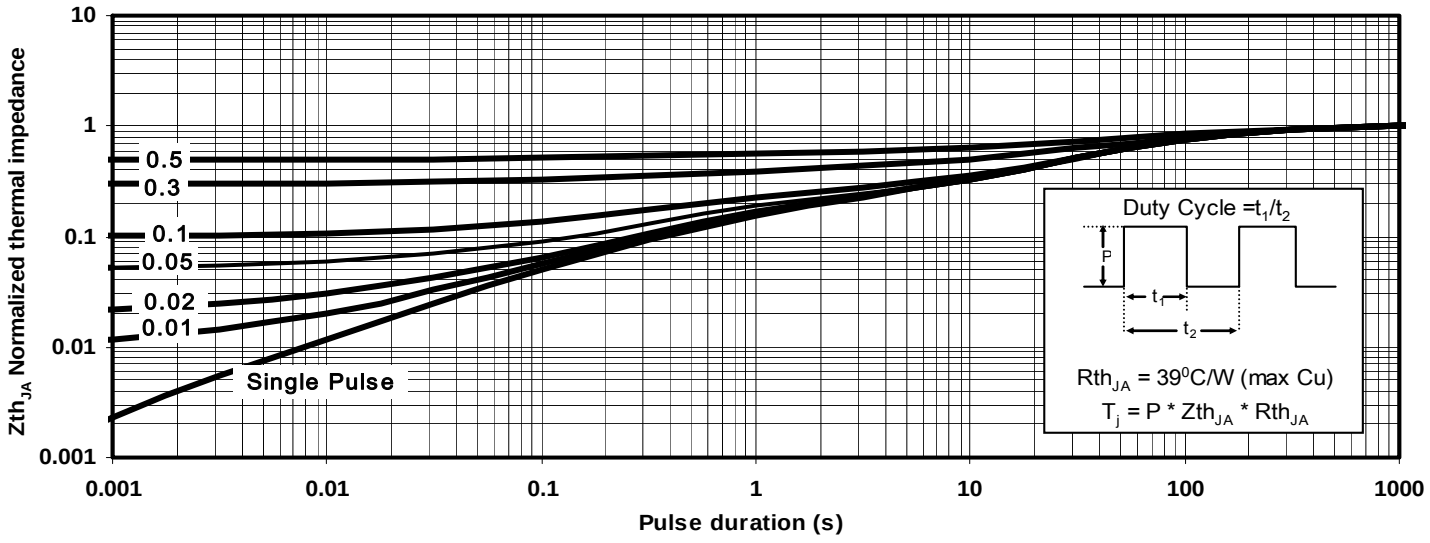


Figure 1: Transient Thermal Impedance

Typical MOSFET Characteristics (T_A = 25°C unless otherwise stated)

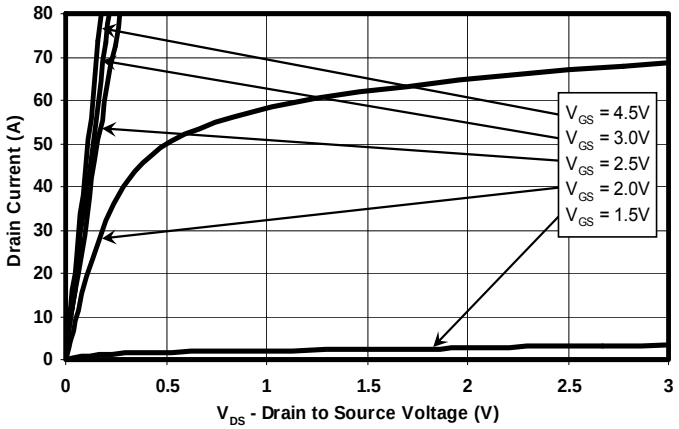


Figure 2: Saturation Characteristics

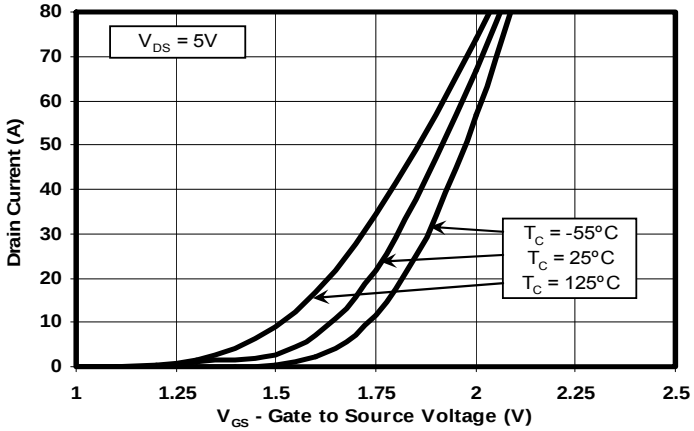


Figure 3: Transfer Characteristics

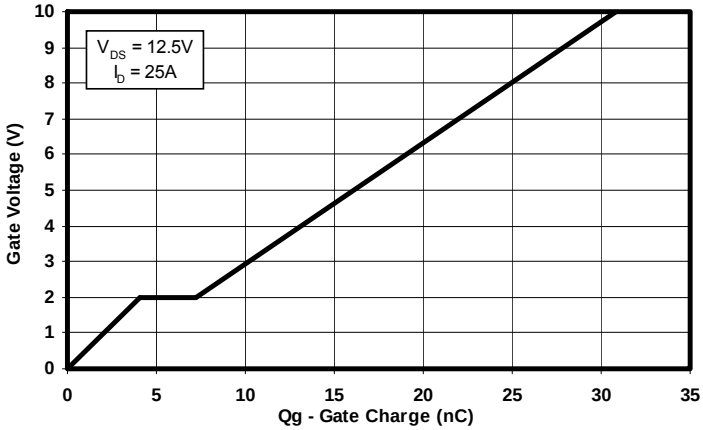


Figure 4: Gate Charge

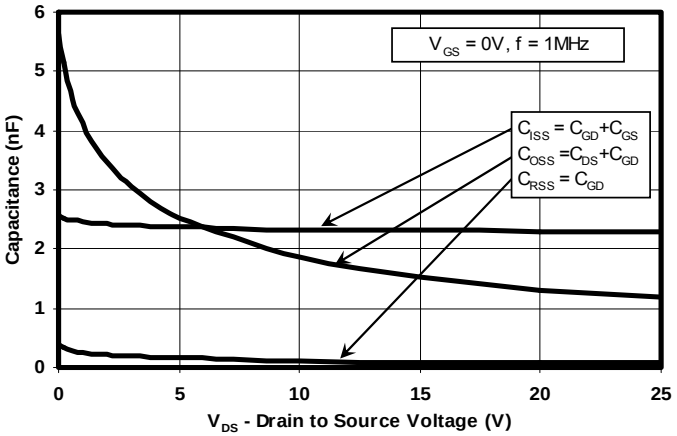


Figure 5: Capacitance

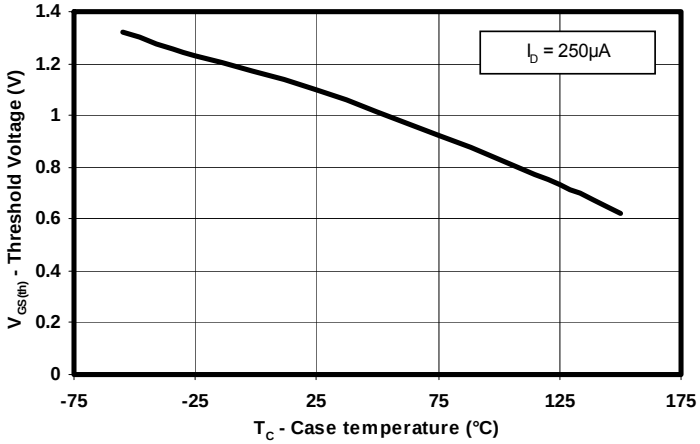


Figure 6: Threshold Voltage vs. Temperature

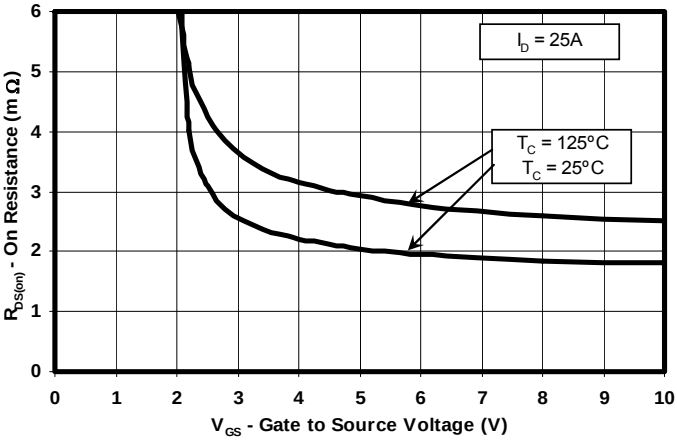


Figure 7: On Resistance vs. Gate Voltage

Typical MOSFET Characteristics (T_A = 25°C unless otherwise stated)

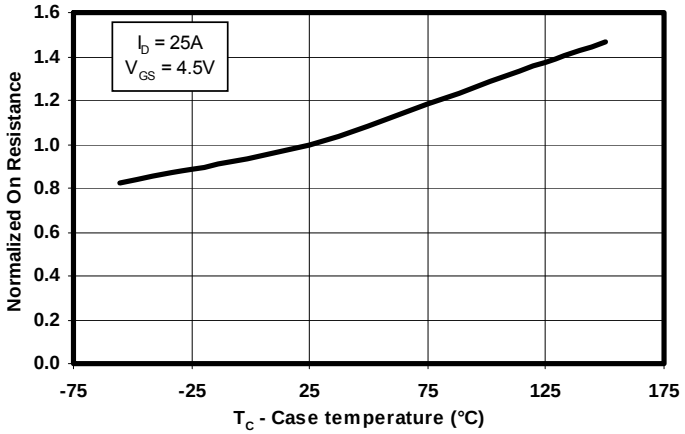


Figure 8: On Resistance vs. Temperature

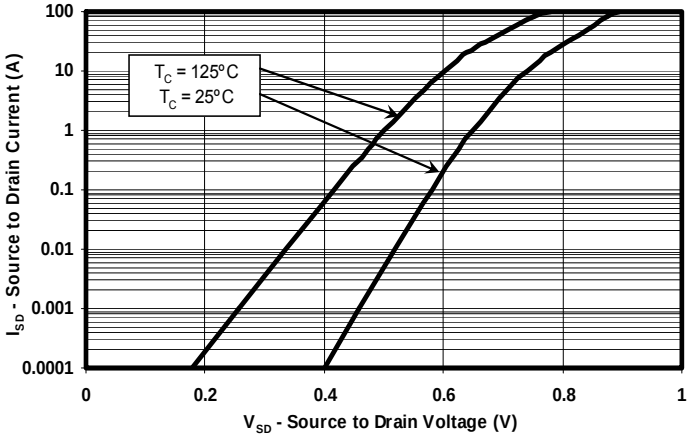


Figure 9: Typical Diode Forward Voltage

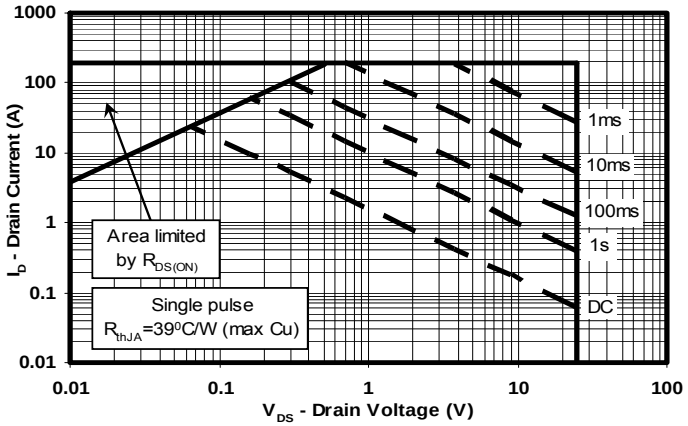


Figure 10: Maximum Safe Operating Area

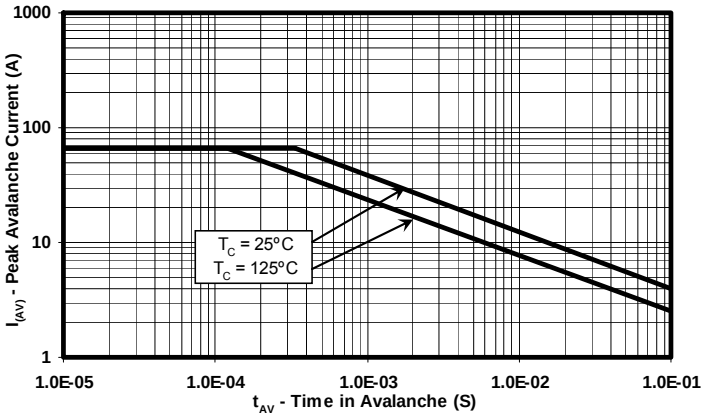


Figure 11: Single Pulse Unclamped Inductive Switching

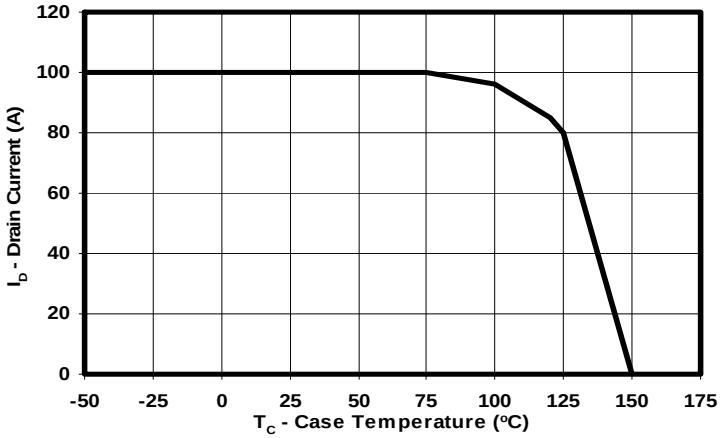


Figure 12: Maximum Drain Current vs. Temperature

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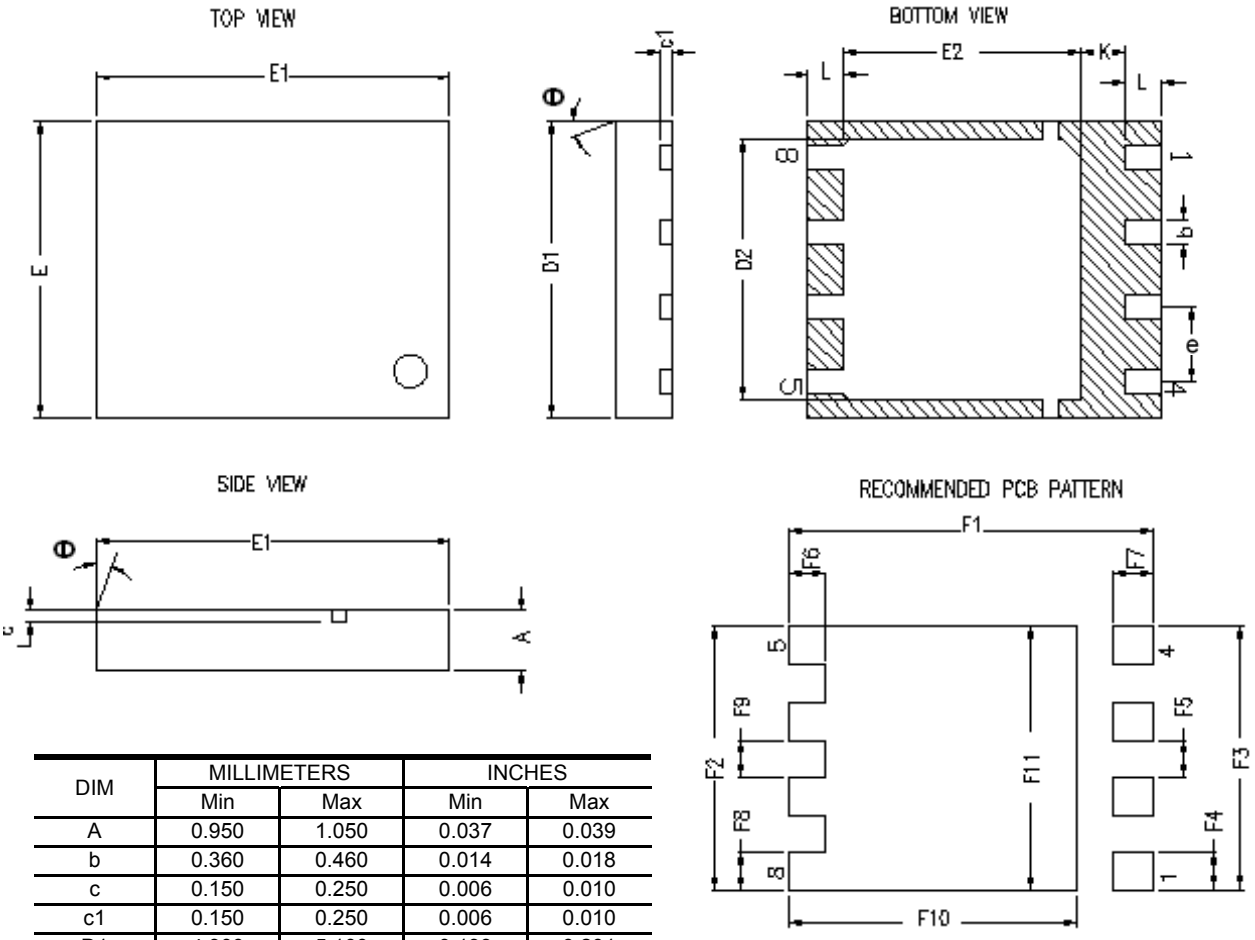
Q5 Package Dimensions



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	0.950	1.050	0.037	0.039
b	0.360	0.460	0.014	0.018
c	0.150	0.250	0.006	0.010
c1	0.150	0.250	0.006	0.010
D1	4.900	5.100	0.193	0.201
D2	4.320	4.520	0.170	0.178
E	4.900	5.100	0.193	0.201
E1	5.900	6.100	0.232	0.240
E2	3.920	4.12	0.154	0.162
e	1.27 TYP		0.050	
L	0.510	0.710	0.020	0.028
θ	0.00	-	-	-
K	0.760	-	0.030	-
F1	6.205	6.305	0.244	0.248
F2	4.460	4.560	0.176	0.180
F3	4.460	4.560	0.176	0.180
F4	0.650	0.700	0.026	0.028
F5	0.620	0.670	0.024	0.026
F6	0.630	0.680	0.025	0.027
F7	0.700	0.800	0.028	0.031
F8	0.650	0.700	0.026	0.028
F9	0.620	0.670	0.024	0.026
F10	4.900	5.000	0.193	0.197
F11	4.460	4.560	0.176	0.180

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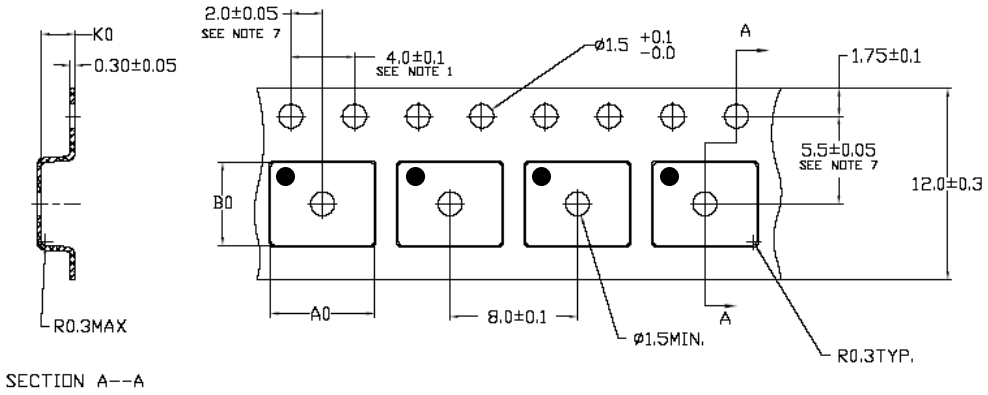
Q5 Tape and Reel Information



A0=6.5±0.1
B0=5.3±0.1
K0=1.4±0.1

Note:

1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE +/-0.2
2. CAMBER NOT TO EXCEED 1mm IN 100mm, NONCUMULATIVE OVER 250mm
3. MATERIAL:BLACK STATIC DISSIPATIVE POLYSTYRENE
4. ALL DIMENSIONS ARE IN mm (UNLESS OTHERWISE SPECIFIED)
5. THICKNESS: 0.30 +/-0.05mm

Package Marking Information

Location:

1st Line

CSD = Fixed Characters

NNNNN = Product Code

2nd Line (Date Code)

YY = Last 2 digits of the Year

WW = 2-digit Work Week

C = Country of Origin

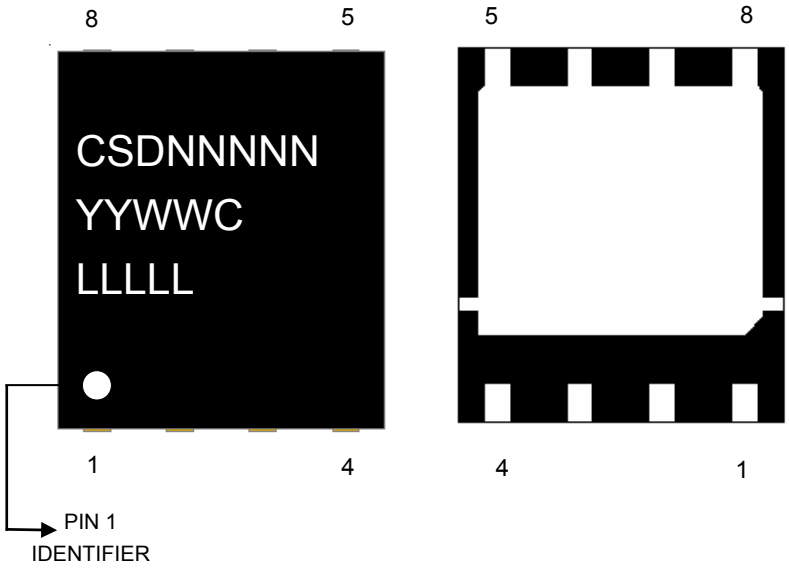
> Philippines = P

> Taiwan = T

> China = C

3rd Line

LLLLL= Last 5 digits of the Wafer Lot #



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