

IRFP22N60K

HEXFET® Power MOSFET

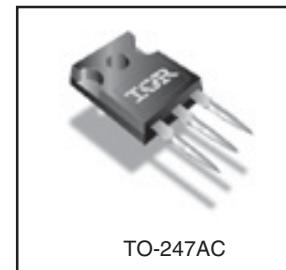
Applications

- Hard Switching Primary or PFS Switch
- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Speed Power Switching
- Motor Drive

Benefits

- Low Gate Charge Qg results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Enhanced Body Diode dv/dt Capability

V _{DSS}	R _{DS(on)} typ.	I _D
600V	240mΩ	22A



TO-247AC

Absolute Maximum Ratings

	Parameter	Max.	Units
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V	22	
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V	14	A
I _{DM}	Pulsed Drain Current ①	88	
P _D @ T _C = 25°C	Power Dissipation	370	W
	Linear Derating Factor	2.9	W/°C
V _{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ③	18	V/ns
T _J T _{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	°C

Avalanche Characteristics

Symbol	Parameter	Typ.	Max.	Units
E _{AS}	Single Pulse Avalanche Energy②	—	380	mJ
I _{AR}	Avalanche Current①	—	22	A
E _{AR}	Repetitive Avalanche Energy①	—	37	mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
R _{θJC}	Junction-to-Case⑥	—	0.34	
R _{θCS}	Case-to-Sink, Flat, Greased Surface	0.24	—	°C/W
R _{θJA}	Junction-to-Ambient⑥	—	40	

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Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(\text{BR})\text{DSS}}$	Drain-to-Source Breakdown Voltage	600	—	—	V	$V_{\text{GS}} = 0\text{V}, I_D = 250\mu\text{A}$
$\Delta V_{(\text{BR})\text{DSS}/\Delta T_J}$	Breakdown Voltage Temp. Coefficient	—	0.30	—	V°C	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$ ⑥
$R_{\text{DS}(\text{on})}$	Static Drain-to-Source On-Resistance	—	240	280	$\text{m}\Omega$	$V_{\text{GS}} = 10\text{V}, I_D = 13\text{A}$ ④
$V_{\text{GS}(\text{th})}$	Gate Threshold Voltage	3.0	—	5.0	V	$V_{\text{DS}} = V_{\text{GS}}, I_D = 250\mu\text{A}$
I_{DS}	Drain-to-Source Leakage Current	—	—	50	μA	$V_{\text{DS}} = 600\text{V}, V_{\text{GS}} = 0\text{V}$
				250	μA	$V_{\text{DS}} = 480\text{V}, V_{\text{GS}} = 0\text{V}, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{\text{GS}} = 30\text{V}$
				-100	nA	$V_{\text{GS}} = -30\text{V}$

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	11	—	—	S	$V_{\text{DS}} = 50\text{V}, I_D = 13\text{A}$
Q_g	Total Gate Charge	—	—	150		$I_D = 22\text{A}$
Q_{gs}	Gate-to-Source Charge	—	—	45	nC	$V_{\text{DS}} = 480\text{V}$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	76		$V_{\text{GS}} = 10\text{V}$ ④
$t_{\text{d}(\text{on})}$	Turn-On Delay Time	—	26	—		$V_{\text{DD}} = 300\text{V}$
t_r	Rise Time	—	99	—	ns	$I_D = 22\text{A}$
$t_{\text{d}(\text{off})}$	Turn-Off Delay Time	—	48	—		$R_G = 6.2\ \Omega$
t_f	Fall Time	—	37	—		$V_{\text{GS}} = 10\text{V}$ ④
C_{iss}	Input Capacitance	—	3570	—		$V_{\text{GS}} = 0\text{V}$
C_{oss}	Output Capacitance	—	350	—	pF	$V_{\text{DS}} = 25\text{V}$
C_{rss}	Reverse Transfer Capacitance	—	36	—		$f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	4710	—		$V_{\text{GS}} = 0\text{V}, V_{\text{DS}} = 1.0\text{V}, f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	92	—		$V_{\text{GS}} = 0\text{V}, V_{\text{DS}} = 480\text{V}, f = 1.0\text{MHz}$
$C_{\text{oss eff.}}$	Effective Output Capacitance	—	180	—		$V_{\text{GS}} = 0\text{V}, V_{\text{DS}} = 0\text{V to } 480\text{V}$ ⑤

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_s	Continuous Source Current (Body Diode)	—	—	22	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	88		
V_{SD}	Diode Forward Voltage	—	—	1.5	V	$T_J = 25^\circ\text{C}, I_S = 22\text{A}, V_{\text{GS}} = 0\text{V}$ ④
t_{rr}	Reverse Recovery Time	—	590	890	ns	$T_J = 25^\circ\text{C}$ $I_F = 22\text{A}$
			670	1010		$T_J = 125^\circ\text{C}$ $\text{di/dt} = 100\text{A}/\mu\text{s}$ ④
Q_{rr}	Reverse Recovery Charge	—	7.2	11	μC	$T_J = 25^\circ\text{C}$
			8.5	13		$T_J = 125^\circ\text{C}$
I_{RRM}	Reverse Recovery Current	—	26	39	A	$T_J = 25^\circ\text{C}$
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 1.5\text{mH}$, $R_G = 25\Omega$, $I_{AS} = 22\text{A}$
- ③ $I_{SD} \leq 22\text{A}$, $\text{di/dt} \leq 540\text{ A}/\mu\text{s}$, $V_{\text{DD}} \leq V_{(\text{BR})\text{DSS}}$, $T_J \leq 150^\circ\text{C}$.
- ④ Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑤ $C_{\text{oss eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑥ R_θ is measured at T_J approximately 90°C

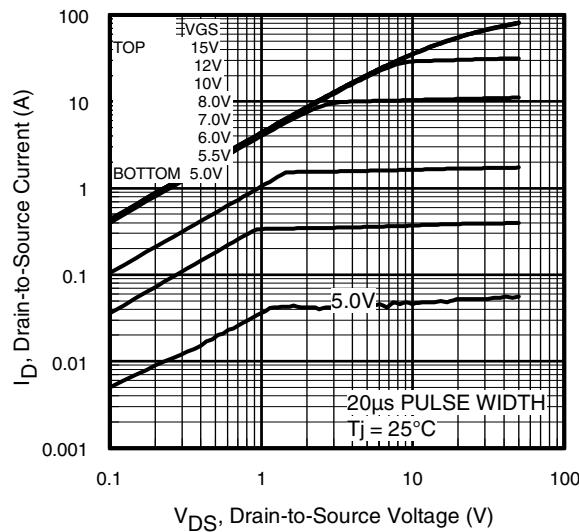


Fig 1. Typical Output Characteristics

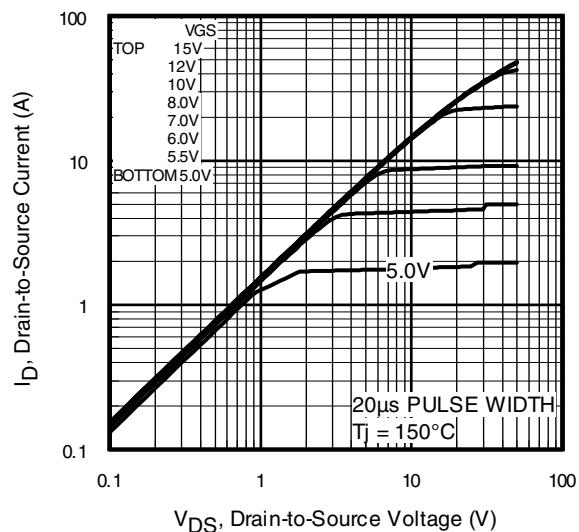


Fig 2. Typical Output Characteristics

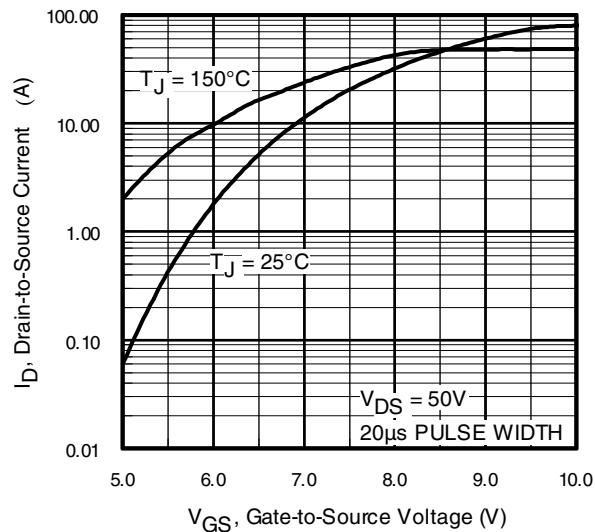


Fig 3. Typical Transfer Characteristics

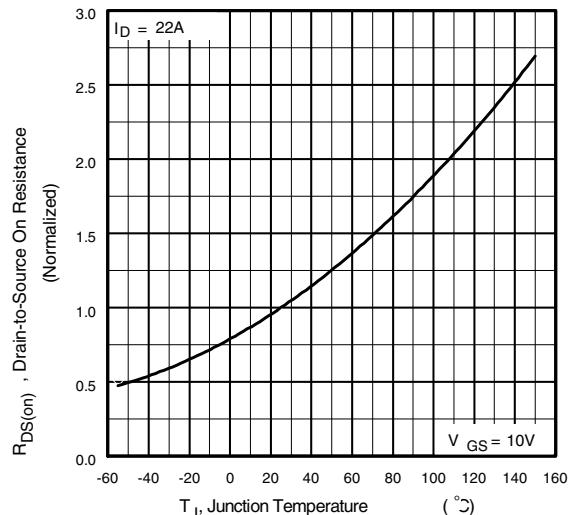


Fig 4. Normalized On-Resistance
Vs. Temperature

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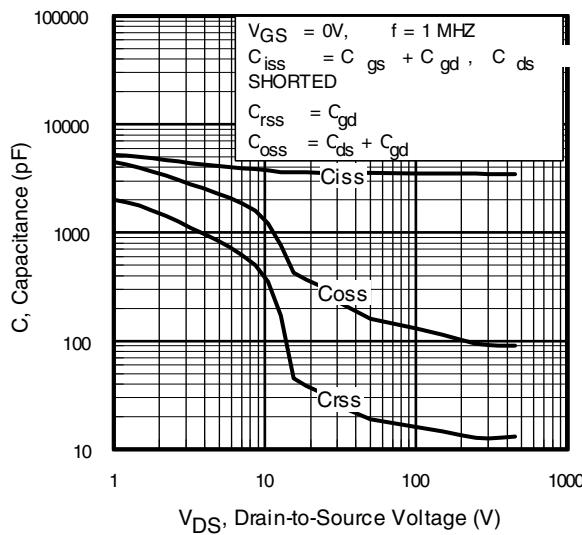


Fig 5. Typical Capacitance Vs.
Drain-to-Source Voltage

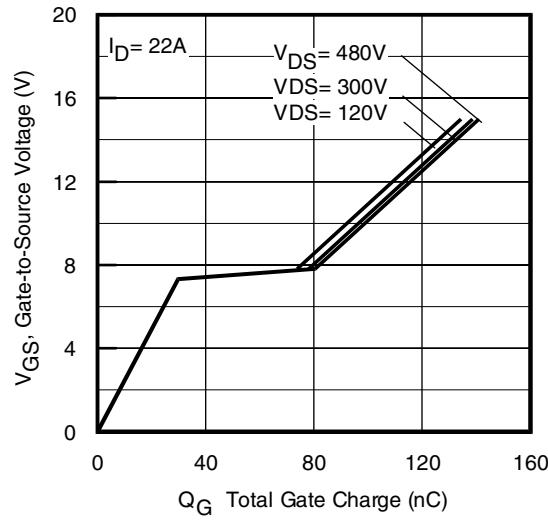


Fig 6. Typical Gate Charge Vs.
Gate-to-Source Voltage

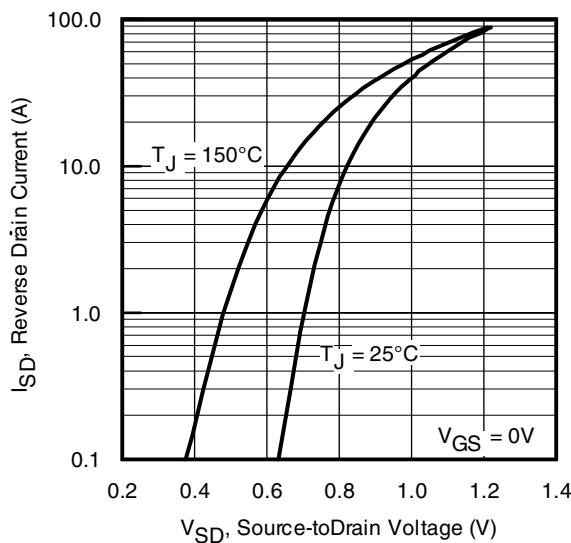


Fig 7. Typical Source-Drain Diode
Forward Voltage

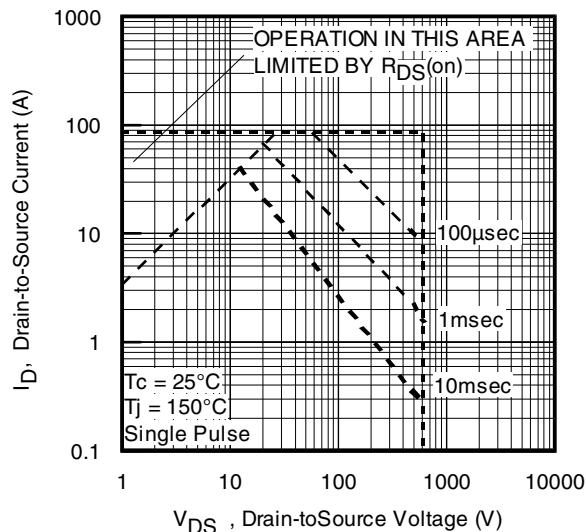


Fig 8. Maximum Safe Operating Area

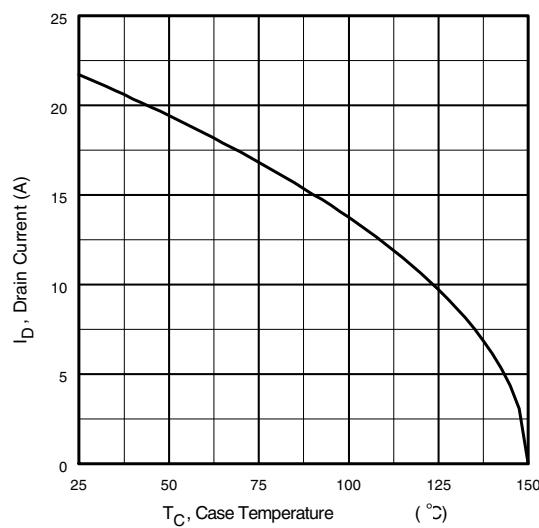


Fig 9. Maximum Drain Current Vs.
Case Temperature

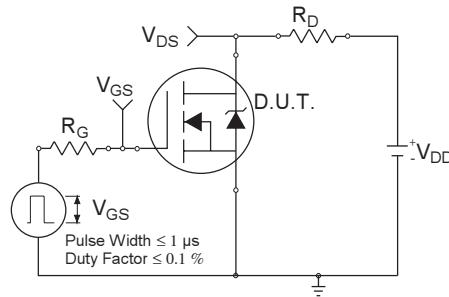


Fig 10a. Switching Time Test Circuit

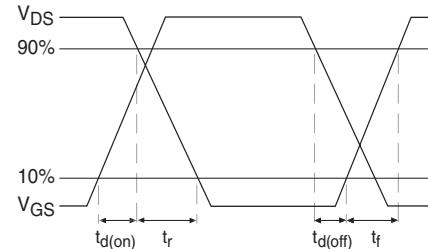


Fig 10b. Switching Time Waveforms

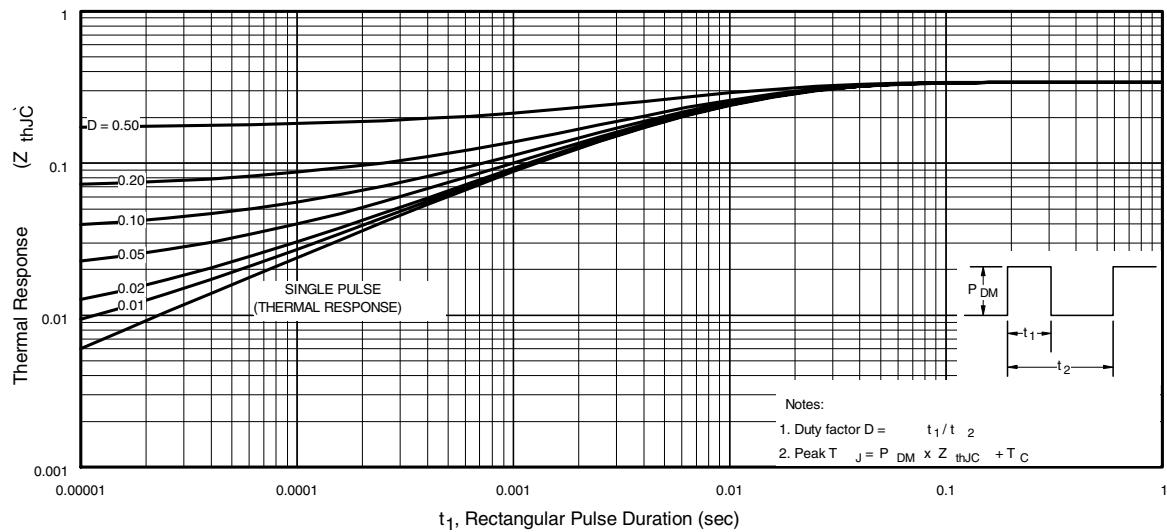


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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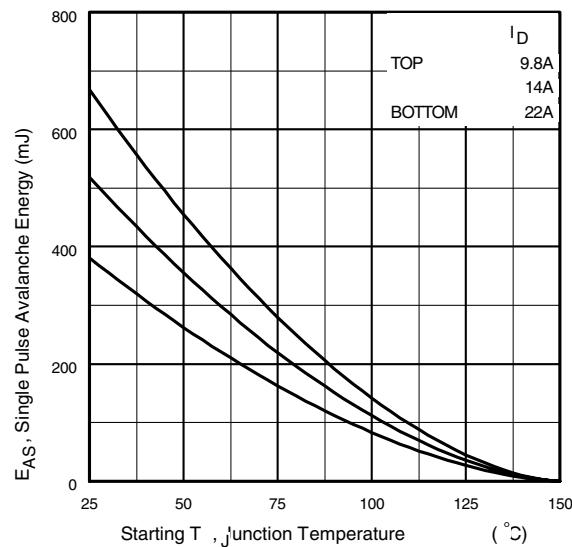


Fig 12a. Maximum Avalanche Energy Vs. Drain Current

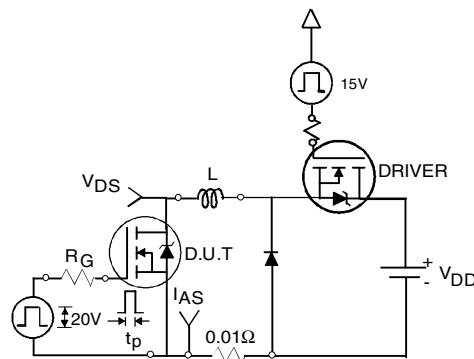


Fig 12c. Unclamped Inductive Test Circuit

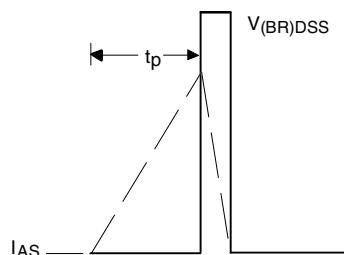


Fig 12d. Unclamped Inductive Waveforms

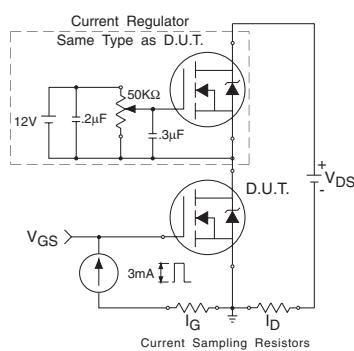


Fig 13a. Gate Charge Test Circuit

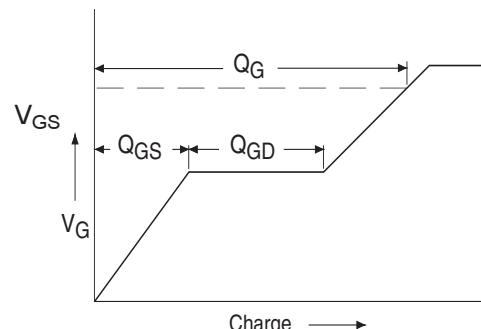
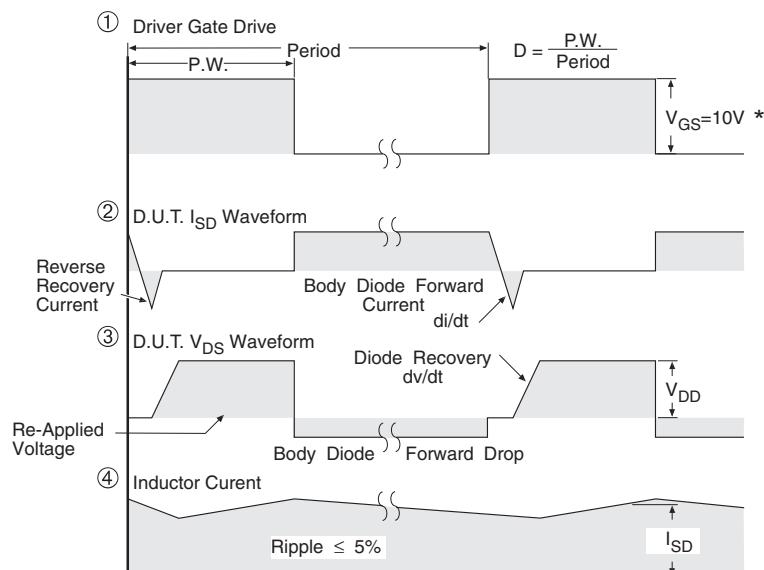
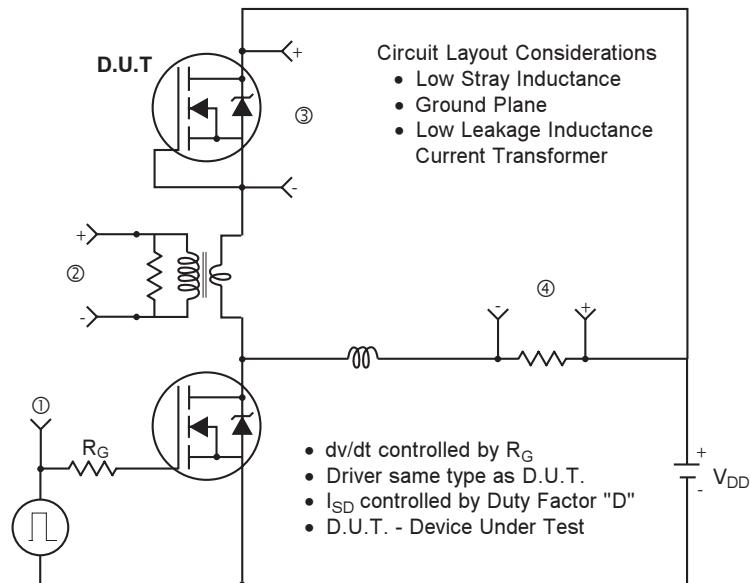


Fig 13b. Basic Gate Charge Waveform

Peak Diode Recovery dv/dt Test Circuit



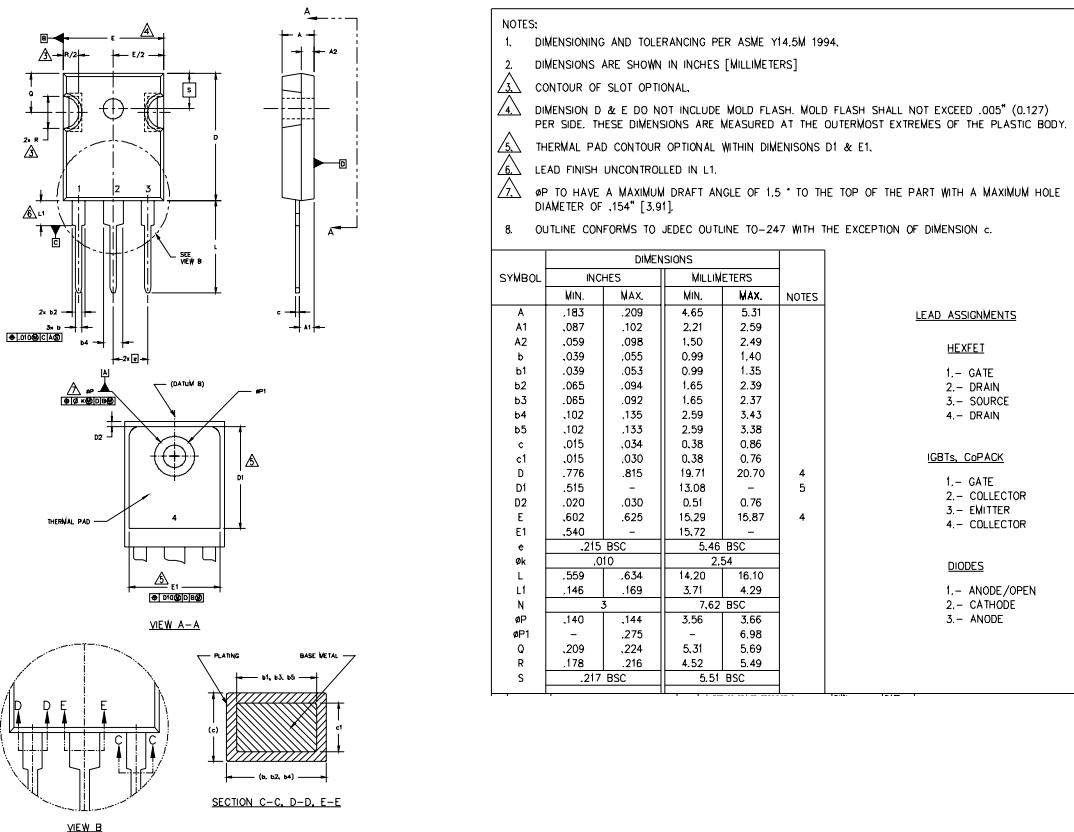
* $V_{GS} = 5V$ for Logic Level Devices

Fig 14. For N-Channel HEXFET® Power MOSFETs

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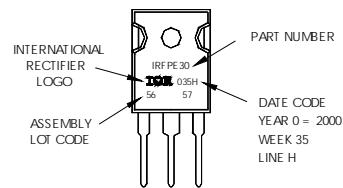
TO-247AC Package Outline Dimensions are shown in millimeters (inches)



TO-247AC Part Marking Information

EXAMPLE: THIS IS AN IRFPE30
WITH ASSEMBLY
LOT CODE 5657
ASSEMBLED ON WW 35, 2000
IN THE ASSEMBLY LINE "H"

Note: "P" in assembly line
position indicates "Lead-Free"



Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

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TAC Fax: (310) 252-7903
08/04



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