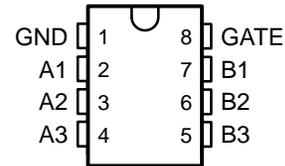


- **Designed to Be Used in Voltage-Limiting Applications**
- **3.5-Ω On-State Connection Between Ports A and B**
- **Flow-Through Pinout for Ease of Printed Circuit Board Trace Routing**
- **Direct Interface With GTL+ Levels**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

**DCT OR DCU PACKAGE
(TOP VIEW)**



description

The SN74TVC3306 provides three parallel NMOS pass transistors with a common unbuffered gate. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

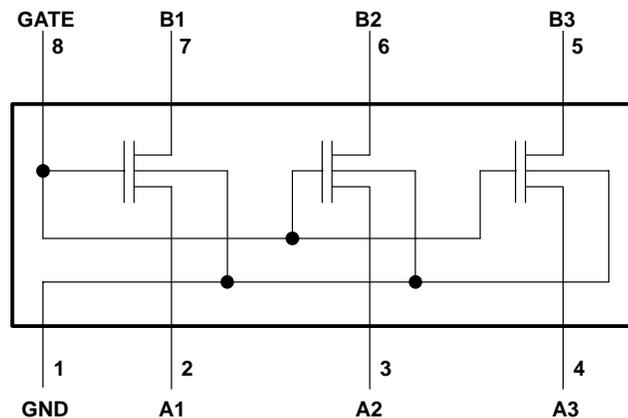
The device can be used as a dual switch, with the gates cascaded together to a reference transistor. The low-voltage side of each pass transistor is limited to a voltage set by the reference transistor. This is done to protect components with inputs that are sensitive to high-state voltage-level overshoots.

ORDERING INFORMATION

T _A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SSOP – DCT	Tape and reel	SN74TVC3306DCTR	FA6
	VSSOP – DCU	Tape and reel	SN74TVC3306DCUR	FA6

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

logic diagram (positive logic)



NOTE A: The SN74TVC3306 has bidirectional capability across many voltage levels. The voltage levels documented in this data sheet are examples.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SN74TVC3306 DUAL VOLTAGE CLAMP

SCDS112C – MARCH 2001 – REVISED MARCH 2002

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Input/output voltage range, $V_{I/O}$ (see Note 1)	–0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2): DCT package	220°C/W
DCU package	227°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and input/output negative-voltage ratings may be exceeded if the input and input/output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

	MIN	MAX	UNIT
$V_{I/O}$ Input/output voltage	0	5	V
V_{GATE} GATE voltage	0	5	V
I_{PASS} Pass transistor current		64	mA
T_A Operating free-air temperature	–40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{IK}	$I_I = -18$ mA,	$V_{GATE} = 0$			–1.2	V
I_{IH}	$V_I = 5$ V,	$V_{GATE} = 0$			5	μA
$C_{i(GATE)}$	$V_I = 3$ V or 0			11		pF
$C_{io(off)}$	$V_O = 3$ V or 0,	$V_{GATE} = 0$		4	6	pF
$C_{io(on)}$	$V_O = 3$ V or 0,	$V_{GATE} = 3$ V		10.5	12.5	pF
$r_{on}§$	$V_I = 0$	$I_O = 64$ mA	$V_{GATE} = 4.5$ V	3.5	5.5	Ω
			$V_{GATE} = 3$ V	4.7	7	
			$V_{GATE} = 2.3$ V	6.3	9.5	
	$V_I = 2.4$ V	$I_O = 15$ mA	$V_{GATE} = 4.5$ V	4.8	7.5	
			$V_{GATE} = 3$ V	14.7	23	
			$V_{GATE} = 2.3$ V	11.3	16.5	

‡ All typical values are at $T_A = 25^\circ\text{C}$.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.



ac performance (translating down)

switching characteristics over recommended operating free-air temperature range, $V_{GATE} = 3.3\text{ V}$, $V_{IH} = 3.3\text{ V}$, $V_{IL} = 0$, and $V_M = 1.15\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$C_L = 50\text{ pF}$		$C_L = 30\text{ pF}$		$C_L = 15\text{ pF}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	0	0.8	0	0.6	0	0.3	ns
t_{PHL}			0	1.2	0	1	0	0.5	

switching characteristics over recommended operating free-air temperature range, $V_{GATE} = 2.5\text{ V}$, $V_{IH} = 2.5\text{ V}$, $V_{IL} = 0$, and $V_M = 0.75\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$C_L = 50\text{ pF}$		$C_L = 30\text{ pF}$		$C_L = 15\text{ pF}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	0	1	0	0.7	0	0.4	ns
t_{PHL}			0	1.3	0	1	0	0.6	

ac performance (translating up)

switching characteristics over recommended operating free-air temperature range, $V_{GATE} = 3.3\text{ V}$, $V_{IH} = 2.3\text{ V}$, $V_{IL} = 0$, $V_T = 3.3\text{ V}$, $V_M = 1.15\text{ V}$, and $R_L = 300\ \Omega$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$C_L = 50\text{ pF}$		$C_L = 30\text{ pF}$		$C_L = 15\text{ pF}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	0	0.9	0	0.6	0	0.4	ns
t_{PHL}			0	1.4	0	1.1	0	0.7	

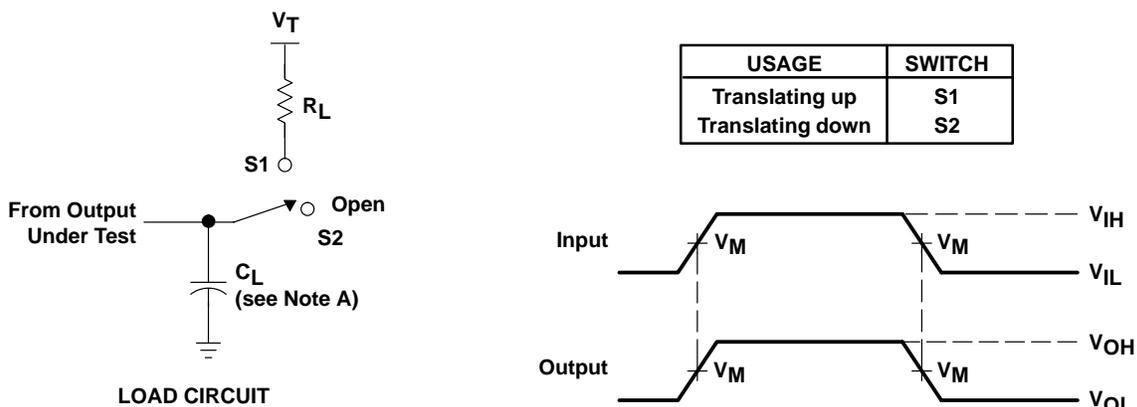
switching characteristics over recommended operating free-air temperature range, $V_{GATE} = 2.5\text{ V}$, $V_{IH} = 1.5\text{ V}$, $V_{IL} = 0$, $V_T = 2.5\text{ V}$, $V_M = 0.75\text{ V}$, and $R_L = 300\ \Omega$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$C_L = 50\text{ pF}$		$C_L = 30\text{ pF}$		$C_L = 15\text{ pF}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	0	1	0	0.6	0	0.4	ns
t_{PHL}			0	1.3	0	1.3	0	0.8	

SN74TVC3306 DUAL VOLTAGE CLAMP

SCDS112C – MARCH 2001 – REVISED MARCH 2002

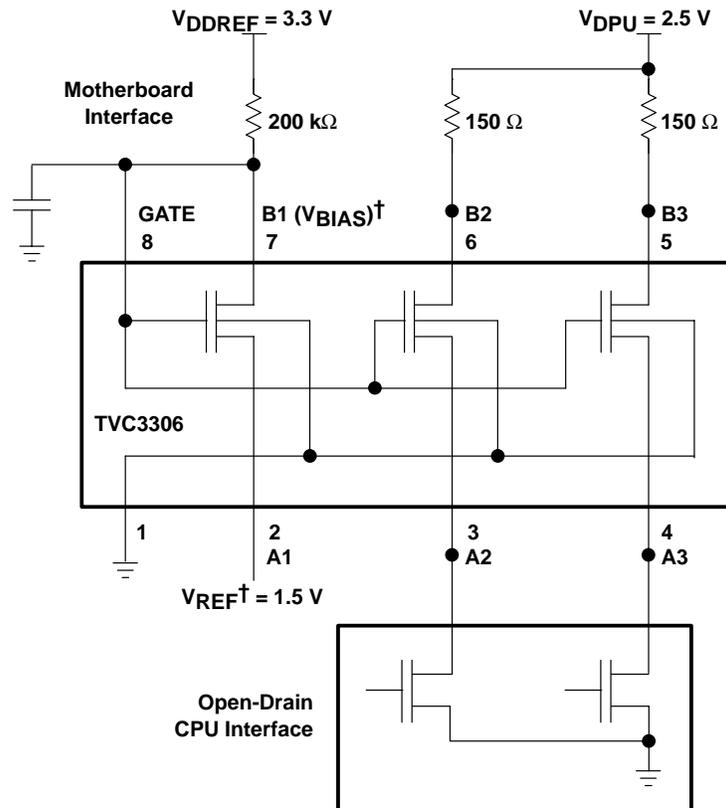
PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2$ ns, $t_f \leq 2$ ns.
 C. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit for Outputs

APPLICATION INFORMATION



† V_{REF} and V_{BIAS} can be applied to any one of the pass transistors. GATE must be connected externally to V_{BIAS} .

Figure 2. Typical Application Circuit

For the clamping configuration, the common GATE input must be connected to one side (An or Bn) of any one of the pass transistors, making that the V_{BIAS} connection of the reference transistor and the opposite side (Bn or An) the V_{REF} connection. When V_{BIAS} is connected through a 200-kΩ resistor to a 3-V to 5.5-V V_{CC} supply and V_{REF} is set to 0 V to $V_{CC} - 0.6$ V, the output of each switch has a maximum clamp voltage equal to V_{REF} . A filter capacitor on V_{BIAS} is recommended.

application operating conditions (see Figure 2)

		MIN	TYP‡	MAX	UNIT
V_{BIAS}	BIAS voltage	$V_{REF} + 0.6$	2.1	5	V
V_{GATE}	GATE voltage	$V_{REF} + 0.6$	2.1	5	V
V_{REF}	Reference voltage	0	1.5	4.4	V
V_{DPU}	Drain pullup voltage	2.36	2.5	2.64	V
I_{PASS}	Pass-transistor current		14		mA
I_{REF}	Reference-transistor current		5		μA
T_A	Operating free-air temperature	-40		85	°C

‡ All typical values are at $T_A = 25^\circ\text{C}$.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265