DATA SHEET

IP4220CZ6

Dual USB 2.0 Integrated ESD protection to IEC 61000-4-2 level 4

Product Specification

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Philips
Semiconductors

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Dual USB 2.0 Integrated ESD Protection

IP4220CZ6

FEATURES

- ESD IEC 61000-4-2 level 4, ± 8kV contact discharge compliant protection
- Four ultra-low input capacitance (1 pF typ.) ESD rail-to-rail protection diodes
- Low voltage clamping due to integrated Zener diode
- Small 6 lead SO6 (SOT457) package

APPLICATIONS

General-purpose downstream ESD protection high frequency analog signals and high-speed serial data transmission for ports inside:

- Cellular and PCS mobile handsets
- PC-/Notebook USB2.0/IEEE1394 ports
- DVI interfaces
- Cordless telephones
- Wireless data (WAN/LAN) systems
- PDAs

DESCRIPTION

The IP4220CZ6 is designed to protect I/Os being sensitive concerning capacitive load, such as USB 2.0, Ethernet, DVI etc. from destruction by Electro Static Discharges (ESD).
Therefore, the IP4220CZ6 incorporates four pairs of ultra-low capacity rail-to-rail diodes plus an additional Zener diode to provide protection to downstream signal and supply components from Electrostatic Discharge (ESD) voltages as high as ±8 kV contact discharge.
Due to the rail-to-rail diodes being connected to the Zener diode, the protection is working independent form the availability of a supply voltage.
The IP4220CZ6 is fabricated using thin film-on-silicon technology and integrates 4 ultra-low capacity rail-to-rail ESD protection diodes in a miniature 6-lead SOT457 package.

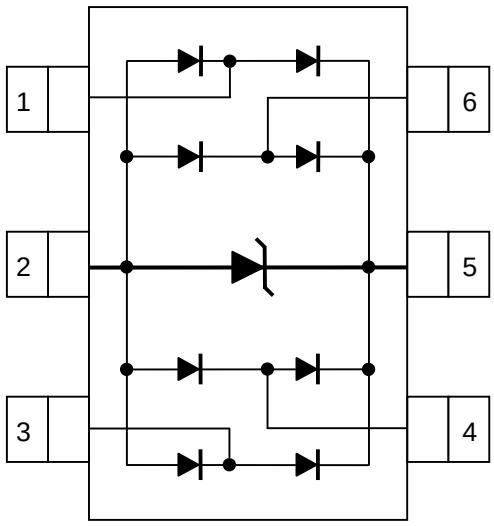


Figure 1: IP4220CZ6
schematic and pinning diagram

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
$V_{I/O}$	DC input voltage range		0	+5.5	V
ESD	Electrostatic Discharge, all pins	IEC 61000-4-2, Level 4, Contact	-8	+8	kV
T_{stg}	Device storage temperature range		-55	+125	°C

RECOMMENDED OPERATING CONDITIONS

	MIN	MAX	UNIT
Operating temperature range	-40	+85	°C

ELECTRICAL CHARACTERISTICS

Tc = 25°C unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$C_{I/O}$	Pin capacitance to ground, Pins 1, 3, 4, 6	V_{dc} = 0 V; f = 1 MHz Pin 5 = +3.0 V	-	1.0	-	pF
I_{lkg}	Diode reverse leakage current, Pins 1, 3, 4, 6 to ground	V = + 3.0V	-	-	100	nA
C_{Zener}	Zener diode capacitance to ground, Pin 5 to 2	V_{dc} = 0 V; f = 1 MHz Pin 5 = +3.0 V	-	40	-	pF
$V_{BR\ I/O}$	Zener diode breakdown voltage, Pin 5 to 2	I = 1mA	6	-	9	V
V_F	Forward voltage		-	0.7	-	V

Application Information

Universal Serial Bus 2.0 protection

The IP4220CZ6 is optimized to protect e.g. two USB 2.0 ports of Electro-Static-Discharge (ESD). Each device is capable of protection both USB data lines and the V_{BUS} supply.
A typical application is shown in the schematic below.

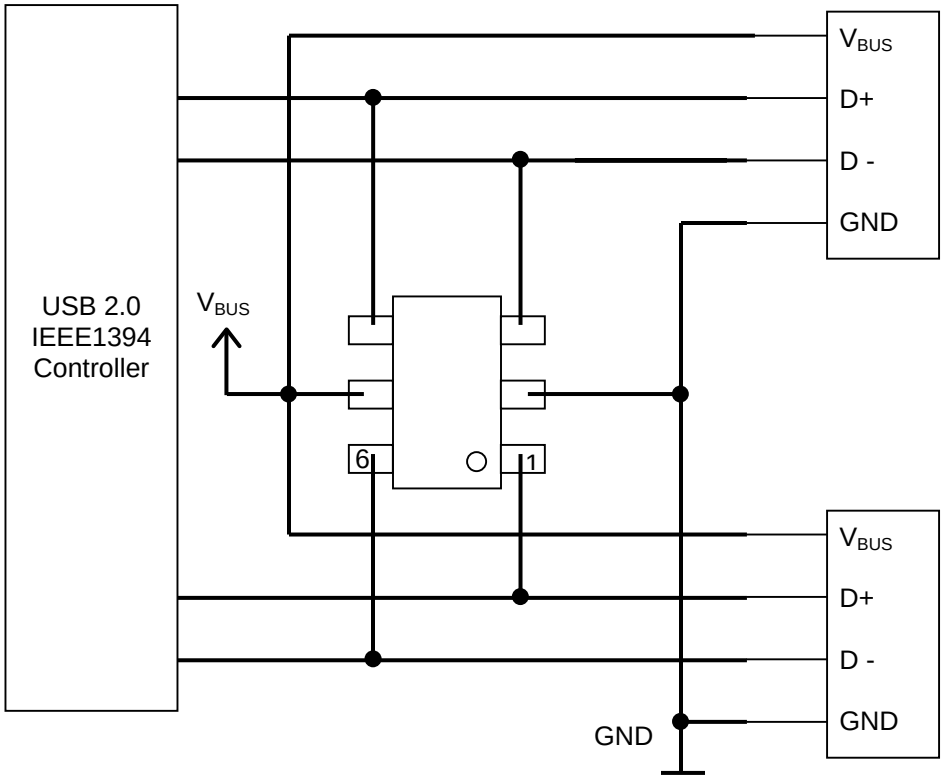
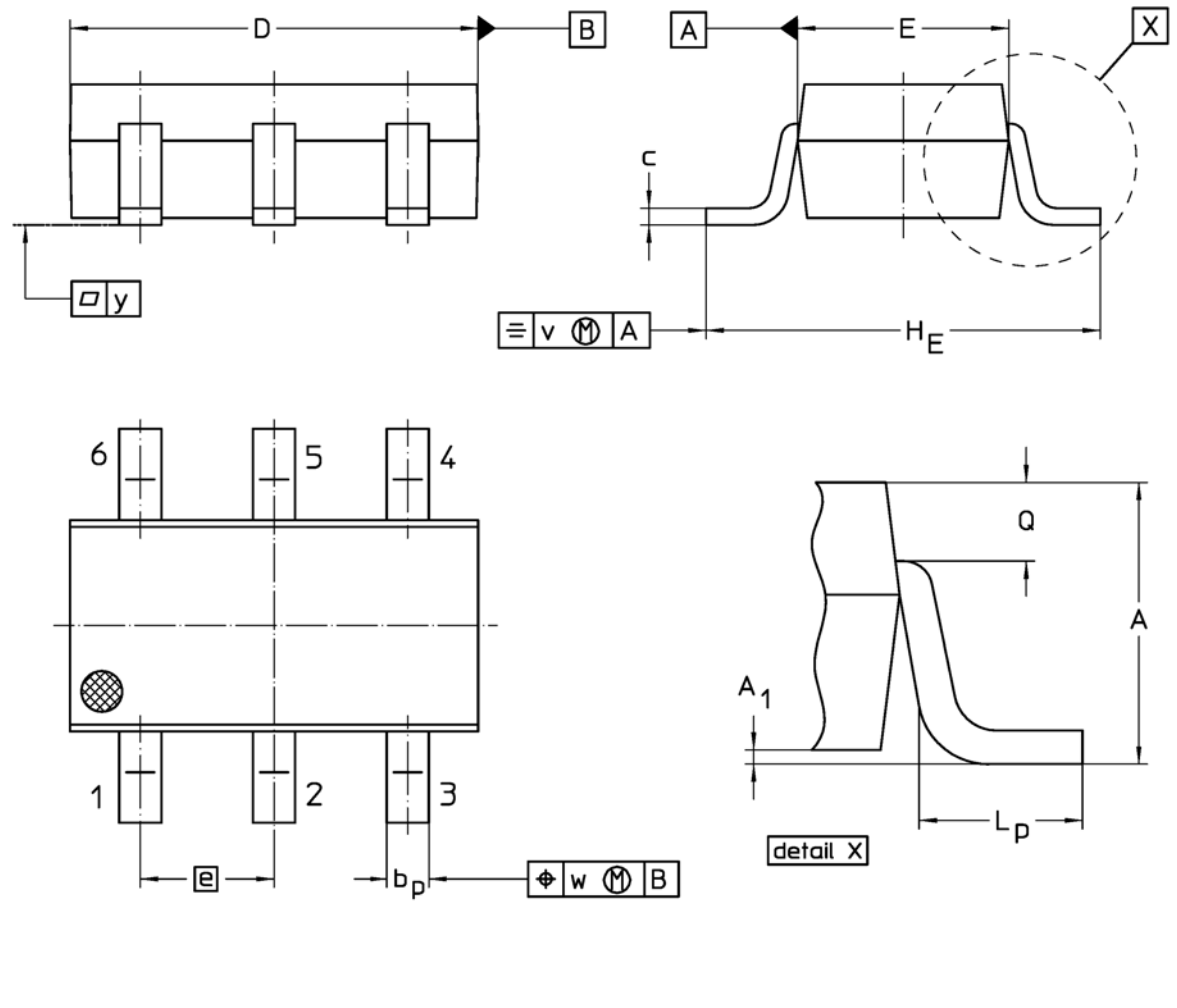


Figure 2: Typical application of IP4220CZ6

PACKAGE OUTLINE

Plastic small outline package; 6 leads; body width 1.5 mm SOT457



UNIT	A	A_1	b_p	c	D	E	e	H_E	L_p	Q	v	w	y
mm	1,1 0,9	0,1 0,013	0,4 0,25	0,26 0,1	3,1 2,7	1,7 1,3	0,95	3,0 2,5	0,6 0,2	0,33 0,23	0,2	0,2	0,1

Figure 3: IP4220CZ6 outline dimensions

DEFINITIONS		
Data Sheet Identification	**Product Status**	**Definition**
Objective Specification	Formative or in Design	This data sheet contains the target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve the design and supply the best possible product.
Product Specification	Full Production	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve the design and supply the best possible product.

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