

BT168GW

Thyristors; logic level for RCD/GFI/LCCB applications

Rev. 04 — 12 November 2004

Product data sheet

1. Product profile

1.1 General description

Passivated, sensitive gate thyristor in a SOT223 plastic package.

1.2 Features

- Designed to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

1.3 Applications

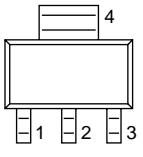
- For use in Residual Current Devices (RCD), Ground Fault Interrupters (GFI) and Leakage Current Circuit Breakers (LCCB) applications where a minimum I_{GT} limit is needed.

1.4 Quick reference data

- | | |
|--------------------------|--|
| ■ $V_{DRM} \leq 600$ V | ■ $I_{T(RMS)} \leq 1$ A |
| ■ $V_{RRM} \leq 600$ V | ■ $I_{TSM} \leq 8$ A |
| ■ $I_{T(AV)} \leq 0.6$ A | ■ $I_{GT} = 50 \mu\text{A}$ (typical). |

2. Pinning information

Table 1: Pinning

Pin	Description	Simplified outline	Symbol
1	cathode		
2	anode		
3	gate		
4	anode	 SOT223	

3. Ordering information

Table 2: Ordering information

Type number	Package			Version
	Name	Description		
BT168GW	SC-73	plastic surface mounted package with increased heatsink; 4 leads		SOT223

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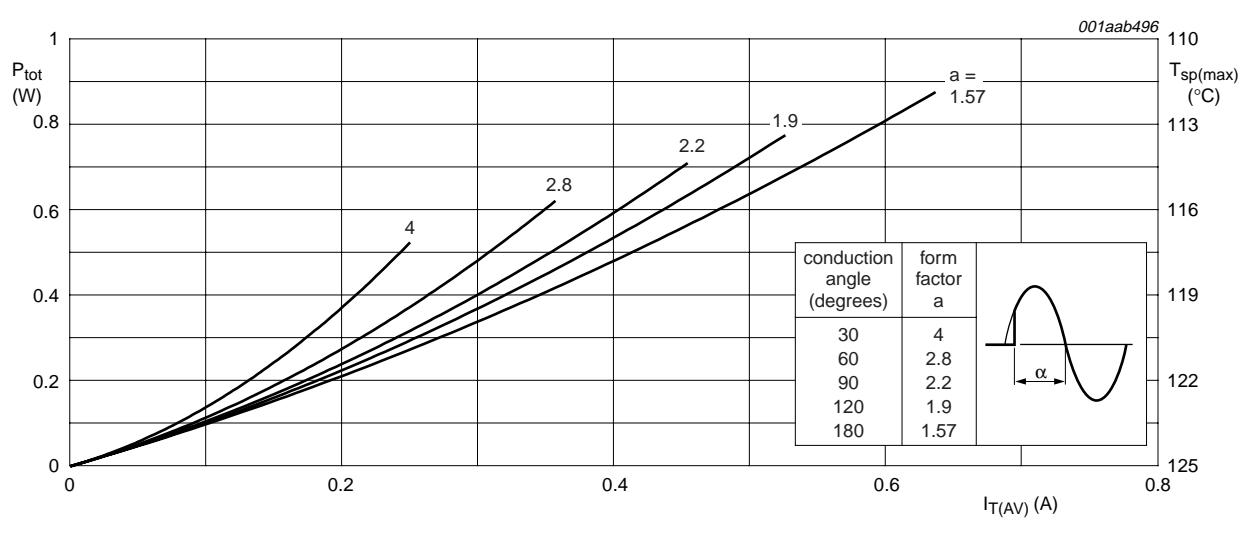
4. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

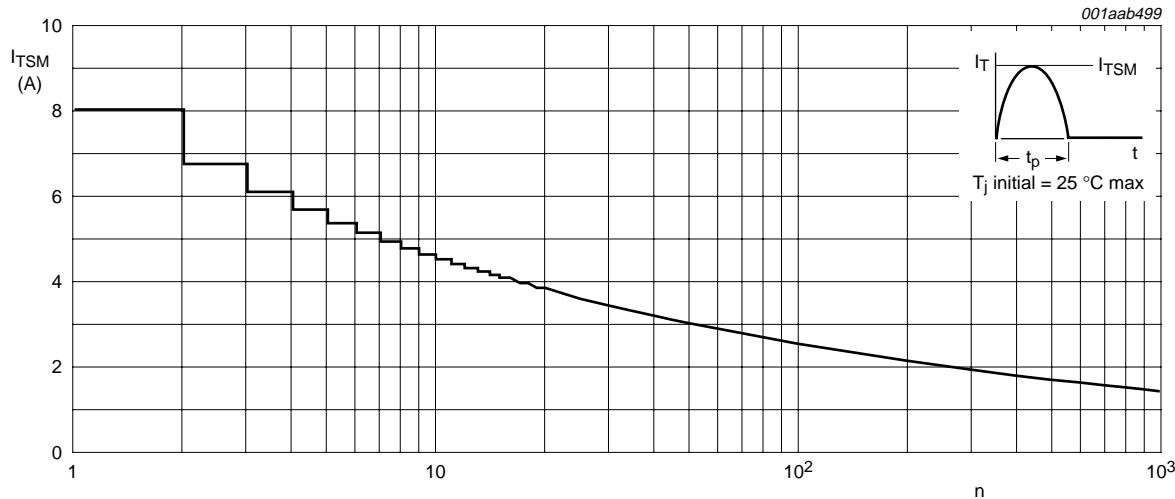
Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}, V_{RRM}	repetitive peak off-state voltage		[1]	-	600 V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{sp} \leq 112^\circ\text{C}$; see Figure 1	-	0.63	A
$I_{T(RMS)}$	RMS on-state current	all conduction angles; see Figure 4 and 5	-	1	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_j = 25^\circ\text{C}$ prior to surge; see Figure 2 and 3			
		$t = 10 \text{ ms}$	-	8	A
		$t = 8.3 \text{ ms}$	-	9	A
I^2t	I^2t for fusing	$t = 10 \text{ ms}$	-	0.32	A^2s
dI_T/dt	repetitive rate of rise of on-state current after triggering	$I_{TM} = 2 \text{ A}; I_G = 10 \text{ mA}; dI_G/dt = 100 \text{ mA}/\mu\text{s}$	-	50	$\text{A}/\mu\text{s}$
I_{GM}	peak gate current		-	1	A
V_{GM}	peak gate voltage		-	5	V
V_{RGM}	peak reverse gate voltage		-	5	V
P_{GM}	peak gate power		-	2	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.1	W
T_{stg}	storage temperature		-40	+150	$^\circ\text{C}$
T_j	junction temperature		-	125	$^\circ\text{C}$

[1] Although not recommended, off-state voltages up to 800 V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/ μs .



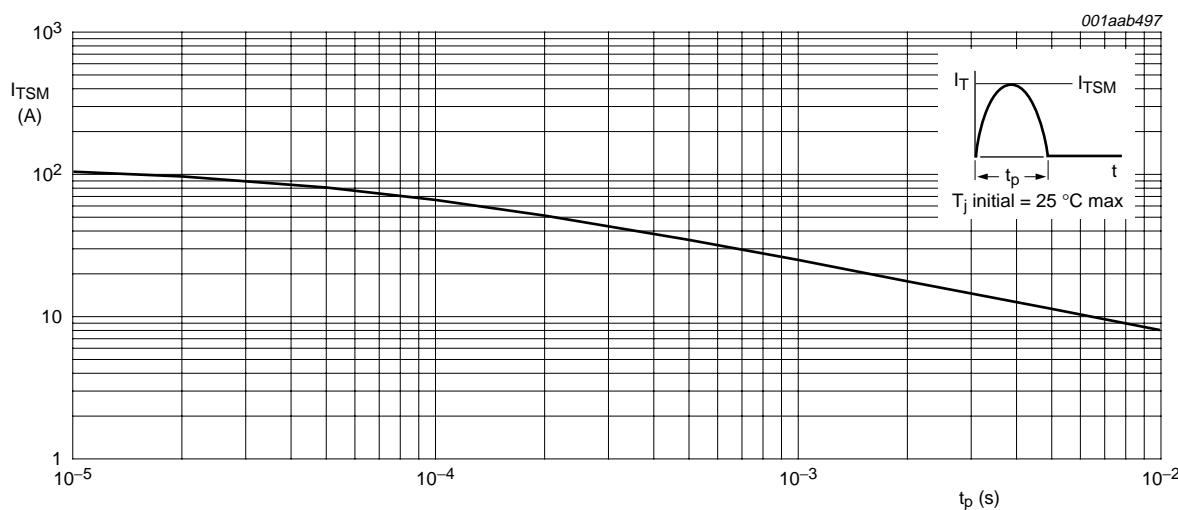
$$a = \text{form factor} = I_{T(RMS)} / I_{T(AV)}$$

Fig 1. Total power dissipation as a function of average on-state current; maximum values



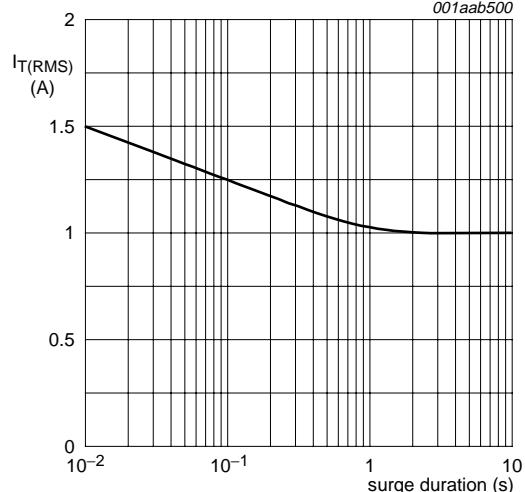
$f = 50$ Hz.

Fig 2. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



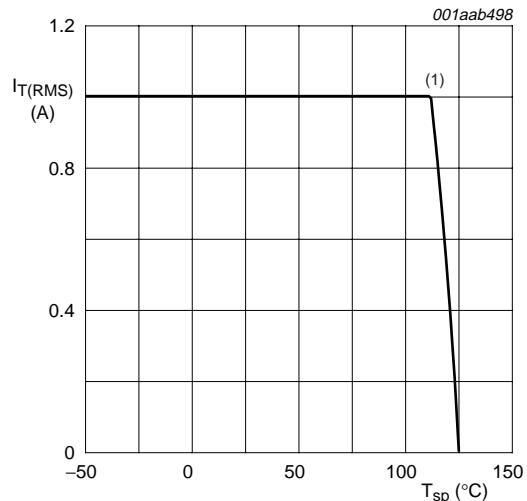
$t_p \leq 10$ ms.

Fig 3. Non-repetitive peak on-state current as a function of pulse width for sinusoidal currents; maximum values



$f = 50 \text{ Hz}; T_{sp} \leq 112 \text{ }^{\circ}\text{C}$.

Fig 4. RMS on-state current as a function of surge duration for sinusoidal currents; maximum values



(1) $T_{sp} = 112 \text{ }^{\circ}\text{C}$.

Fig 5. RMS on-state current as a function of solder point temperature; maximum values

5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	see Figure 6	-	-	15	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	printed-circuit board mounted, minimum footprint	-	156	-	K/W
		printed-circuit board mounted, pad area as in Figure 15	-	70	-	K/W

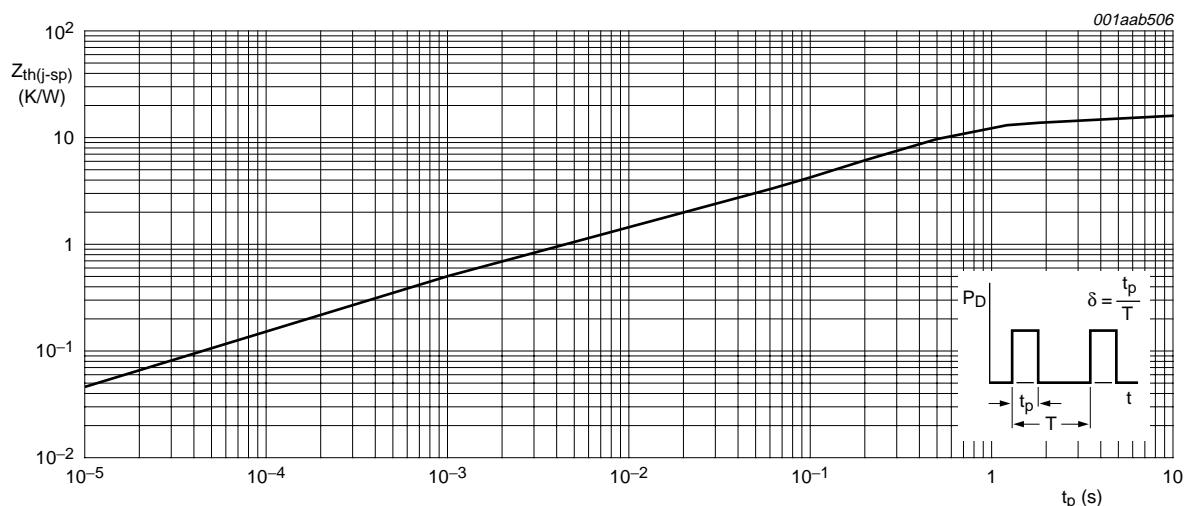
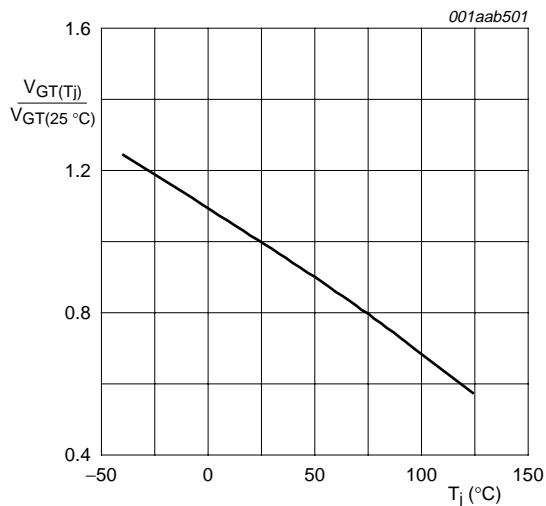
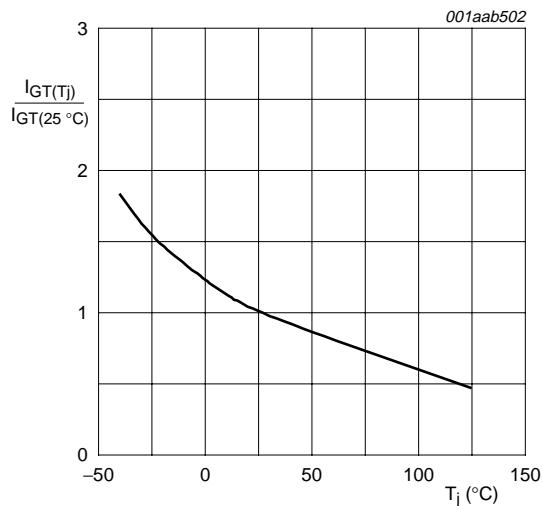


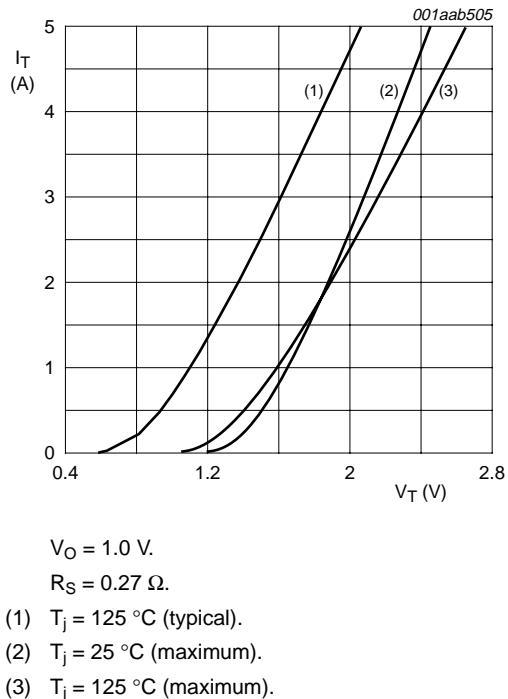
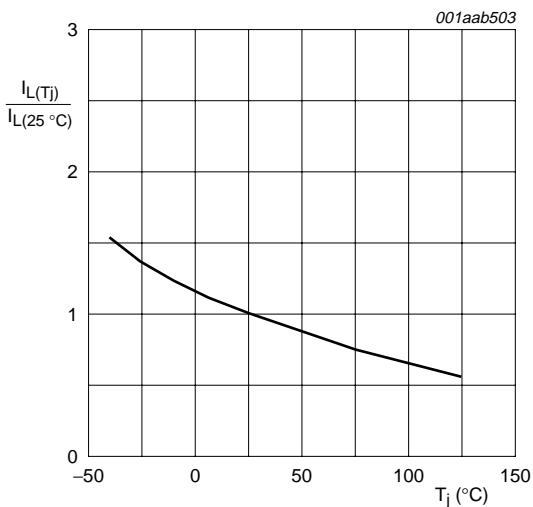
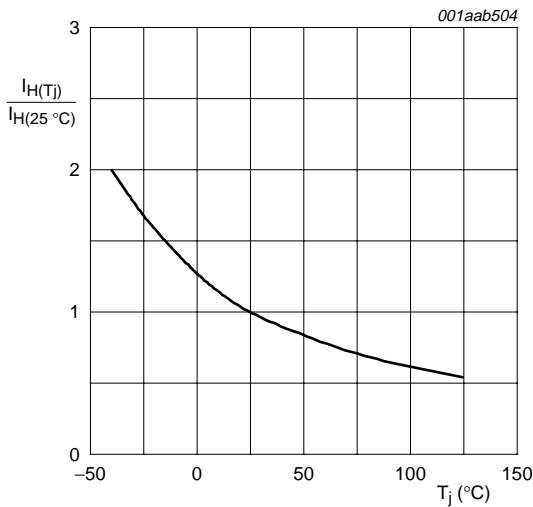
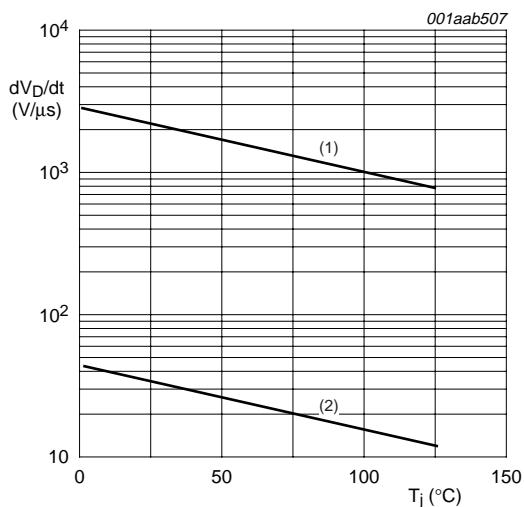
Fig 6. Transient thermal impedance from junction to solder point as a function of pulse duration

6. Characteristics

Table 5: Characteristics $T_j = 25^\circ\text{C}$; unless otherwise stated

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12 \text{ V}$; $I_T = 10 \text{ mA}$; gate open circuit; see Figure 8	20	50	200	μA
I_L	latching current	$V_D = 12 \text{ V}$; $I_{GT} = 0.5 \text{ mA}$; $R_{GK} = 1 \text{ k}\Omega$; see Figure 10	-	2	6	mA
I_H	holding current	$V_D = 12 \text{ V}$; $I_{GT} = 0.5 \text{ mA}$; $R_{GK} = 1 \text{ k}\Omega$; see Figure 11	-	2	5	mA
V_T	on-state voltage	$I_T = 1.2 \text{ A}$	-	1.25	1.7	V
V_{GT}	gate trigger voltage	$I_T = 10 \text{ mA}$; gate open circuit; see Figure 7				
		$V_D = 12 \text{ V}$	-	0.5	0.8	V
		$V_D = V_{DRM(\text{max})}$; $T_j = 125^\circ\text{C}$	0.2	0.3	-	V
I_D, I_R	off-state leakage current	$V_D = V_{DRM(\text{max})}$; $V_R = V_{RRM(\text{max})}$; $T_j = 125^\circ\text{C}$; $R_{GK} = 1 \text{ k}\Omega$	-	0.05	0.1	mA
Dynamic characteristics						
dV_D/dt	critical rate of rise of off-state voltage	$V_{DM} = 67\% V_{DRM(\text{max})}$; $T_j = 125^\circ\text{C}$; exponential waveform; see Figure 12				
		$R_{GK} = 1 \text{ k}\Omega$	500	800	-	$\text{V}/\mu\text{s}$
		gate open circuit	-	25	-	$\text{V}/\mu\text{s}$
t_{gt}	gate controlled turn-on time	$I_{TM} = 2 \text{ A}$; $V_D = V_{DRM(\text{max})}$; $I_G = 10 \text{ mA}$; $dI_G/dt = 0.1 \text{ A}/\mu\text{s}$	-	2	-	μs
t_q	circuit commuted turn-off time	$V_D = 67\% V_{DRM(\text{max})}$; $T_j = 125^\circ\text{C}$; $I_{TM} = 1.6 \text{ A}$; $V_R = 35 \text{ V}$; $dI_{TM}/dt = 30 \text{ A}/\mu\text{s}$; $dV_D/dt = 2 \text{ V}/\mu\text{s}$; $R_{GK} = 1 \text{ k}\Omega$	-	100	-	μs

**Fig 7. Normalized gate trigger voltage as a function of junction temperature****Fig 8. Normalized gate trigger current as a function of junction temperature**

**Fig 9. On-state current characteristics****Fig 10. Normalized latching current as a function of junction temperature****Fig 11. Normalized holding current as a function of junction temperature****Fig 12. Critical rate of rise of off-state voltage as a function of junction temperature; typical values**

7. Package information

Epoxy meets requirements of UL94 V-0 at $\frac{1}{8}$ inch.

8. Package outline

Plastic surface mounted package with increased heatsink; 4 leads

SOT223

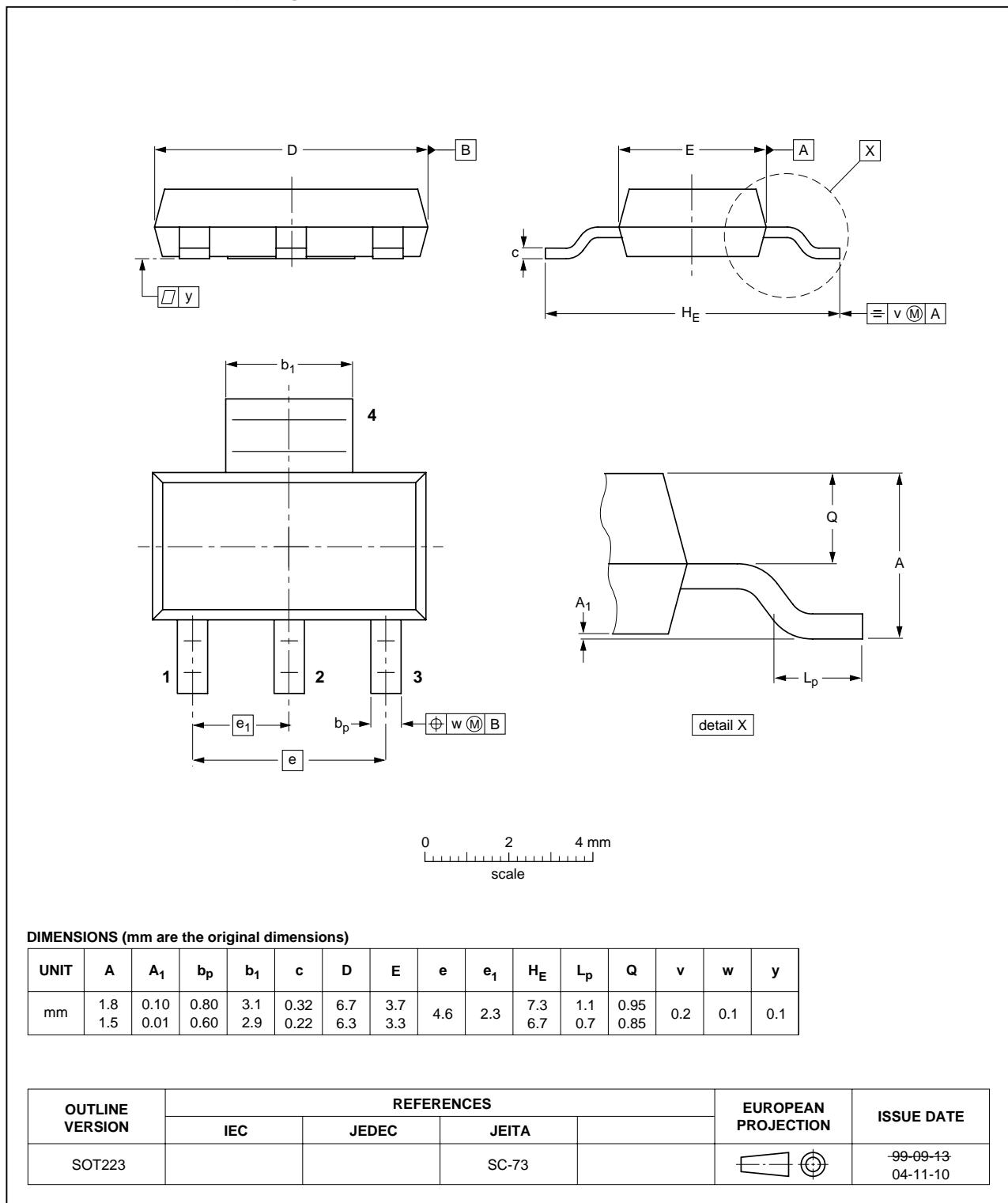
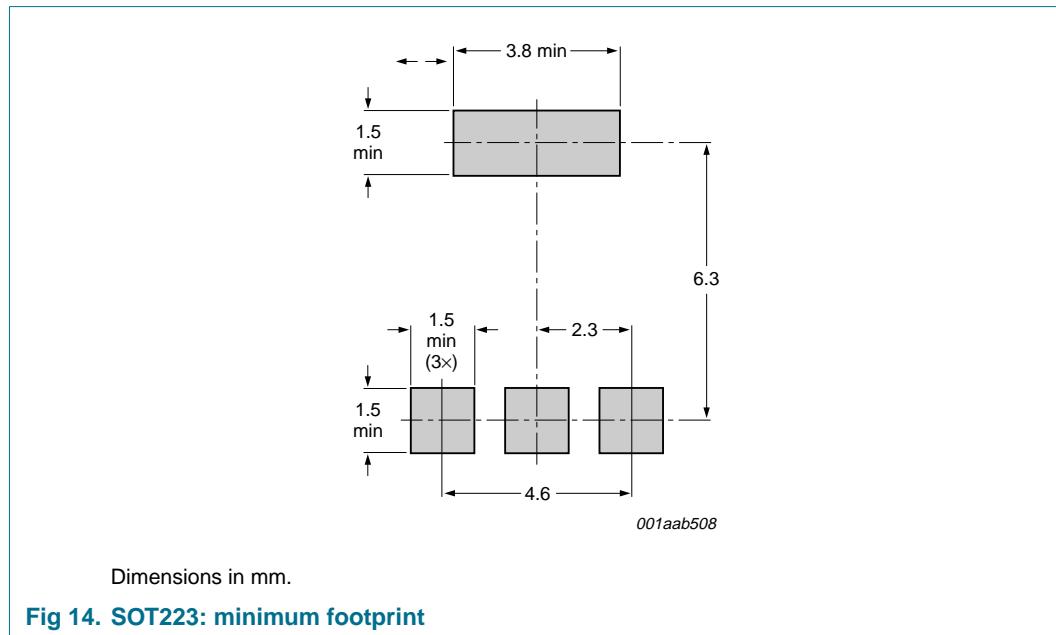


Fig 13. Package outline SOT223 (SC-73)

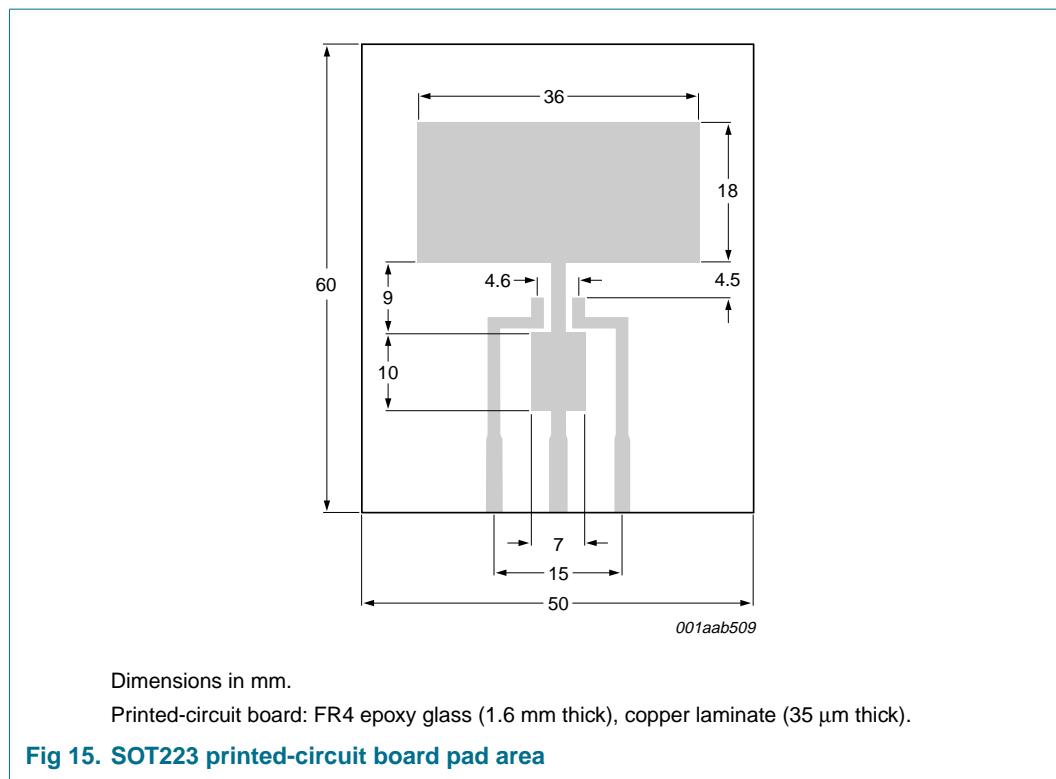


9. Mounting

9.1 Mounting instructions



9.2 Printed-circuit board





10. Revision history

Table 6: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
BT168GW_4	20041112	Product data sheet	-	9397 750 13509	BT168GW_3
Modifications:	<ul style="list-style-type: none">The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors.				
BT168GW_3	20010902	Product specification	-	n.a.	BT168W_series_2
BT168W_series_2	20010901	Product specification	-	n.a.	BT168W_series_1
BT168W_series_1	19970901	Product specification	-	n.a.	-

11. Data sheet status

Level	Data sheet status [1]	Product status [2][3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Date of release: 12 November 2004
Document number: 9397 750 13509



Published in The Netherlands