PML260SN

N-channel TrenchMOS standard level FET

Rev. 02 — 29 May 2006 | Product data sheet

1. Product profile

1.1 General description

Standard level N-channel enhancement mode Field-Effect Transistor (FET) in a surface-mounted plastic package using TrenchMOS technology.

1.2 Features

- Standard level threshold
- Very low thermal impedance
- Low profile and small footprint
- Low on-state resistance

1.3 Applications

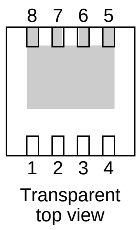
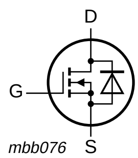
- Primary side switching
- Portable appliances
- DC-to-DC converters

1.4 Quick reference data

- $V_{DS} \leq 200$ V
- $R_{DSon} \leq 294$ mΩ
- $I_D \leq 8.8$ A
- $Q_{GD} = 4.2$ nC (typ)

2. Pinning information

Table 1. Pinning

Pin	Description	Simplified outline	Symbol
1, 2, 3	source (S)	 SOT873-1 (HVSON8)	
4	gate (G)		
5, 6, 7, 8	drain (D)		

PHILIPS

3. Ordering information

Table 2. Ordering information

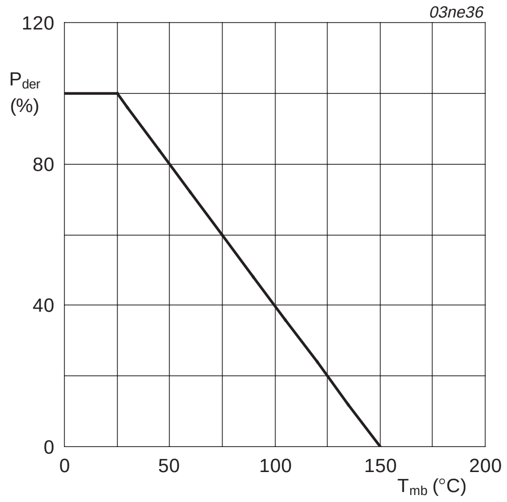
Type number	Package		
	Name	Description	Version
PML260SN	HVSON8	plastic thermal enhanced very thin small outline package; no leads; 8 terminals; body 3.3 × 3.3 × 0.85 mm	SOT873-1

4. Limiting values

Table 3. Limiting values

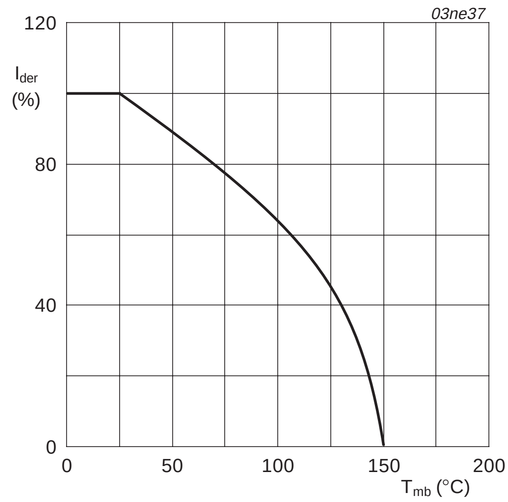
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 150 °C	-	200	V
V_{GS}	gate-source voltage		-	±20	V
I_D	drain current	T_{mb} = 25 °C; V_{GS} = 10 V; see Figure 2 and 3	-	8.8	A
		T_{mb} = 100 °C; V_{GS} = 10 V; see Figure 2	-	5.5	A
I_{DM}	peak drain current	T_{mb} = 25 °C; pulsed; t_p ≤ 10 µs; see Figure 3	-	15	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; see Figure 1	-	50	W
T_{stg}	storage temperature		–55	+150	°C
T_j	junction temperature		–55	+150	°C
Source-drain diode					
I_S	source current	T_{mb} = 25 °C	-	8.8	A
I_{SM}	peak source current	T_{mb} = 25 °C; pulsed; t_p ≤ 10 µs	-	15	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; I_D = 3.5 A; t_p = 0.05 ms; V_{DS} ≤ 200 V; R_{GS} = 50 Ω; V_{GS} = 10 V; starting at T_j = 25 °C	-	22	mJ



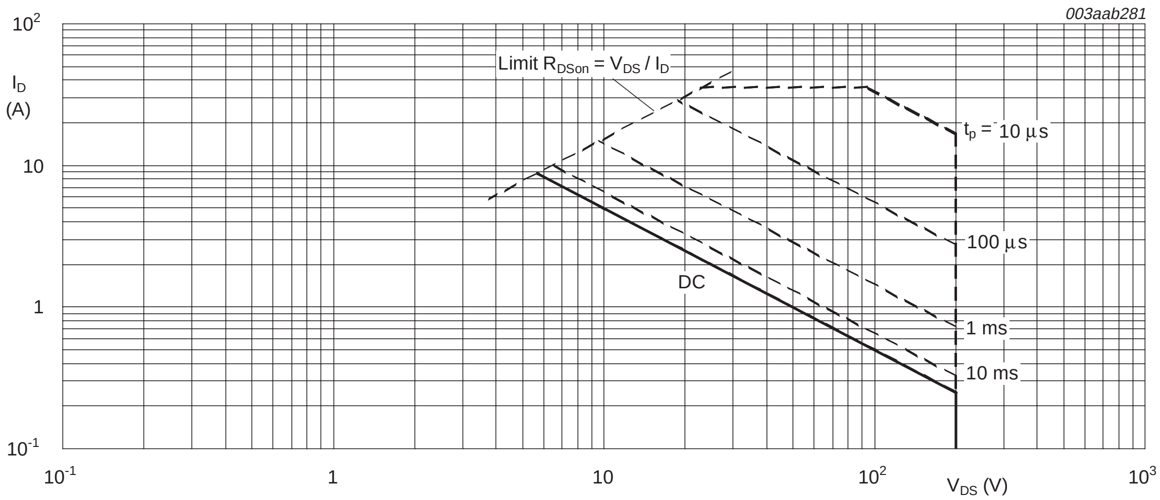
$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\ \%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature



$$I_{der} = \frac{I_D}{I_{D(25°C)}} \times 100\ \%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature



T_{mb} = 25 °C; I_{DM} is single pulse; V_{GS} = 10 V

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4		-	-	2.5	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint	[1]	-	60	-	K/W

[1] Mounted on a printed-circuit board; vertical in still air.

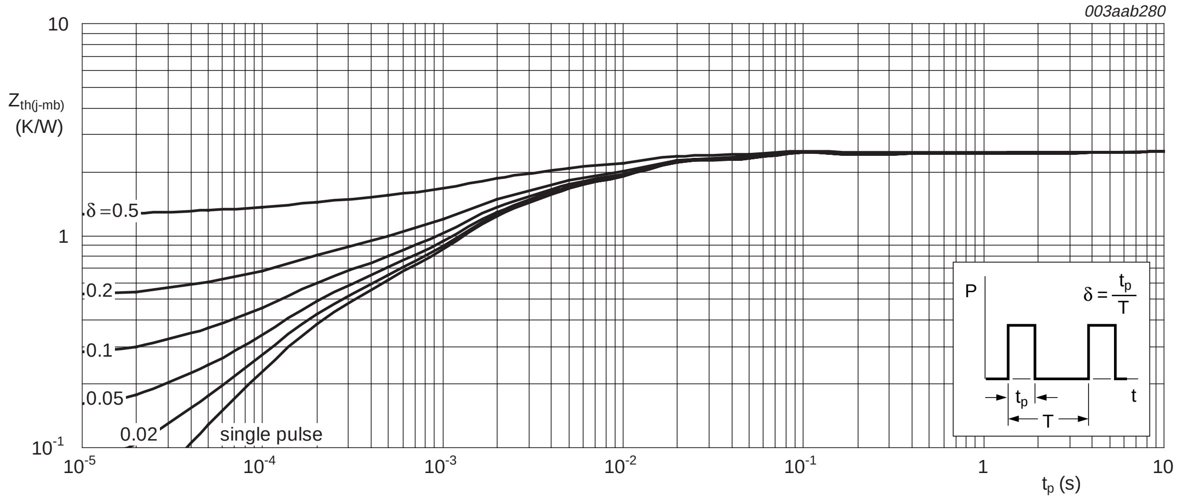


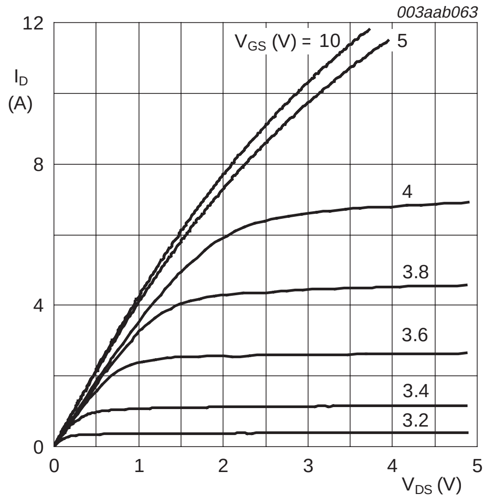
Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

Table 5. Characteristics

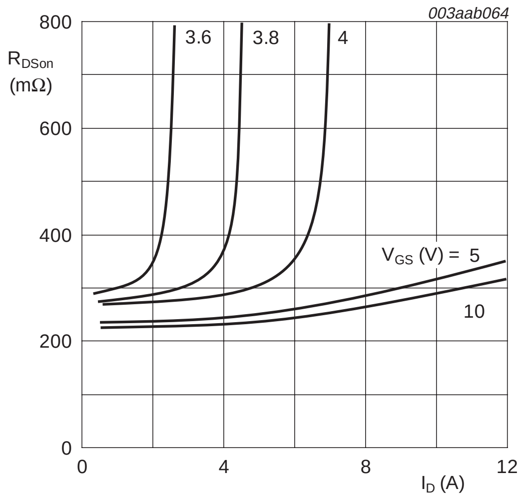
T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V				
		T_j = 25 °C	200	-	-	V
		T_j = –55 °C	178	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; see Figure 9 and 10				
		T_j = 25 °C	2	3	4	V
		T_j = 150 °C	1.2	-	-	V
		T_j = –55 °C	-	-	4.4	V
I_{DSS}	drain leakage current	V_{DS} = 160 V; V_{GS} = 0 V				
		T_j = 25 °C	-	-	1	µA
		T_j = 150 °C	-	-	100	µA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	-	10	100	nA
R_G	gate resistance	f = 1 MHz	-	0.6	-	Ω
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 2.6 A; see Figure 6 and 8				
		T_j = 25 °C	-	250	294	mΩ
		T_j = 150 °C	-	550	647	mΩ
		V_{GS} = 6 V; I_D = 2.5 A	-	263	309	mΩ
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	I_D = 2.6 A; V_{DS} = 100 V; V_{GS} = 10 V; see Figure 11 and 12	-	13.3	-	nC
Q_{GS}	gate-source charge		-	2.4	-	nC
Q_{GS1}	pre-$V_{GS(th)}$ gate-source charge		-	1.15	-	nC
Q_{GS2}	post-$V_{GS(th)}$ gate-source charge		-	1.25	-	nC
Q_{GD}	gate-drain charge		-	4.2	-	nC
$V_{GS(pl)}$	gate-source plateau voltage		-	4.2	-	V
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 30 V; f = 1 MHz; see Figure 14	-	657	-	pF
C_{oss}	output capacitance		-	74	-	pF
C_{rss}	reverse transfer capacitance		-	25	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 100 V; R_L = 100 Ω; V_{GS} = 10 V; R_G = 5.6 Ω	-	7	-	ns
t_r	rise time		-	11	-	ns
$t_{d(off)}$	turn-off delay time		-	19	-	ns
t_f	fall time		-	7	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	I_S = 3.2 A; V_{GS} = 0 V; see Figure 13	-	0.8	1.2	V
t_{rr}	reverse recovery time	I_S = 3.2 A; dI_S/dt = –100 A/µs; V_{GS} = 0 V; V_R = 120 V	-	101	-	ns
Q_r	recovered charge		-	267	-	nC



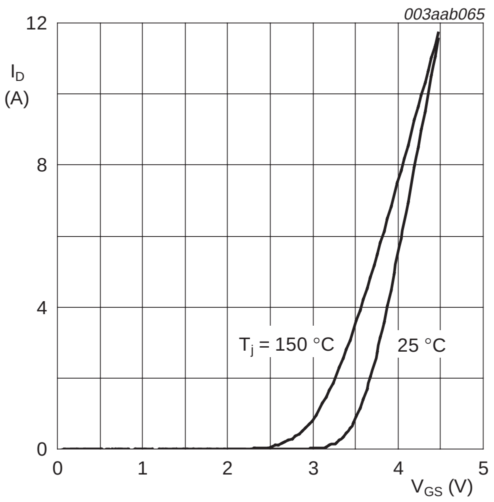
T_j = 25 °C

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



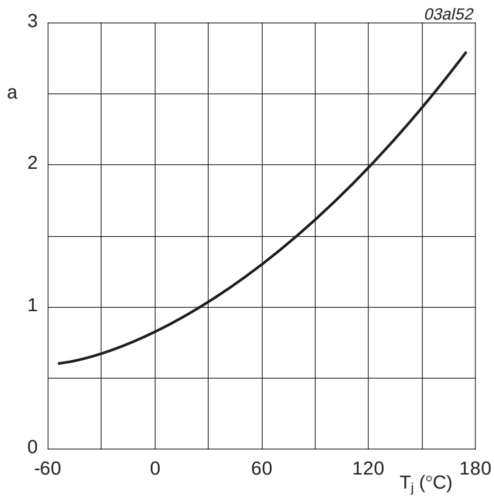
T_j = 25 °C

Fig 6. Drain-source on-state resistance as a function of drain current; typical values



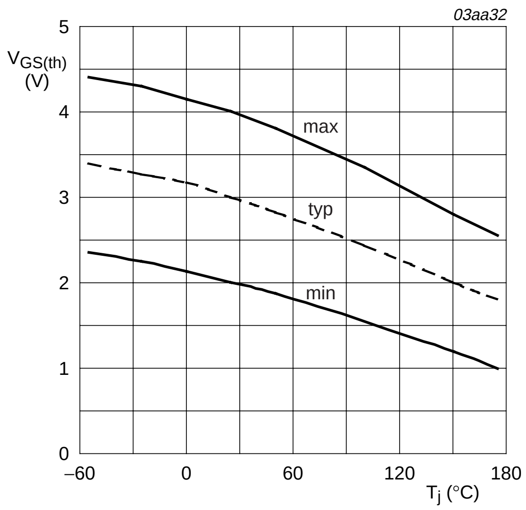
T_j = 25 °C and 150 °C; $V_{DS} > I_D \times R_{DSon}$

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values



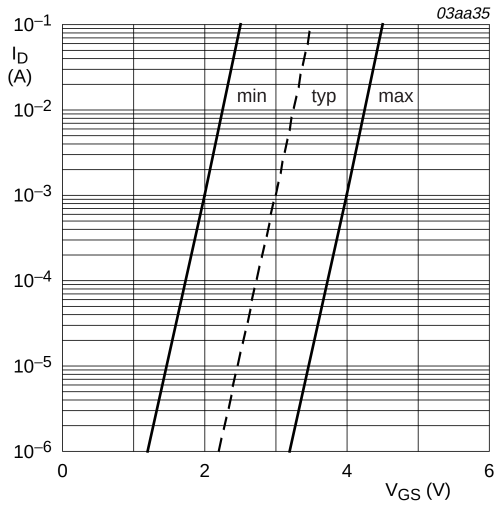
$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature



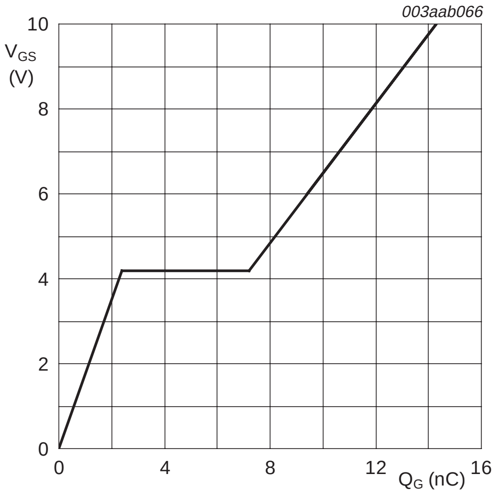
I_D = 1 mA; $V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature



T_j = 25 °C; V_{DS} = 5 V

Fig 10. Sub-threshold drain current as a function of gate-source voltage



I_D = 2.6 A; V_{DS} = 100 V

Fig 11. Gate-source voltage as a function of gate charge; typical values

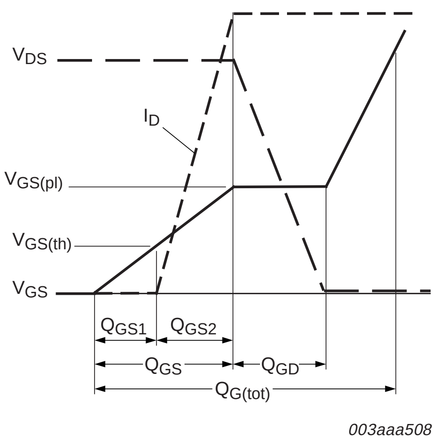
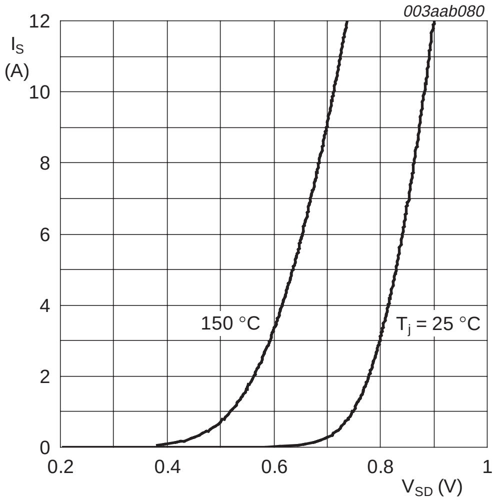
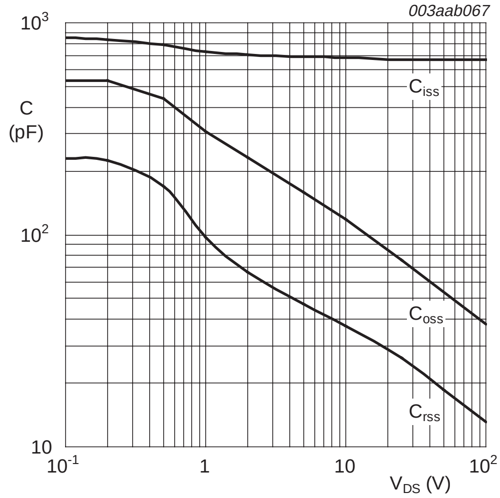


Fig 12. Gate charge waveform definitions



T_j = 25 °C and 150 °C; V_{GS} = 0 V

Fig 13. Source current as a function of source-drain voltage; typical values

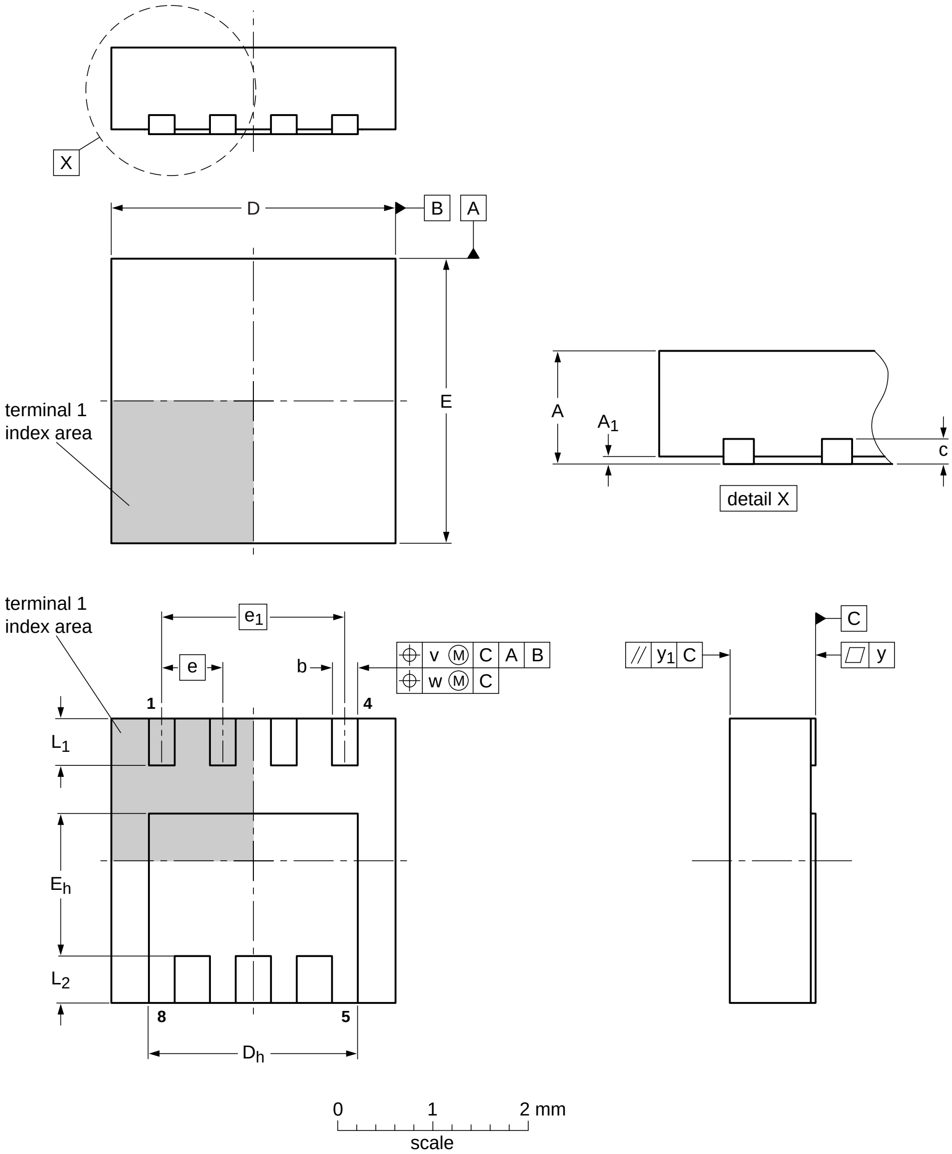


V_{GS} = 0 V; f = 1 MHz

Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

7. Package outline

HVSON8: plastic thermal enhanced very thin small outline package; no leads;
8 terminals; body 3.3 × 3.3 × 0.85 mm **SOT873-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	b	c	D	D_h	E	E_h	e	e_1	L_1	L_2	v	w	y	y_1
mm	1	0.05 0.00	0.35 0.25	0.2	3.4 3.2	2.3 2.2	3.4 3.2	1.68 1.58	0.65	1.95	0.55 0.45	0.52 0.42	0.1	0.05	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT873-1	- - -	- - -	- - -			~~05-06-16~~ 05-06-21

Fig 15. Package outline SOT873-1 (HVSON8)

8. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PML260SN_2	20060529	Product data sheet	-	PML260SN_1
Modifications:	• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors.			
PML260SN_1	20051222	Preliminary data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.semiconductors.philips.com.

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11. Contents

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