

# DATA SHEET

## **TDA8703**

**8-bit high-speed analog-to-digital  
converter**

Product specification  
Supersedes data of April 1993  
File under Integrated Circuits, IC02

1996 Aug 26

# 8-bit high-speed analog-to-digital converter

## TDA8703

### FEATURES

- 8-bit resolution
- Sampling rate up to 40 MHz
- High signal-to-noise ratio over a large analog input frequency range (7.1 effective bits at 4.43 MHz full-scale input)
- Binary or two's complement 3-state TTL outputs
- Overflow/underflow 3-state TTL output
- TTL compatible digital inputs
- Low-level AC clock input signal allowed
- Internal reference voltage generator
- Power dissipation only 290 mW (typical)
- Low analog input capacitance, no buffer amplifier required
- No sample-and-hold circuit required.

### APPLICATIONS

- General purpose high-speed analog-to-digital conversion
- Digital TV, IDTV
- Subscriber TV decoder
- Satellite TV decoders
- Digital VCR.

### GENERAL DESCRIPTION

The TDA8703 is an 8-bit high-speed Analog-to-Digital Converter (ADC) for video and other applications. It converts the analog input signal into 8-bit binary-coded digital words at a maximum sampling rate of 40 MHz. All digital inputs and outputs are TTL compatible, although a low-level AC clock input signal is allowed.

### ORDERING INFORMATION

| TYPE NUMBER | PACKAGE |  |          |
|-------------|---------|--|----------|
|             | NAME    | DESCRIPTION  | VERSION  |
| TDA8703     | DIP24   | plastic dual in-line package; 24 leads (600 mil)           | SOT101-1 |
| TDA8703T    | SO24    | plastic small outline package; 24 leads; body width 7.5 mm | SOT137-1 |

## 8-bit high-speed analog-to-digital converter

TDA8703

## QUICK REFERENCE DATA

| SYMBOL                             | PARAMETER                       | CONDITIONS                        | MIN. | TYP. | MAX. | UNIT |
|------------------------------------|---------------------------------|-----------------------------------|------|------|------|------|
| V <sub>CCA</sub>                   | analog supply voltage           |                                   | 4.5  | 5.0  | 5.5  | V    |
| V <sub>CCD</sub>                   | digital supply voltage          |                                   | 4.5  | 5.0  | 5.5  | V    |
| V <sub>CCO</sub>                   | output stages supply voltage    |                                   | 4.2  | 5.0  | 5.5  | V    |
| I <sub>CCA</sub>                   | analog supply current           |                                   | –    | 28   | 36   | mA   |
| I <sub>CCD</sub>                   | digital supply current          |                                   | –    | 19   | 25   | mA   |
| I <sub>CCO</sub>                   | output stages supply current    |                                   | –    | 11   | 14   | mA   |
| ILE                                | DC integral linearity error     |                                   | –    | –    | ±1   | LSB  |
| DLE                                | DC differential linearity error |                                   | –    | –    | ±1/2 | LSB  |
| AILE                               | AC integral linearity error     | note 1                            | –    | –    | ±2   | LSB  |
| B                                  | –3 dB bandwidth                 | note 2; f <sub>CLK</sub> = 40 MHz | –    | 19.5 | –    | MHz  |
| f <sub>CLK</sub> /f <sub>CLK</sub> | maximum conversion rate         | note 3                            | 40   | –    | –    | MHz  |
| P <sub>tot</sub>                   | total power dissipation         |                                   | –    | 290  | 415  | mW   |

## Notes

1. Full-scale sinewave (f<sub>i</sub> = 4.4 MHz; f<sub>CLK</sub>; f<sub>CLK</sub> = 27 MHz).
2. The –3 dB bandwidth is determined by the 3 dB reduction in the reconstructed output (full-scale signal at input).
3. The circuit has two clock inputs CLK and  $\overline{\text{CLK}}$ . There are four modes of operation:
  - a) TTL (mode 1);  $\overline{\text{CLK}}$  decoupled to DGND by a capacitor. CLK input is TTL threshold voltage of 1.5 V and sampling on the LOW-to-HIGH transition of the input clock signal.
  - b) TTL (mode 2); CLK decoupled to DGND by a capacitor.  $\overline{\text{CLK}}$  input is TTL threshold voltage of 1.5 V and sampling on the HIGH-to-LOW transition of the input clock signal.
  - c) AC drive modes (modes 3 and 4); When driving the CLK input directly and with any AC signal of 0.5 V (peak-to-peak value) imposed on a DC level of 1.5 V, sampling takes place on the LOW-to-HIGH transition of the clock signal. When driving the  $\overline{\text{CLK}}$  input with such a signal, sampling takes place on the HIGH-to-LOW transition.
  - d) If one of the clock inputs is not driven, then it is recommended to decouple this input to DGND with a 100 nF capacitor.

# 8-bit high-speed analog-to-digital converter

# TDA8703

## BLOCK DIAGRAM

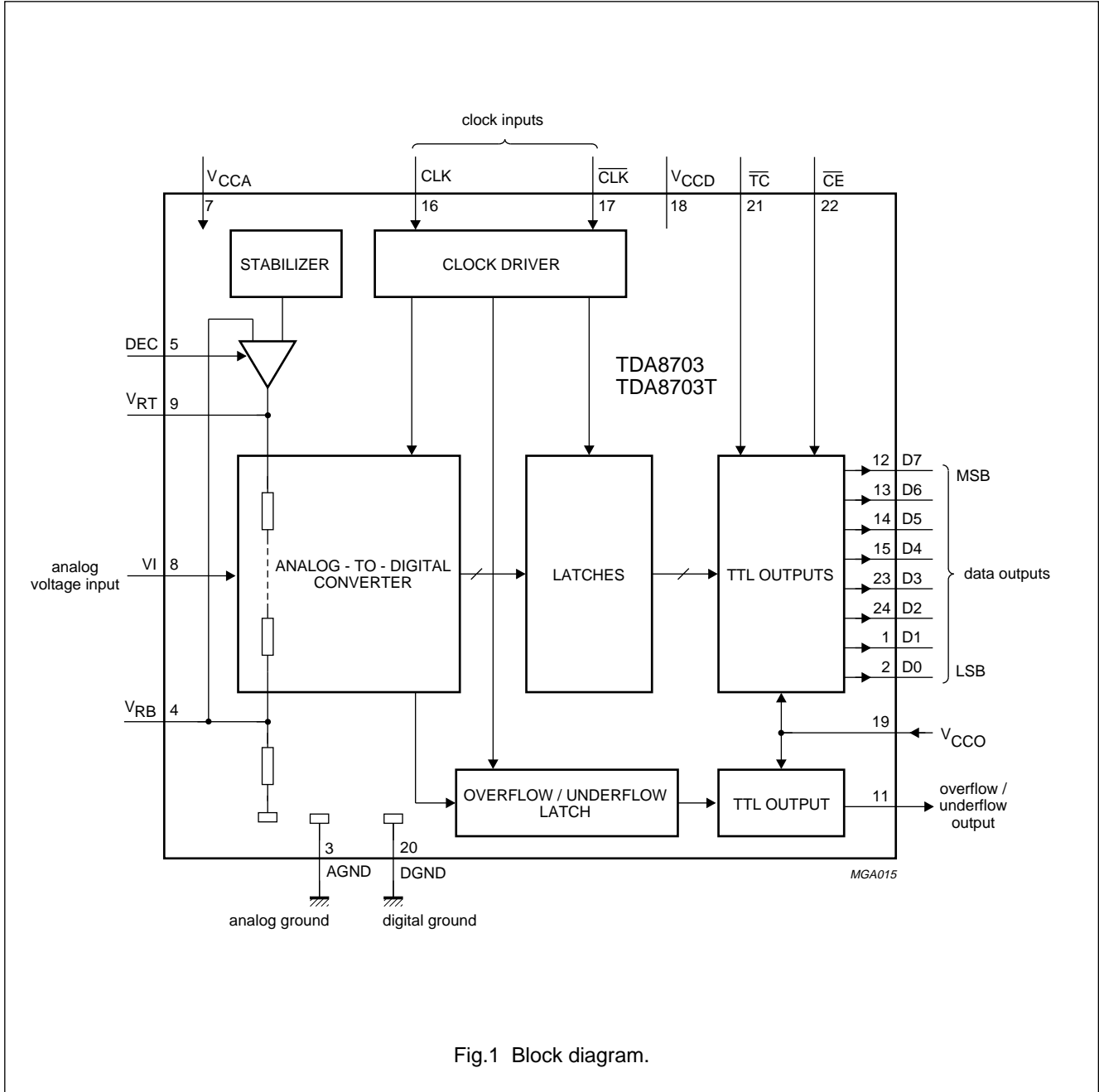


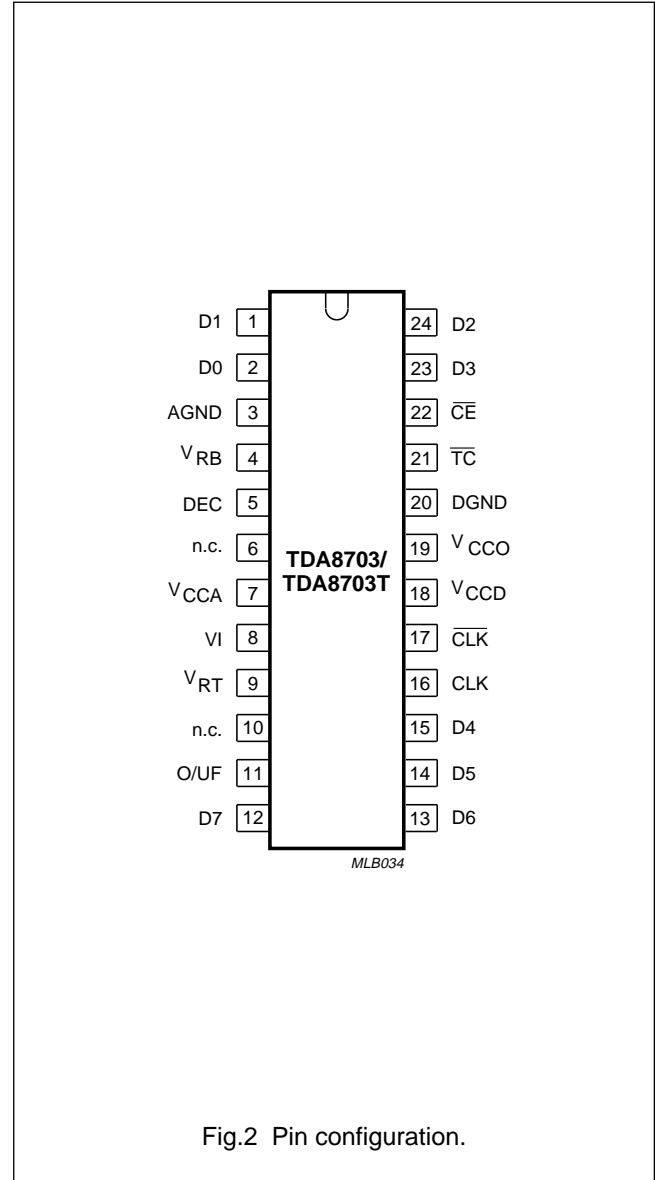
Fig.1 Block diagram.

8-bit high-speed analog-to-digital converter

TDA8703

**PINNING**

| SYMBOL           | PIN | DESCRIPTION   |
|------------------|-----|---|
| D1               | 1   | data output; bit 1  |
| D0               | 2   | data output; bit 0 (LSB)  |
| AGND             | 3   | analog ground   |
| V <sub>RB</sub>  | 4   | reference voltage bottom (decoupling)                           |
| DEC              | 5   | decoupling input (internal stabilization loop decoupling)       |
| n.c.             | 6   | not connected   |
| V <sub>CCA</sub> | 7   | positive supply voltage for analog circuits (+5 V)              |
| VI               | 8   | analog voltage input  |
| V <sub>RT</sub>  | 9   | reference voltage top (decoupling)                              |
| n.c.             | 10  | not connected   |
| O/UF             | 11  | overflow/underflow data output                                  |
| D7               | 12  | data output; bit 7 (MSB)  |
| D6               | 13  | data output; bit 6  |
| D5               | 14  | data output; bit 5  |
| D4               | 15  | data output; bit 4  |
| CLK              | 16  | clock input   |
| CLK              | 17  | complementary clock input                                       |
| V <sub>CCD</sub> | 18  | positive supply voltage for digital circuits (+5 V)             |
| V <sub>CCO</sub> | 19  | positive supply voltage for output stages (+5 V)                |
| DGND             | 20  | digital ground  |
| TC               | 21  | input for two's complement output (TTL level input, active LOW) |
| CE               | 22  | chip enable input (TTL level input, active LOW)                 |
| D3               | 23  | data output; bit 3  |
| D2               | 24  | data output; bit 2  |



## 8-bit high-speed analog-to-digital converter

TDA8703

**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 134).

| SYMBOL                       | PARAMETER   | CONDITIONS                 | MIN. | MAX. | UNIT |
|------------------------------|---|----------------------------|------|------|------|
| $V_{CCA}$                    | analog supply voltage                               |                            | -0.3 | +7.0 | V    |
| $V_{CCD}$                    | digital supply voltage                              |                            | -0.3 | +7.0 | V    |
| $V_{CCO}$                    | output stages supply voltage                        |                            | -0.3 | +7.0 | V    |
| $V_{CCA} - V_{CCD}$          | supply voltage differences                          |                            | -1.0 | +1.0 | V    |
| $V_{CCO} - V_{CCD}$          | supply voltage differences                          |                            | -1.0 | +1.0 | V    |
| $V_{CCA} - V_{CCO}$          | supply voltage differences                          |                            | -1.0 | +1.0 | V    |
| $V_{VI}$                     | input voltage range                                 | referenced to AGND         | -0.3 | +7.0 | V    |
| $V_{CLK}/V_{\overline{CLK}}$ | AC input voltage for switching (peak-to-peak value) | note 1; referenced to DGND | -    | 2.0  | V    |
| $I_o$                        | output current                                      |                            | -    | +10  | mA   |
| $T_{stg}$                    | storage temperature                                 |                            | -55  | +150 | °C   |
| $T_{amb}$                    | operating ambient temperature                       |                            | 0    | +70  | °C   |
| $T_j$                        | junction temperature                                |                            | -    | +125 | °C   |

**Notes**

- The circuit has two clock inputs CLK and  $\overline{CLK}$ . There are four modes of operation:
  - TTL (mode 1);  $\overline{CLK}$  decoupled to DGND by a capacitor. CLK input is TTL threshold voltage of 1.5 V and sampling on the LOW-to-HIGH transition of the input clock signal.
  - TTL (mode 2); CLK decoupled to DGND by a capacitor.  $\overline{CLK}$  input is TTL threshold voltage of 1.5 V and sampling on the HIGH-to-LOW transition of the input clock signal.
  - AC drive modes (modes 3 and 4); When driving the CLK input directly and with any AC signal of 0.5 V (peak-to-peak value) imposed on a DC level of 1.5 V, sampling takes place on the LOW-to-HIGH transition of the clock signal. When driving the  $\overline{CLK}$  input with such a signal, sampling takes place on the HIGH-to-LOW transition.
  - If one of the clock inputs is not driven, then it is recommended to decouple this input to DGND with a 100 nF capacitor.

**HANDLING**

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

**THERMAL RESISTANCE**

| SYMBOL        | PARAMETER                            | VALUE | UNIT |
|---------------|--------------------------------------|-------|------|
| $R_{th\ j-a}$ | from junction to ambient in free air |       |      |
|               | SOT101-1                             | 55    | K/W  |
|               | SOT137-1                             | 75    | K/W  |

## 8-bit high-speed analog-to-digital converter

TDA8703

**CHARACTERISTICS**

$V_{CCA} = V_7 - V_3 = 4.5 \text{ V to } 5.5 \text{ V}$ ;  $V_{CCD} = V_{18} - V_{20} = 4.5 \text{ V to } 5.5 \text{ V}$ ;  $V_{CCO} = V_{19} - V_{20} = 4.5 \text{ V to } 5.5 \text{ V}$ ; AGND and DGND shorted together;  $V_{CCA} - V_{CCD} = -0.5 \text{ V to } +0.5 \text{ V}$ ;  $V_{CCO} - V_{CCD} = -0.5 \text{ V to } +0.5 \text{ V}$ ;  
 $V_{CCA} - V_{CCD} = -0.5 \text{ V to } +0.5 \text{ V}$ ;  $T_{amb} = 0 \text{ }^\circ\text{C to } +70 \text{ }^\circ\text{C}$ ; unless otherwise specified (typical values measured at  $V_{CCA} = V_{CCD} = V_{CCO} = 5 \text{ V}$  and  $T_{amb} = 25 \text{ }^\circ\text{C}$ ).

| SYMBOL   | PARAMETER   | CONDITIONS  | MIN.  | TYP. | MAX.      | UNIT          |
|--|---|---|-------|------|-----------|---------------|
| <b>Supply</b>  |   |   |       |      |           |               |
| $V_{CCA}$  | analog supply voltage                               |   | 4.5   | 5.0  | 5.5       | V             |
| $V_{CCD}$  | digital supply voltage                              |   | 4.5   | 5.0  | 5.5       | V             |
| $V_{CCO}$  | output stages supply voltage                        |   | 4.2   | 5.0  | 5.5       | V             |
| $I_{CCA}$  | analog supply current                               |   | –     | 28   | 36        | mA            |
| $I_{CCD}$  | digital supply current                              |   | –     | 19   | 25        | mA            |
| $I_{CCO}$  | output stage supply current                         | all outputs LOW   | –     | 11   | 14        | mA            |
| <b>Inputs</b>  |   |   |       |      |           |               |
| CLOCK INPUT $\overline{\text{CLK}}$ AND CLK (note 1; REFERENCED TO DGND) |   |   |       |      |           |               |
| $V_{IL}$   | LOW level input voltage                             |   | 0     | –    | 0.8       | V             |
| $V_{IH}$   | HIGH level input voltage                            |   | 2.0   | –    | $V_{CCD}$ | V             |
| $I_{IL}$   | LOW level input current                             | $V_{\text{CLK}}/V_{\overline{\text{CLK}}} = 0.4 \text{ V}$  | –400  | –    | –         | $\mu\text{A}$ |
| $I_{IH}$   | HIGH level input current                            | $V_{\text{CLK}}/V_{\overline{\text{CLK}}} = 0.4 \text{ V}$  | –     | –    | 100       | $\mu\text{A}$ |
|  |   | $V_{\text{CLK}}/V_{\overline{\text{CLK}}} = V_{CCD}$        | –     | –    | 300       | $\mu\text{A}$ |
| $Z_i$  | input impedance                                     | $f_{\text{CLK}}/f_{\overline{\text{CLK}}} = 10 \text{ MHz}$ | –     | 4    | –         | k $\Omega$    |
| $C_i$  | input capacitance                                   | $f_{\text{CLK}}/f_{\overline{\text{CLK}}} = 10 \text{ MHz}$ | –     | 4.5  | –         | pF            |
| $V_{\text{CLK}} - V_{\overline{\text{CLK}}}$                             | AC input voltage for switching (peak-to-peak value) | note 1; DC level = 1.5 V                                    | 0.5   | –    | 2.0       | V             |
| $\overline{\text{TC}}$ AND $\overline{\text{CE}}$ (REFERENCED TO DGND)   |   |   |       |      |           |               |
| $V_{IL}$   | LOW level input voltage                             |   | 0     | –    | 0.8       | V             |
| $V_{IH}$   | HIGH level input voltage                            |   | 2.0   | –    | $V_{CCD}$ | V             |
| $I_{IL}$   | LOW level input current                             | $V_{IL} = 0.4 \text{ V}$                                    | –400  | –    | –         | $\mu\text{A}$ |
| $I_{IH}$   | HIGH level input current                            | $V_{IH} = 2.7 \text{ V}$                                    | –     | –    | 20        | $\mu\text{A}$ |
| VI (ANALOG INPUT VOLTAGE REFERENCED TO AGND)                             |   |   |       |      |           |               |
| $V_{VI(B)}$  | input voltage (bottom)                              |   | 1.33  | 1.41 | 1.48      | V             |
| $V_{VI(0)}$  | input voltage                                       | output code = 0   | 1.455 | 1.55 | 1.635     | V             |
| $V_{OS(B)}$  | offset voltage (bottom)                             | $V_{VI(0)} - V_{VI(B)}$                                     | 0.125 | –    | 0.155     | V             |
| $V_{VI(T)}$  | input voltage (top)                                 |   | 3.2   | 3.36 | 3.5       | V             |
| $V_{VI(255)}$  | input voltage                                       | output code = 255   | 3.115 | 3.26 | 3.385     | V             |
| $V_{OS(T)}$  | offset voltage (top)                                | $V_{VI(T)} - V_{VI(255)}$                                   | 0.085 | –    | 0.115     | V             |
| $V_{VI(p-p)}$  | input voltage amplitude (peak-to-peak value)        |   | 1.66  | 1.71 | 1.75      | V             |
| $I_{IL}$   | LOW level input current                             | $V_{VI} = 1.4 \text{ V}$                                    | –     | 0    | –         | $\mu\text{A}$ |
| $I_{IH}$   | HIGH level input current                            | $V_{VI} = 3.6 \text{ V}$                                    | 60    | 120  | 180       | $\mu\text{A}$ |
| $Z_i$  | input impedance                                     | $f_i = 1 \text{ MHz}$                                       | –     | 10   | –         | k $\Omega$    |
| $C_i$  | input capacitance                                   | $f_i = 1 \text{ MHz}$                                       | –     | 14   | –         | pF            |

## 8-bit high-speed analog-to-digital converter

TDA8703

| SYMBOL  | PARAMETER                              | CONDITIONS                  | MIN. | TYP. | MAX.      | UNIT     |
|---|--|-----------------------------|------|------|-----------|----------|
| <b>Reference resistance</b>                                     |  |                             |      |      |           |          |
| $R_{ref}$   | reference resistance                   | $V_{RT}$ to $V_{RB}$        | –    | 220  | –         | $\Omega$ |
| <b>Outputs</b>  |  |                             |      |      |           |          |
| DIGITAL OUTPUTS (D7 - D0) (REFERENCED TO DGND)                  |  |                             |      |      |           |          |
| $V_{OL}$  | LOW level output voltage               | $I_O = 1$ mA                | 0    | –    | 0.4       | V        |
| $V_{OH}$  | HIGH level output voltage              | $I_O = -0.4$ mA             | 2.7  | –    | $V_{CCD}$ | V        |
| $I_{OZ}$  | output current in 3-state mode         | $0.4$ V < $V_O$ < $V_{CCD}$ | –20  | –    | +20       | $\mu$ A  |
| <b>Switching characteristics</b> (note 2; see Fig.3)            |  |                             |      |      |           |          |
| $f_{CLK}/f_{\overline{CLK}}$                                    | maximum clock frequency                |                             | 40   | –    | –         | MHz      |
| <b>Analog signal processing (<math>f_{CLK} = 40</math> MHz)</b> |  |                             |      |      |           |          |
| B   | –3 dB bandwidth                        | note 3                      | –    | 19.5 | –         | MHz      |
| $G_d$   | differential gain                      | note 4                      | –    | 0.6  | –         | %        |
| $\phi_d$  | differential phase                     | note 4                      | –    | 0.8  | –         | deg      |
| $f_1$   | fundamental harmonics (full-scale)     | $f_i = 4.43$ MHz            | –    | –    | 0         | dB       |
| $f_{all}$   | harmonics (full-scale), all components | $f_i = 4.43$ MHz            | –    | –55  | –         | dB       |
| SVRR1   | supply voltage ripple rejection        | note 5                      | –    | –28  | –25       | dB       |
| SVRR2   | supply voltage ripple rejection        | note 5                      | –    | 1    | 2.5       | %/V      |
| <b>Transfer function</b>  |  |                             |      |      |           |          |
| ILE   | DC integral linearity error            |                             | –    | –    | $\pm 1$   | LSB      |
| DLE   | DC differential linearity error        |                             | –    | –    | $\pm 1/2$ | LSB      |
| AILE  | AC integral linearity error            | note 6                      | –    | –    | $\pm 2$   | LSB      |
| EB  | effective bits                         | $f_i = 4.43$ MHz            | –    | 7.1  | –         | bits     |
| <b>Timing</b> (note 7; see Figs 3 to 6; $f_{CLK} = 40$ MHz)     |  |                             |      |      |           |          |
| $t_{dS}$  | sampling delay                         |                             | –    | –    | 2         | ns       |
| $t_{HD}$  | output hold time                       |                             | 6    | –    | –         | ns       |
| $t_{dLH}$   | output delay time                      | LOW-to-HIGH transition      | –    | 8    | 10        | ns       |
| $t_{dHL}$   | output delay time                      | HIGH-to-LOW transition      | –    | 16   | 20        | ns       |
| $t_{dZH}$   | 3-state output delay times             | enable-to-HIGH              | –    | 19   | 25        | ns       |
| $t_{dZL}$   | 3-state output delay times             | enable-to-LOW               | –    | 16   | 20        | ns       |
| $t_{dHZ}$   | 3-state output delay times             | disable-to-HIGH             | –    | 14   | 20        | ns       |
| $t_{dLZ}$   | 3-state output delay times             | disable-to-LOW              | –    | 9    | 12        | ns       |



## 8-bit high-speed analog-to-digital converter

TDA8703

**Notes**

1. The circuit has two clock inputs CLK and  $\overline{\text{CLK}}$ . There are four modes of operation:
  - a) TTL (mode 1);  $\overline{\text{CLK}}$  decoupled to DGND by a capacitor. CLK input is TTL threshold voltage of 1.5 V and sampling on the LOW-to-HIGH transition of the input clock signal.
  - b) TTL (mode 2); CLK decoupled to DGND by a capacitor.  $\overline{\text{CLK}}$  input is TTL threshold voltage of 1.5 V and sampling on the HIGH-to-LOW transition of the input clock signal.
  - c) AC drive modes (modes 3 and 4); When driving the CLK input directly and with any AC signal of 0.5 V (peak-to-peak value) imposed on a DC level of 1.5 V, sampling takes place on the LOW-to-HIGH transition of the clock signal. When driving the  $\overline{\text{CLK}}$  input with such a signal, sampling takes place on the HIGH-to-LOW transition.
  - d) If one of the clock inputs is not driven, then it is recommended to decouple this input to DGND with a 100 nF capacitor.
2. In addition to a good layout of the digital and analog ground, it is recommended that the rise and fall times of the clock must not be less than 2 ns.
3. The -3 dB bandwidth is determined by the 3 dB reduction in the reconstructed output (full-scale signal at the input).
4. Low frequency ramp signal ( $V_{VI(p-p)} = 1.8$  V and  $f_i = 15$  kHz) combined with a sinewave input voltage ( $V_{VI(p-p)} = 0.5$  V,  $f_i = 4.43$  MHz) at the input.
5. Supply voltage ripple rejection:
  - a) SVRR1; variation of the input voltage producing output code 127 for supply voltage variation of 1 V:  

$$\text{SVRR1} = 20 \log (\Delta V_{VI(127)} / \Delta V_{CCA})$$
  - b) SVRR2; relative variation of the full-scale range of analog input for a supply voltage variation of 1 V:  

$$\text{SVR2} = \{ \Delta (V_{VI(0)} - V_{VI(255)}) / (V_{VI(0)} - V_{VI(255)}) \} \div \Delta V_{CCA}$$
6. Full-scale sinewave ( $f_i = 4.4$  MHz;  $f_{\text{CLK}}$ ;  $f_{\overline{\text{CLK}}} = 27$  MHz).
7. Output data acquisition:
  - a) Output data is available after the maximum delay of  $t_{dHL}$  and  $t_{dLH}$ .

8-bit high-speed analog-to-digital converter

TDA8703

**Table 1** Output coding and input voltage (referenced to AGND; typical values)

| STEP      | $V_{VI(p-p)}$ | O/UF | BINARY OUTPUT BITS |    |    |    |    |    |    |    | TWO'S COMPLEMENT OUTPUT BITS |    |    |    |    |    |    |    |
|-----------|---------------|------|--------------------|----|----|----|----|----|----|----|------------------------------|----|----|----|----|----|----|----|
|           |               |      | D7                 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | D7                           | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Underflow | <1.55         | 1    | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1                            | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| 0         | 1.55          | 0    | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1                            | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| 1         | -             | 0    | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1                            | 0  | 0  | 0  | 0  | 0  | 0  | 1  |
| .         | .             | .    | .                  | .  | .  | .  | .  | .  | .  | .  | .                            | .  | .  | .  | .  | .  | .  | .  |
| .         | .             | .    | .                  | .  | .  | .  | .  | .  | .  | .  | .                            | .  | .  | .  | .  | .  | .  | .  |
| 254       | .             | 0    | 1                  | 1  | 1  | 1  | 1  | 1  | 1  | 0  | 0                            | 1  | 1  | 1  | 1  | 1  | 1  | 0  |
| 255       | 3.26          | 0    | 1                  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 0                            | 1  | 1  | 1  | 1  | 1  | 1  | 1  |
| Overflow  | >3.26         | 1    | 1                  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 0                            | 1  | 1  | 1  | 1  | 1  | 1  | 1  |

**Table 2** Mode selection

| $\overline{TC}$  | $\overline{CE}$ | D7-D0                    | O/UF           |
|------------------|-----------------|--------------------------|----------------|
| X <sup>(1)</sup> | 1               | high impedance           | high impedance |
| 0                | 0               | active; two's complement | active         |
| 1                | 0               | active; binary           | active         |

**Note**

- 1. X = don't care.

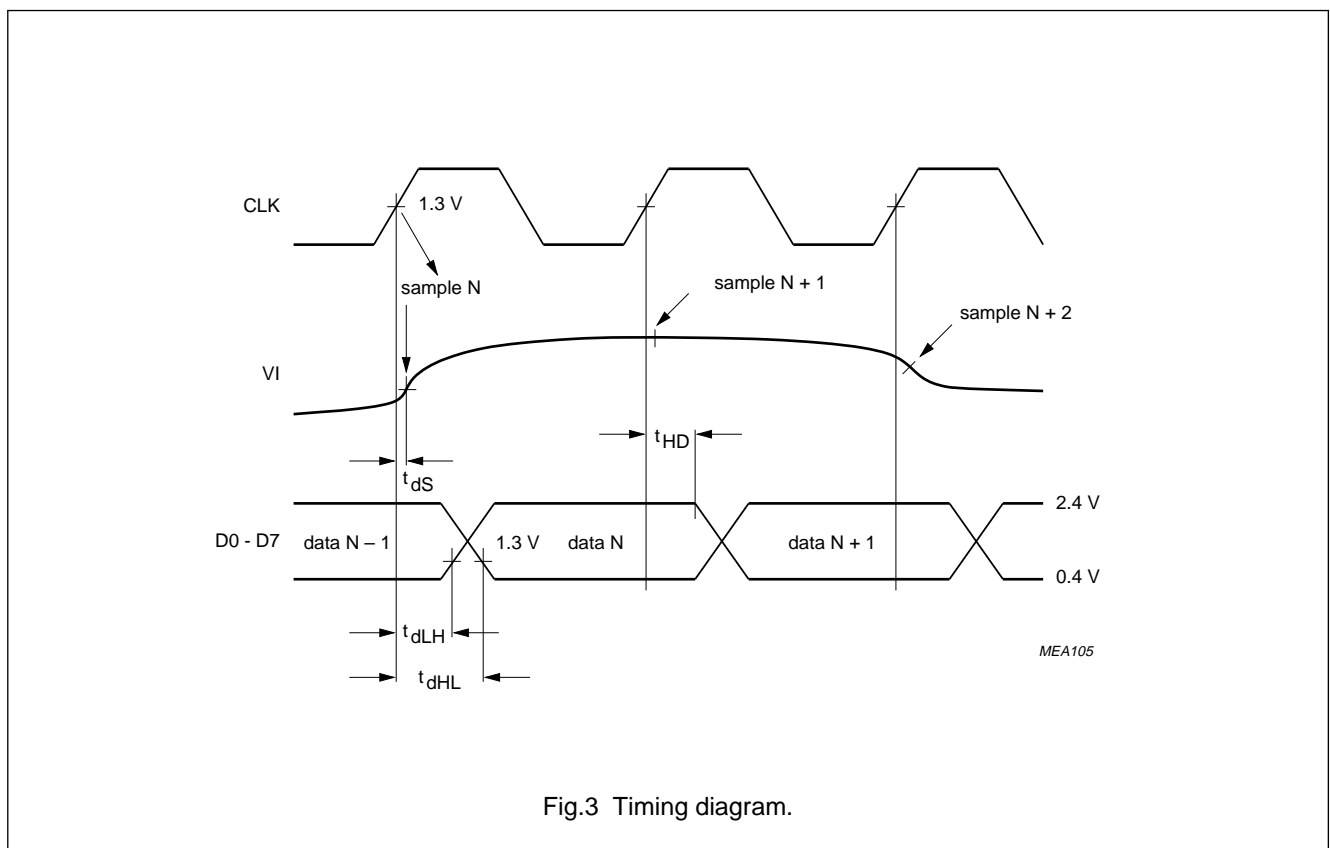


Fig.3 Timing diagram.

8-bit high-speed analog-to-digital converter

TDA8703

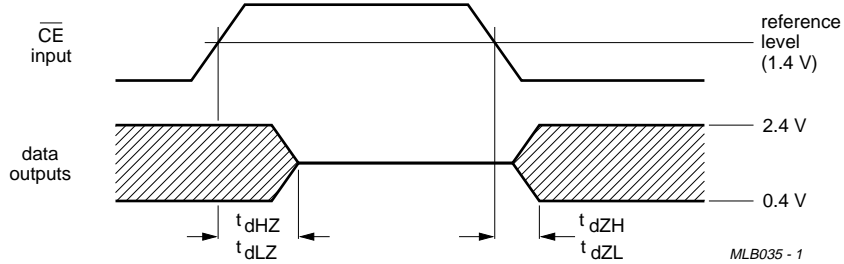


Fig.4 3-state delay timing diagram.

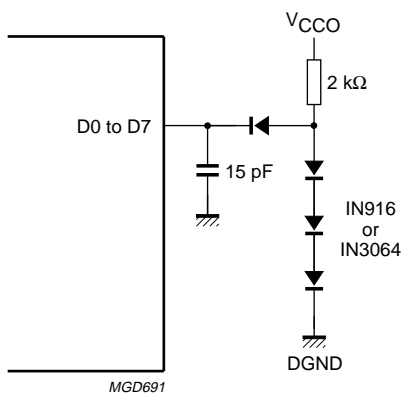


Fig.5 Load circuit for timing measurement; data outputs ( $\overline{CE} = \text{LOW}$ ).

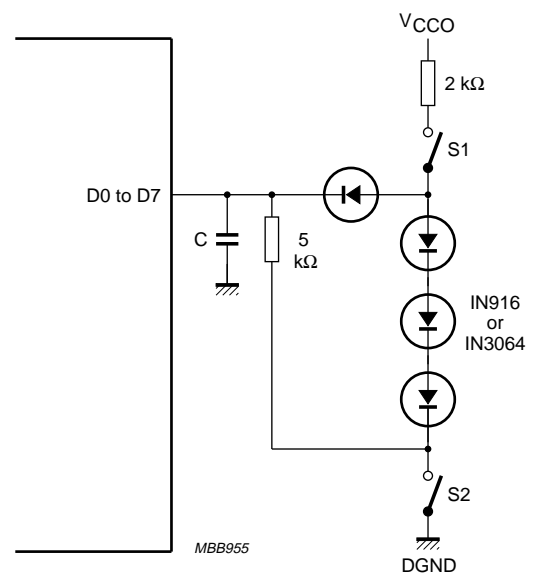


Fig.6 Load circuit for timing measurement; 3-state outputs ( $\overline{CE}$ :  $f_i = 1 \text{ MHz}$ ;  $V_{V1} = 3 \text{ V}$ ); see Table 3.

8-bit high-speed analog-to-digital converter

TDA8703

**Table 3** Mode selection

| TIMING MEASUREMENT | SWITCH S1 | SWITCH S2 | CAPACITOR |
|--------------------|-----------|-----------|-----------|
| $t_{dZH}$          | open      | closed    | 15 pF     |
| $t_{dZL}$          | closed    | open      | 15 pF     |
| $t_{dHZ}$          | closed    | closed    | 5 pF      |
| $t_{dLZ}$          | closed    | closed    | 5 pF      |

**INTERNAL PIN CONFIGURATIONS**

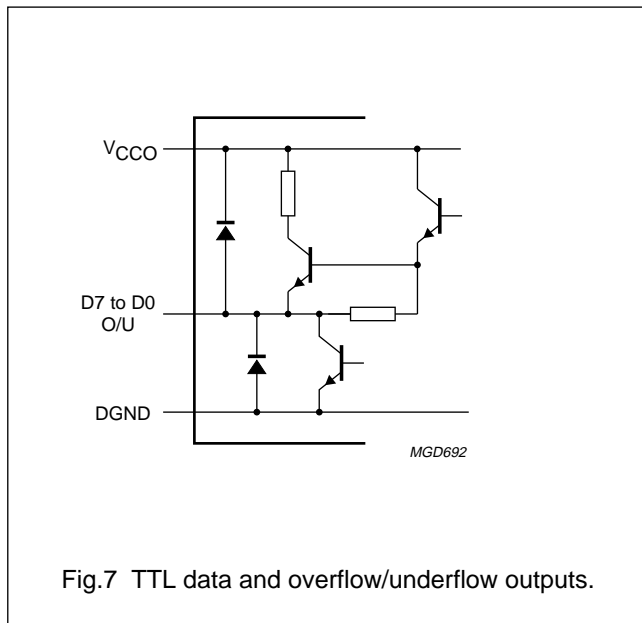


Fig.7 TTL data and overflow/underflow outputs.

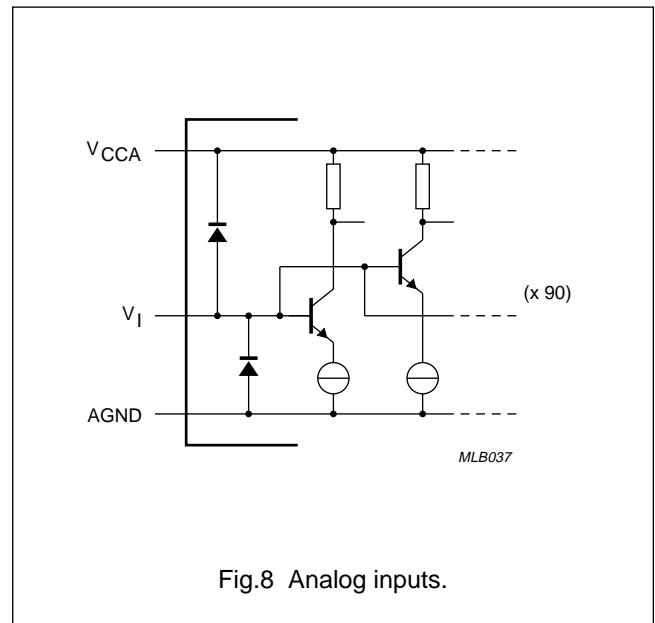


Fig.8 Analog inputs.

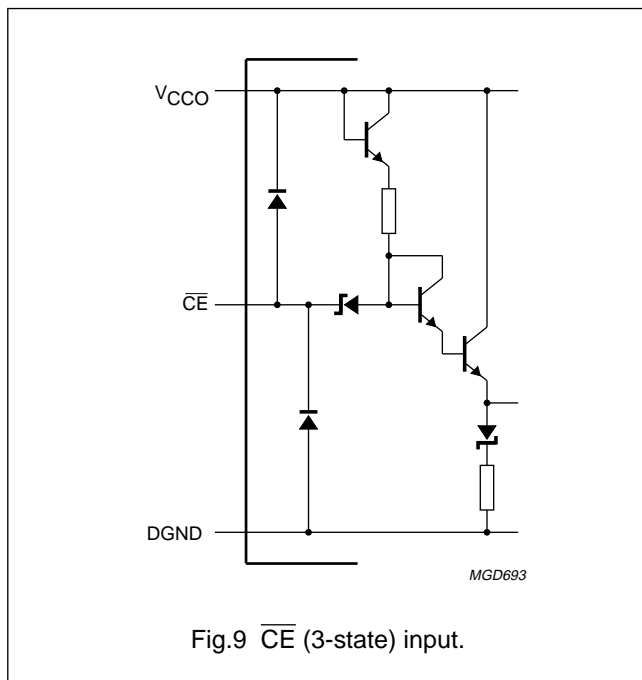


Fig.9  $\overline{CE}$  (3-state) input.

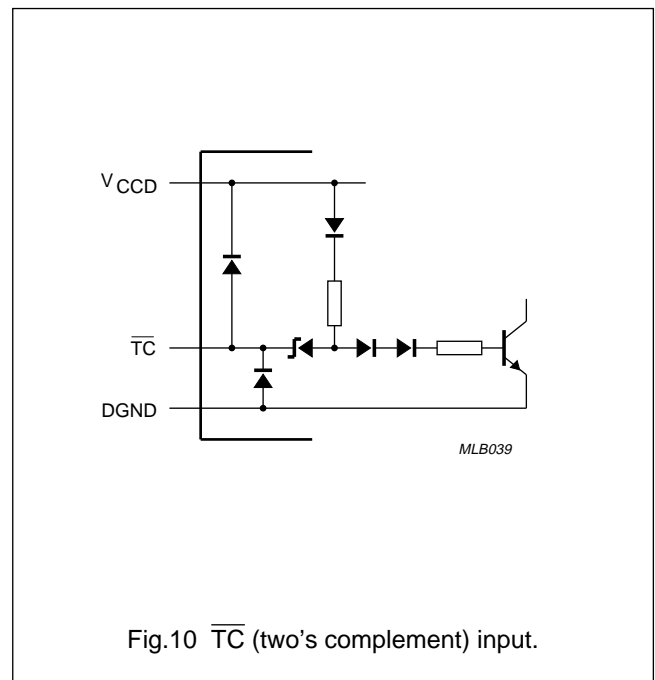


Fig.10  $\overline{TC}$  (two's complement) input.

8-bit high-speed analog-to-digital converter

TDA8703

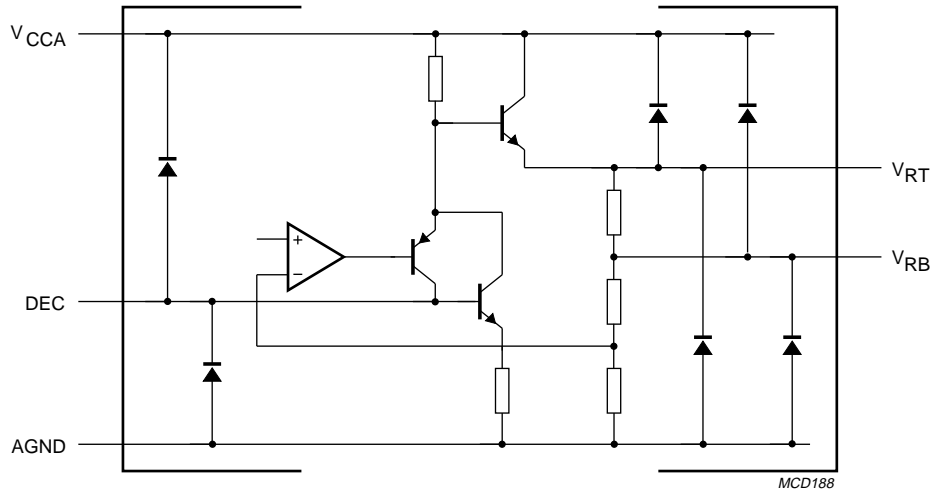


Fig.11  $V_{RB}$ ,  $V_{RT}$  and  $DEC$ .

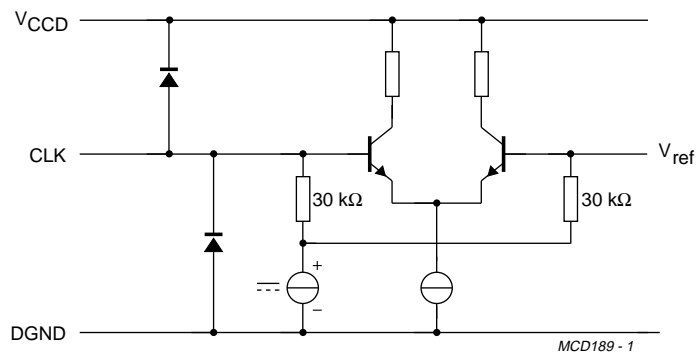


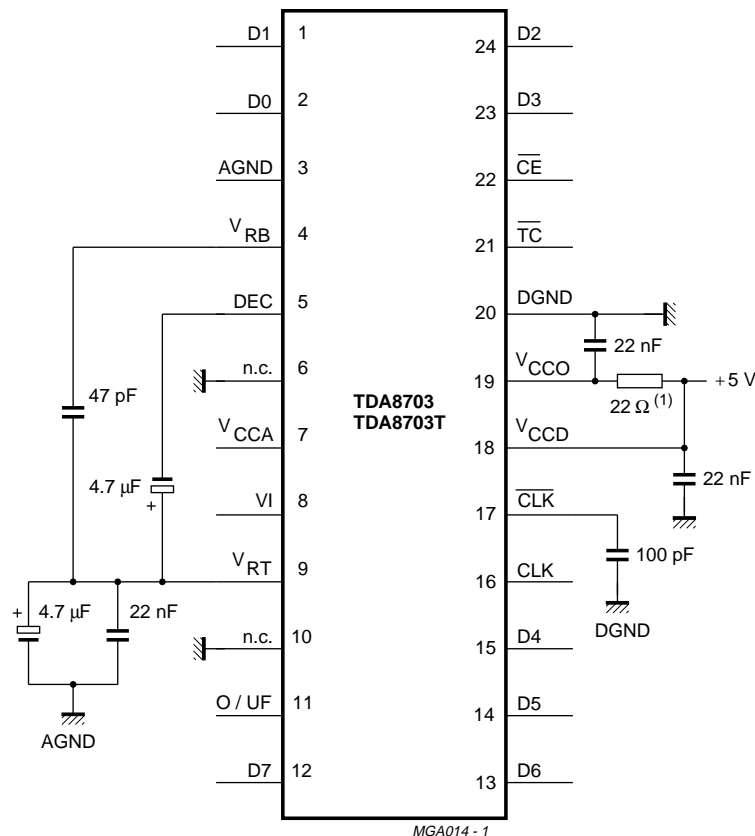
Fig.12  $CLK$  and  $\overline{CLK}$  inputs.

## 8-bit high-speed analog-to-digital converter

## TDA8703

## APPLICATION INFORMATION

Additional application information will be supplied upon request (please quote number FTV/8901).



CLK should be decoupled to the DGND with a 100 nF capacitor, if a TTL signal is used on CLK (see Chapter "Characteristics", note 1).

CLK and  $\overline{\text{CLK}}$  can be used in a differential mode (see Chapter "Characteristics", note 1).

$V_{\text{RB}}$  and  $V_{\text{RT}}$  are decoupling pins for the internal reference ladder; do not draw current from these pins in order to achieve good linearity.

If it is required to use the TDA8703 in a parallel system configuration, the references ( $V_{\text{RB}}$  and  $V_{\text{RT}}$ ) of each TDA8703 can be connected together. Code 0 will be identical and code 255 will remain in the 1 LSB variation for each TDA8703.

Analog and digital supplies should be separated and decoupled.

Pins 6 and 10 should be connected to AGND in order to prevent noise influence.

(1) It is recommended to decouple  $V_{\text{CCO}}$  through a 22  $\Omega$  resistor especially when the output data of the TDA8703 interfaces with a capacitive CMOS load device.

Fig.13 Application diagram.

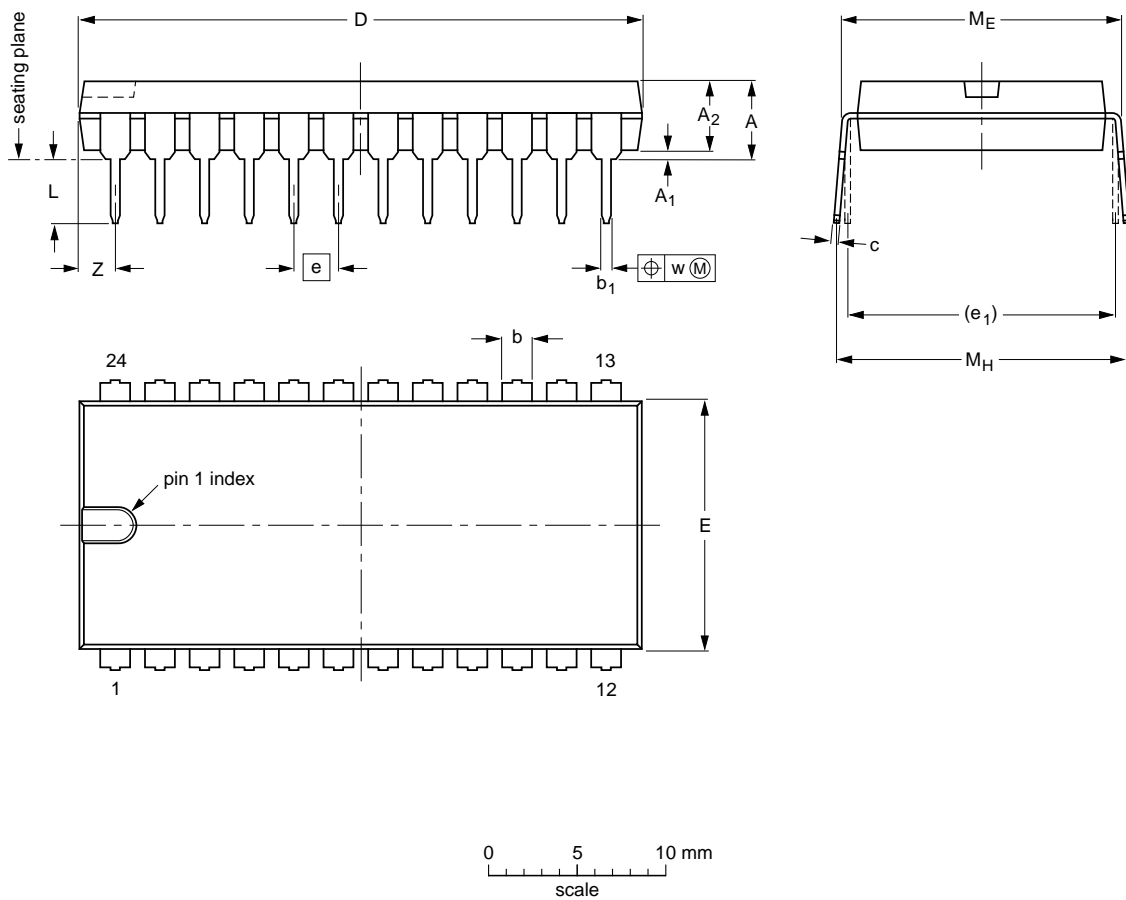
8-bit high-speed analog-to-digital converter

TDA8703

PACKAGE OUTLINES

DIP24: plastic dual in-line package; 24 leads (600 mil)

SOT101-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

| UNIT   | A max. | A <sub>1</sub> min. | A <sub>2</sub> max. | b              | b <sub>1</sub> | c              | D <sup>(1)</sup> | E <sup>(1)</sup> | e    | e <sub>1</sub> | L            | M <sub>E</sub> | M <sub>H</sub> | w    | Z <sup>(1)</sup> max. |
|--------|--------|---------------------|---------------------|----------------|----------------|----------------|------------------|------------------|------|----------------|--------------|----------------|----------------|------|-----------------------|
| mm     | 5.1    | 0.51                | 4.0                 | 1.7<br>1.3     | 0.53<br>0.38   | 0.32<br>0.23   | 32.0<br>31.4     | 14.1<br>13.7     | 2.54 | 15.24          | 3.9<br>3.4   | 15.80<br>15.24 | 17.15<br>15.90 | 0.25 | 2.2                   |
| inches | 0.20   | 0.020               | 0.16                | 0.066<br>0.051 | 0.021<br>0.015 | 0.013<br>0.009 | 1.26<br>1.24     | 0.56<br>0.54     | 0.10 | 0.60           | 0.15<br>0.13 | 0.62<br>0.60   | 0.68<br>0.63   | 0.01 | 0.087                 |

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

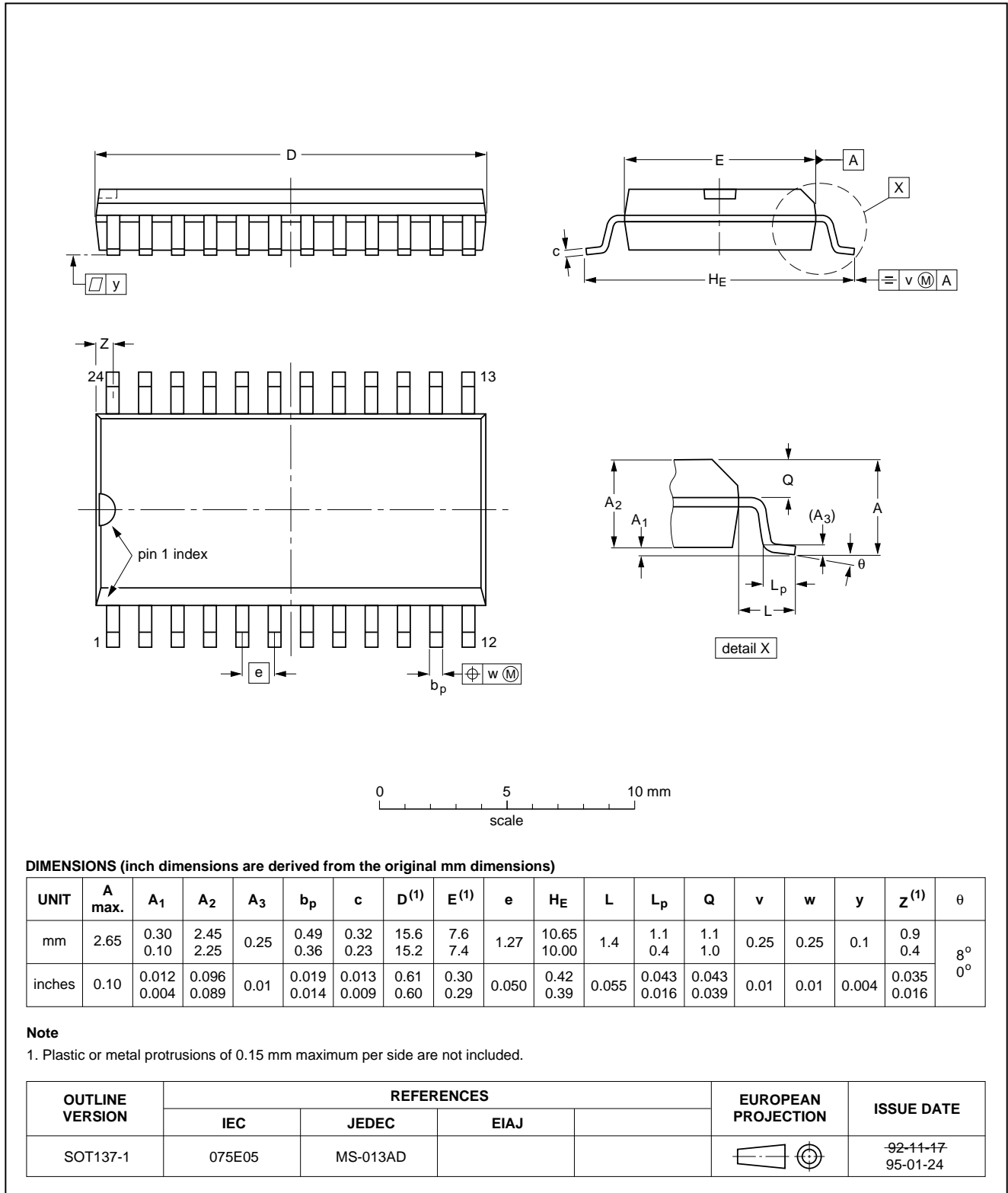
| OUTLINE VERSION | REFERENCES |          |      |  | EUROPEAN PROJECTION | ISSUE DATE           |
|-----------------|------------|----------|------|--|---------------------|----------------------|
|                 | IEC        | JEDEC    | EIAJ |  |                     |                      |
| SOT101-1        | 051G02     | MO-015AD |      |  |                     | 92-11-17<br>95-01-23 |

8-bit high-speed analog-to-digital converter

TDA8703

SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1





## 8-bit high-speed analog-to-digital converter

TDA8703

### SOLDERING

#### Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "IC Package Databook" (order code 9398 652 90011).

#### DIP

##### SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ( $T_{stg\ max}$ ). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

##### REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

#### SO

##### REFLOW SOLDERING

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

##### WAVE SOLDERING

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

##### REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

## 8-bit high-speed analog-to-digital converter

TDA8703

**DEFINITIONS**

|   |   |
|---|---|
| <b>Data sheet status</b>  |   |
| Objective specification   | This data sheet contains target or goal specifications for product development.       |
| Preliminary specification   | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification   | This data sheet contains final product specifications.                                |
| <b>Limiting values</b>  |   |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. |   |
| <b>Application information</b>  |   |
| Where application information is given, it is advisory and does not form part of the specification.   |   |

**LIFE SUPPORT APPLICATIONS**

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.