## SN54HCT139, SN74HCT139 DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

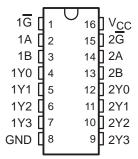
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- Operating Voltage Range of 4.5 V to 5.5 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 80-μA Max I<sub>CC</sub>
- Typical t<sub>pd</sub> = 10 ns
- ±4-mA Output Drive at 5 V
- Low Input Current of 1 μA Max
- Inputs Are TTL-Voltage Compatible
- Designed Specifically for High-Speed Memory Decoders and Data-Transmission Systems
- Incorporate Two Enable Inputs to Simplify Cascading and/or Data Reception

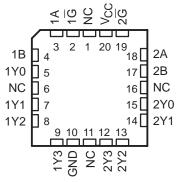
## description/ordering information

The 'HCT139 devices are designed for high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay time of these decoders and the enable time of the memory usually are less than the typical access time of the memory. This means that the effective system delay introduced by the decoders is negligible.

#### SN54HCT139...J OR W PACKAGE SN74HCT139...D, DB, N, OR PW PACKAGE (TOP VIEW)



## SN54HCT139 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

#### ORDERING INFORMATION

TA	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
	PDIP – N	Tube of 25	SN74HCT139N	SN74HCT139N
		Tube of 40	SN74HCT139D	
-40°C to 85°C	SOIC - D	Reel of 2500	SN74HCT139DR	HCT139
		Reel of 250	SN74HCT139DT	
	SSOP – DB	Reel of 2000	SN74HCT139DBR	HT139
		Reel of 2000	SN74HCT139PWR	LITAGO
	TSSOP – PW	Reel of 250	SN74HCT139PWT	HT139
	CDIP – J Tube of 25		SNJ54HCT139J	SNJ54HCT139J
–55°C to 125°C	CFP – W	Tube of 150	SNJ54HCT139W	SNJ54HCT139W
	LCCC - FK	Tube of 55	SNJ54HCT139FK	SNJ54HCT139FK

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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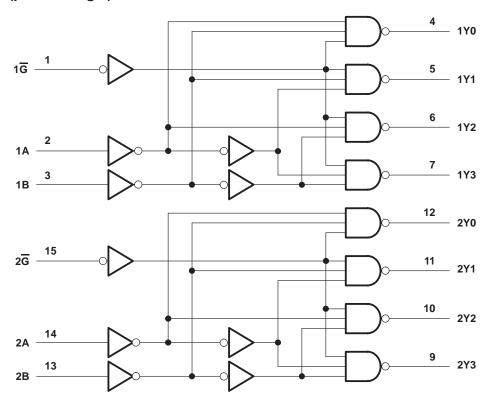
## description/ordering information (continued)

The 'HCT139 devices comprise two individual 2-line to 4-line decoders in a single package. The active-low enable  $(\overline{G})$  input can be used as a data line in demultiplexing applications. These decoders/demultiplexers feature fully buffered inputs, each of which represents only one normalized load to its driving circuit.

**FUNCTION TABLE** 

	INPUTS			OUT	PUTS	
G	SEL	ECT				
G	В	Α	Y0	Y1	Y2	Y3
Н	Χ	Χ	Н	Н	Н	Н
L	L	L	L	Н	Н	Н
L	L	Н	Н	L	Н	Н
L	Н	L	Н	Н	L	Н
L	Н	Н	Н	Н	Н	L

## logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, PW, and W packages.



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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>		 –0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) (s	see Note 1)	 ±20 mA
Output clamp current, IOK (VO < 0 or VO > VO	<sub>CC</sub> ) (see Note 1)	 ±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$	)	 ±25 mA
Continuous current through V <sub>CC</sub> or GND		 ±50 mA
Package thermal impedance, θ <sub>JA</sub> (see Note 2	e): D package	 73°C/W
	DB package	 82°C/W
	N package	 67°C/W
	PW package	 108°C/W
Storage temperature range, T <sub>stg</sub>		 35°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions (see Note 3)

			SN	54HCT1	39	SN	74HCT1	39	
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	2		(5)	2			V
VIL	Low-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V		PA.	0.8			8.0	V
VI	Input voltage		0	7	VCC	0		VCC	V
Vo	Output voltage		0	5	VCC	0		VCC	V
t <sub>t</sub>	Input transition (rise and fall) time		Ó	7	500			500	ns
TA	Operating free-air temperature		-55		125	-40		85	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

24244555	PARAMETER TEST CONDITIONS		Vaa	Т	A = 25°C	;	SN54H	CT139	SN74HCT139		
PARAMETER			VCC	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
.,	V VV	I <sub>OH</sub> = -20 μA	45.7	4.4	4.499		4.4		4.4		.,
Voн	$V_I = V_{IH}$ or $V_{IL}$	I <sub>OH</sub> = -4 mA	4.5 V	3.98	4.3		3.7	3	3.84		V
.,	\\ \\ an\\	I <sub>OL</sub> = 20 μA	45.1/		0.001	0.1		0.1		0.1	.,
Vol	$V_I = V_{IH}$ or $V_{IL}$	I <sub>OL</sub> = 4 mA	4.5 V		0.17	0.26		0.4		0.33	V
lį	$V_I = V_{CC}$ or 0		5.5 V		±0.1	±100		±1000		±1000	nA
ICC	$V_I = V_{CC}$ or 0,	I <sub>O</sub> = 0	5.5 V			8	2	160		80	μΑ
ΔI <sub>CC</sub> ‡	One input at 0.5 V of Other inputs at 0 or		5.5 V		1.4	2.4	OHO	3		2.9	mA
Ci			4.5 V to 5.5 V		3	10		10		10	pF

<sup>‡</sup>This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or VCC.



NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

<sup>2.</sup> The package thermal impedance is calculated in accordance with JESD 51-7.

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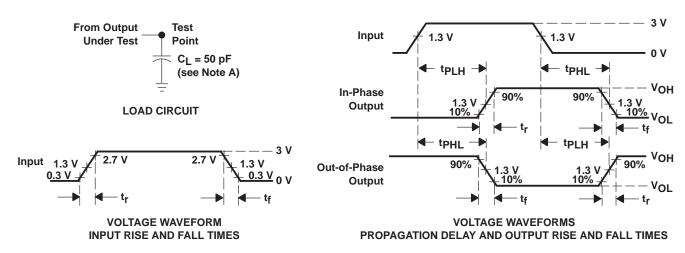
# switching characteristics over recommended operating free-air temperature range, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

DADAMETED	FROM	FROM TO		Τ <sub>Δ</sub>	λ = 25°C	;	SN54H	CT139	SN74H	CT139	
PARAMETER	(INPUT)	(OUTPUT)	VCC	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
	A == D	D V			14	34		51		43	
4 .	A or B		5.5 V		12	30		4/50		40	
<sup>t</sup> pd	G	Y	4.5 V		11	34	1	51		43	ns
	G		5.5 V		10	30	05	50		40	
+.		V	4.5 V		8	15	90	22		19	nc
t <sub>t</sub>		1	5.5 V		6	14	by d	21		17	ns

## operating characteristics, T<sub>A</sub> = 25°C

	PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance per decoder	No load	25	pF

#### PARAMETER MEASUREMENT INFORMATION



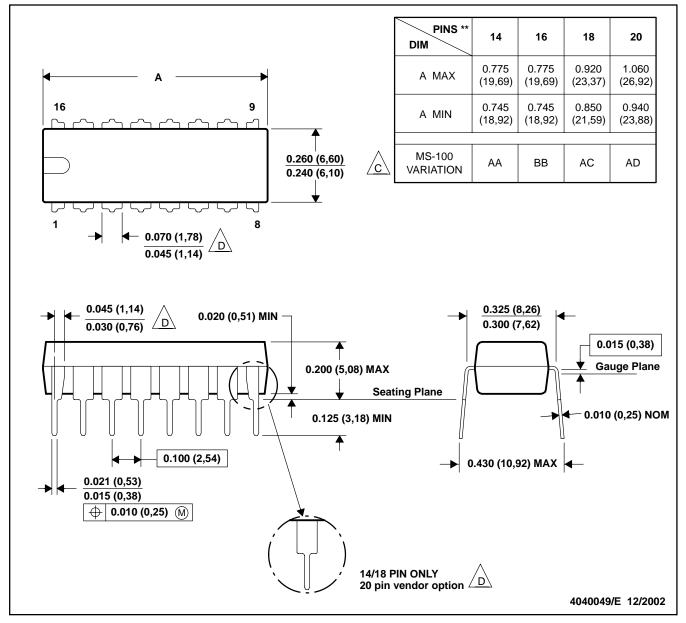
- NOTES: A. C<sub>L</sub> includes probe and test-fixture capacitance.
  - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_Q = 50 \Omega$ ,  $t_f = 6$  ns,  $t_f = 6$  ns.
  - C. The outputs are measured one at a time with one input transition per measurement.
  - D. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

## N (R-PDIP-T\*\*)

#### **16 PINS SHOWN**

#### PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

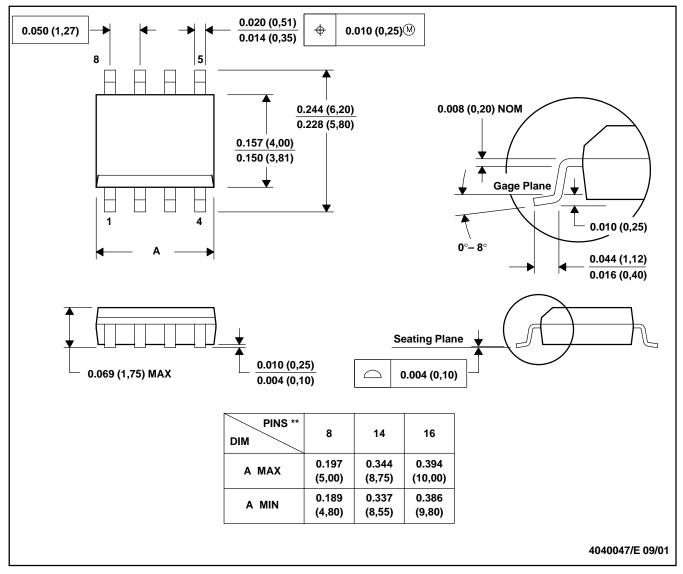
Falls within JEDEC MS-001, except 18 and 20 pin minimum body Irngth (Dim A).

The 20 pin end lead shoulder width is a vendor option, either half or full width.

## D (R-PDSO-G\*\*)

#### PLASTIC SMALL-OUTLINE PACKAGE

#### **8 PINS SHOWN**



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

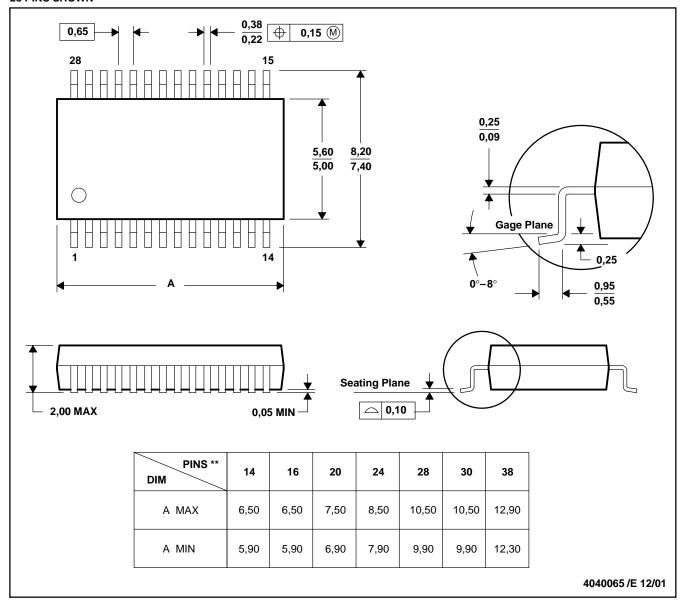
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).

D. Falls within JEDEC MS-012

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

#### **28 PINS SHOWN**



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

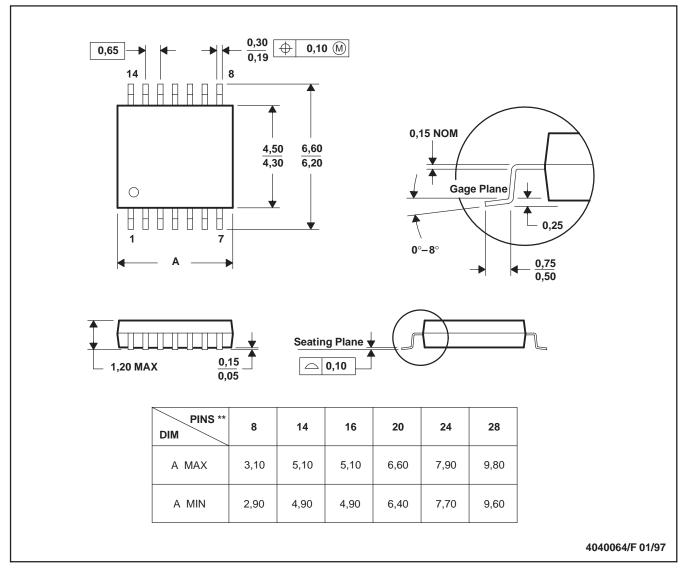
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-150

## PW (R-PDSO-G\*\*)

#### 14 PINS SHOWN

#### PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

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