Triple-Channel Digital Isolators

ADuM1300/ADuM1301

FEATURES

Low power operation
- **5 V operation**
  - **1.2 mA per channel maximum @ 0 Mbps to 2 Mbps**
  - **3.5 mA per channel maximum @ 10 Mbps**
  - **32 mA per channel maximum @ 90 Mbps**
- **3 V operation**
  - **0.8 mA per channel maximum @ 0 Mbps to 2 Mbps**
  - **2.2 mA per channel maximum @ 10 Mbps**
  - **20 mA per channel maximum @ 90 Mbps**

Bidirectional communication
3 V/5 V level translation
High temperature operation: 105°C
High data rate: dc to 90 Mbps (NRZ)
Precise timing characteristics
- **2 ns maximum pulse width distortion**
- **2 ns maximum channel-to-channel matching**

High common-mode transient immunity: >25 kV/μs
Output enable function
16-lead SOIC wide body package
RoHS-compliant models available
Safety and regulatory approvals
- **UL recognition: 2500 V rms for 1 minute per UL 1577**
- **CSA Component Acceptance Notice #5A**
- **VDE Certificate of Conformity**
  - **DIN V VDE V 0884-10 (VDE V 0884-10):2006-12**
  - **V_{IORM} = 560 V peak**
- **TÜV approval: IEC/EN/UL/CSA 61010-1**

APPLICATIONS

General-purpose multichannel isolation
SPI interface/data converter isolation
RS-232/RS-422/RS-485 transceivers
Industrial field bus isolation

GENERAL DESCRIPTION

The ADuM130x[1] are 3-channel digital isolators based on the Analog Devices, Inc., *i*Coupler® technology. Combining high speed CMOS and monolithic transformer technology, these isolation components provide outstanding performance characteristics superior to alternatives, such as optocoupler devices.

By avoiding the use of LEDs and photodiodes, *i*Coupler devices remove the design difficulties commonly associated with optocouplers. The typical optocoupler concerns regarding uncertain current transfer ratios, nonlinear transfer functions, and temperature and lifetime effects are eliminated with the simple *i*Coupler digital interfaces and stable performance characteristics. The need for external drivers and other discrete components is eliminated with these *i*Coupler products. Furthermore, *i*Coupler devices consume one-tenth to one-sixth the power of optocouplers at comparable signal data rates.

The ADuM130x isolators provide three independent isolation channels in a variety of channel configurations and data rates (see the Ordering Guide). Both models operate with the supply voltage on either side ranging from 2.7 V to 5.5 V, providing compatibility with lower voltage systems as well as enabling a voltage translation functionality across the isolation barrier. In addition, the ADuM130x provide low pulse width distortion (<2 ns for CRW grade) and tight channel-to-channel matching (<2 ns for CRW grade). Unlike other optocoupler alternatives, the ADuM130x isolators have a patented refresh feature that ensures dc correctness in the absence of input logic transitions and during power-up/power-down conditions.

[1] Protected by U.S. Patents 5,952,849; 6,873,065; 6,903,578; and 7,075,329. Other patents are pending.

FUNCTIONAL BLOCK DIAGRAMS

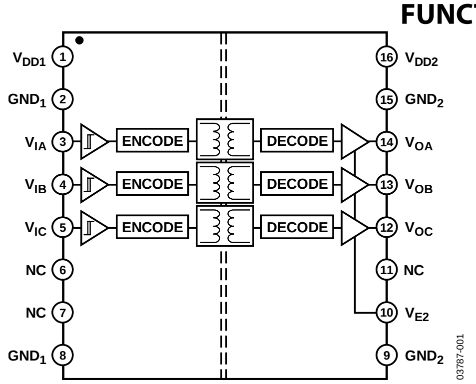

Figure 1. ADuM1300 Functional Block Diagram

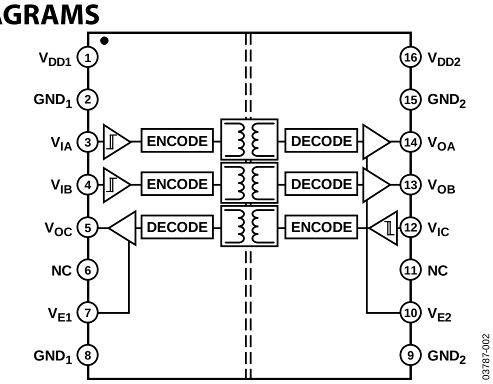

Figure 2. ADuM1301 Functional Block Diagram

Rev. G

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TABLE OF CONTENTS

REVISION HISTORY

11/07—Rev. F to Rev. G

Changes to Note 1 and Figure 2 1
Added ADuM130xARW Change vs. Temperature Parameter 3
Added ADuM130xARW Change vs. Temperature Parameter 5
Added ADuM130xARW Change vs. Temperature Parameter 8
Changes to Figure 14 16

6/07—Rev. E to Rev. F

Updated VDE Certification Throughout 1
Changes to Features, Note 1, Figure 1, and Figure 2 1
Changes to Regulatory Information Section 10
Added Table 10 12
Added Insulation Lifetime Section 17
Updated Outline Dimensions 19
Changes to Ordering Guide 19

2/06—Rev. D to Rev. E

Updated Format .... Universal
Added TÜV Approval .... Universal
Changes to Figure 2 1

5/05—Rev. C to Rev. D

Changes to Format .... Universal
Changes to Figure 2 1
Changes to Table 6 10
Changes to Ordering Guide 18

6/04—Rev. B to Rev. C

Changes to Format .... Universal
Changes to Features 1
Changes to Electrical Characteristics—5 V Operation 3
Changes to Electrical Characteristics—3 V Operation 5
Changes to Electrical Characteristics—Mixed 5 V/3 V or 3 V/5 V Operation 7
Changes to Ordering Guide 18

5/04—Rev. A to Rev. B

Changes to the Format .... Universal
Changes to the Features 1
Changes to Table 7 and Table 8 14
Changes to Table 9 15
Changes to the DC Correctness and Magnetic Field Immunity Section 19
Changes to the Power Consumption Section 20
Changes to the Ordering Guide 21

9/03—Rev. 0 to Rev. A

Edits to Regulatory Information 13
Edits to Absolute Maximum Ratings 15
Deleted the Package Branding Information 16

9/03—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V OPERATION

All voltages are relative to their respective ground. 4.5 V ≤ V_{DD1} ≤ 5.5 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V; all minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted; all typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 5 V.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current per Channel, Quiescent	$I_{DDI (Q)}$		0.50	0.53	mA	
Output Supply Current per Channel, Quiescent	$I_{DDO (Q)}$		0.19	0.21	mA	
ADuM1300 Total Supply Current Three Channels[1]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$		1.6	2.5	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (Q)}$		0.7	1.0	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRW and CRW Grades Only)						
V_{DD1} Supply Current	$I_{DD1 (10)}$		6.5	8.1	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (10)}$		1.9	2.5	mA	5 MHz logic signal freq.
90 Mbps (CRW Grade Only)						
V_{DD1} Supply Current	$I_{DD1 (90)}$		57	77	mA	45 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (90)}$		16	18	mA	45 MHz logic signal freq.
ADuM1301 Total Supply Current, Three Channels[1]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$		1.3	2.1	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (Q)}$		1.0	1.4	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRW and CRW Grades Only)						
V_{DD1} Supply Current	$I_{DD1 (10)}$		5.0	6.2	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (10)}$		3.4	4.2	mA	5 MHz logic signal freq.
90 Mbps (CRW Grade Only)						
V_{DD1} Supply Current	$I_{DD1 (90)}$		43	57	mA	45 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (90)}$		29	37	mA	45 MHz logic signal freq.
For All Models						
Input Currents	I_{IA}, I_{IB}, I_{IC}, I_{E1}, I_{E2}	−10	+0.01	+10	µA	0 V ≤ V_{IA}, V_{IB}, V_{IC} ≤ V_{DD1} or V_{DD2}, 0 V ≤ V_{E1}, V_{E2} ≤ V_{DD1} or V_{DD2}
Logic High Input Threshold	V_{IH}, V_{EH}	2.0			V	
Logic Low Input Threshold	V_{IL}, V_{EL}			0.8	V	
Logic High Output Voltages	V_{OAH}, V_{OBH}, V_{OCH}	(V_{DD1} or V_{DD2}) − 0.1	5.0		V	I_{Ox} = −20 µA, V_{Ix} = V_{IxH}
		(V_{DD1} or V_{DD2}) − 0.4	4.8		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OAL}, V_{OBL}, V_{OCL}		0.0	0.1	V	I_{Ox} = 20 µA, V_{Ix} = V_{IxL}
			0.04	0.1	V	I_{Ox} = 400 µA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxL}
SWITCHING SPECIFICATIONS						
ADuM130xARW						
Minimum Pulse Width[2]	PW			1000	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate[3]		1			Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay[4]	t_{PHL}, t_{PLH}	50	65	100	ns	C_L = 15 pF, CMOS signal levels
Pulse Width Distortion, $\|t_{PLH} − t_{PHL}\|$[4]	PWD			40	ns	C_L = 15 pF, CMOS signal levels
Change vs. Temperature			11		ps/°C	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew[5]	t_{PSK}			50	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching[6]	t_{PSKCD}/t_{PSKOD}			50	ns	C_L = 15 pF, CMOS signal levels

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
ADuM130xBRW						
Minimum Pulse Width[2]	PW			100	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate[3]		10			Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay[4]	t_{PHL}, t_{PLH}	20	32	50	ns	C_L = 15 pF, CMOS signal levels
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$[4]	PWD			3	ns	C_L = 15 pF, CMOS signal levels
Change vs. Temperature			5		ps/°C	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew[5]	t_{PSK}			15	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels[6]	t_{PSKCD}			3	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels[6]	t_{PSKOD}			6	ns	C_L = 15 pF, CMOS signal levels
ADuM130xCRW						
Minimum Pulse Width[2]	PW		8.3	11.1	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate[3]		90	120		Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay[4]	t_{PHL}, t_{PLH}	18	27	32	ns	C_L = 15 pF, CMOS signal levels
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$[4]	PWD		0.5	2	ns	C_L = 15 pF, CMOS signal levels
Change vs. Temperature			3		ps/°C	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew[5]	t_{PSK}			10	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels[6]	t_{PSKCD}			2	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels[6]	t_{PSKOD}			5	ns	C_L = 15 pF, CMOS signal levels
For All Models						
Output Disable Propagation Delay (High/Low to High Impedance)	t_{PHZ}, t_{PLH}		6	8	ns	C_L = 15 pF, CMOS signal levels
Output Enable Propagation Delay (High Impedance to High/Low)	t_{PZH}, t_{PZL}		6	8	ns	C_L = 15 pF, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t_R/t_F		2.5		ns	C_L = 15 pF, CMOS signal levels
Common-Mode Transient Immunity at Logic High Output[7]	$\|CM_H\|$	25	35		kV/µs	$V_{Ix} = V_{DD1}$ or V_{DD2}, V_{CM} = 1000 V, transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output[7]	$\|CM_L\|$	25	35		kV/µs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.2		Mbps	
Input Dynamic Supply Current per Channel[8]	$I_{DDI (D)}$		0.19		mA/Mbps	
Output Dynamic Supply Current per Channel[8]	$I_{DDO (D)}$		0.05		mA/Mbps	

[1] The supply current values are for all three channels combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate may be calculated as described in the Power Consumption section. See Figure 6 through Figure 8 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 9 through Figure 12 for total V_{DD1} and V_{DD2} supply currents as a function of data rate for ADuM1300/ADuM1301 channel configurations.

[2] The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

[3] The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

[4] t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{Ix} signal to the 50% level of the falling edge of the V_{Ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{Ix} signal to the 50% level of the rising edge of the V_{Ox} signal.

[5] t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

[6] Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

[7] CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8\ V_{DD2}$. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O < 0.8$ V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

[8] Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 6 through Figure 8 for information on per-channel supply current for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating the per-channel supply current for a given data rate.

ELECTRICAL CHARACTERISTICS—3 V OPERATION

All voltages are relative to their respective ground. 2.7 V ≤ V_{DD1} ≤ 3.6 V, 2.7 V ≤ V_{DD2} ≤ 3.6 V; all minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted; all typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 3.0 V.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current per Channel, Quiescent	$I_{DDI (Q)}$		0.26	0.31	mA	
Output Supply Current per Channel, Quiescent	$I_{DDO (Q)}$		0.11	0.14	mA	
ADuM1300 Total Supply Current, Three Channels[1]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$		0.9	1.7	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (Q)}$		0.4	0.7	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRW and CRW Grades Only)						
V_{DD1} Supply Current	$I_{DD1 (10)}$		3.4	4.9	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (10)}$		1.1	1.6	mA	5 MHz logic signal freq.
90 Mbps (CRW Grade Only)						
V_{DD1} Supply Current	$I_{DD1 (90)}$		31	48	mA	45 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (90)}$		8	13	mA	45 MHz logic signal freq.
ADuM1301 Total Supply Current, Three Channels[1]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$		0.7	1.4	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (Q)}$		0.6	0.9	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRW and CRW Grades Only)						
V_{DD1} Supply Current	$I_{DD1 (10)}$		2.6	3.7	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (10)}$		1.8	2.5	mA	5 MHz logic signal freq.
90 Mbps (CRW Grade Only)						
V_{DD1} Supply Current	$I_{DD1 (90)}$		24	36	mA	45 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (90)}$		16	23	mA	45 MHz logic signal freq.
For All Models						
Input Currents	I_{IA}, I_{IB}, I_{IC}, I_{E1}, I_{E2}	−10	+0.01	+10	µA	0 V ≤ V_{IA}, V_{IB}, V_{IC} ≤ V_{DD1} or V_{DD2}, 0 V ≤ V_{E1}, V_{E2} ≤ V_{DD1} or V_{DD2}
Logic High Input Threshold	V_{IH}, V_{EH}	1.6			V	
Logic Low Input Threshold	V_{IL}, V_{EL}			0.4	V	
Logic High Output Voltages	V_{OAH}, V_{OBH}, V_{OCH}	(V_{DD1} or V_{DD2}) − 0.1	3.0		V	I_{Ox} = −20 µA, V_{Ix} = V_{IxH}
		(V_{DD1} or V_{DD2}) − 0.4	2.8		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OAL}, V_{OBL}, V_{OCL}		0.0	0.1	V	I_{Ox} = 20 µA, V_{Ix} = V_{IxL}
			0.04	0.1	V	I_{Ox} = 400 µA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxL}
SWITCHING SPECIFICATIONS						
ADuM130xARW						
Minimum Pulse Width[2]	PW			1000	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate[3]		1			Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay[4]	t_{PHL}, t_{PLH}	50	75	100	ns	C_L = 15 pF, CMOS signal levels
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$[4]	PWD			40	ns	C_L = 15 pF, CMOS signal levels
Change vs. Temperature			11		ps/°C	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew[5]	t_{PSK}			50	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching[6]	t_{PSKCD}/t_{PSKOD}			50	ns	C_L = 15 pF, CMOS signal levels

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
ADuM130xBRW						
Minimum Pulse Width[2]	PW			100	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate[3]		10			Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay[4]	t_{PHL}, t_{PLH}	20	38	50	ns	C_L = 15 pF, CMOS signal levels
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$[4]	PWD			3	ns	C_L = 15 pF, CMOS signal levels
Change vs. Temperature			5		ps/°C	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew[5]	t_{PSK}			26	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels[6]	t_{PSKCD}			3	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels[6]	t_{PSKOD}			6	ns	C_L = 15 pF, CMOS signal levels
ADuM130xCRW						
Minimum Pulse Width[2]	PW		8.3	11.1	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate[3]		90	120		Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay[4]	t_{PHL}, t_{PLH}	20	34	45	ns	C_L = 15 pF, CMOS signal levels
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$[4]	PWD		0.5	2	ns	C_L = 15 pF, CMOS signal levels
Change vs. Temperature			3		ps/°C	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew[5]	t_{PSK}			16	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels[6]	t_{PSKCD}			2	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels[6]	t_{PSKOD}			5	ns	C_L = 15 pF, CMOS signal levels
For All Models						
Output Disable Propagation Delay (High/Low to High Impedance)	t_{PHZ}, t_{PLH}		6	8	ns	C_L = 15 pF, CMOS signal levels
Output Enable Propagation Delay (High Impedance to High/Low)	t_{PZH}, t_{PZL}		6	8	ns	C_L = 15 pF, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t_R/t_F		3		ns	C_L = 15 pF, CMOS signal levels
Common-Mode Transient Immunity at Logic High Output[7]	$\|CM_H\|$	25	35		kV/μs	$V_{Ix} = V_{DD1}$ or V_{DD2}, V_{CM} = 1000 V, transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output[7]	$\|CM_L\|$	25	35		kV/μs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.1		Mbps	
Input Dynamic Supply Current per Channel[8]	$I_{DDI (D)}$		0.10		mA/Mbps	
Output Dynamic Supply Current per Channel[8]	$I_{DDO (D)}$		0.03		mA/Mbps	

[1] The supply current values are for all three channels combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate may be calculated as described in the Power Consumption section. See Figure 6 through Figure 8 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 9 through Figure 12 for total V_{DD1} and V_{DD2} supply currents as a function of data rate for ADuM1300/ADuM1301 channel configurations.
[2] The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.
[3] The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.
[4] t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{Ix} signal to the 50% level of the falling edge of the V_{Ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{Ix} signal to the 50% level of the rising edge of the V_{Ox} signal.
[5] t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.
[6] Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.
[7] CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8\ V_{DD2}$. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O < 0.8$ V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.
[8] Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 6 through Figure 8 for information on per-channel supply current for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating the per-channel supply current for a given data rate.

ELECTRICAL CHARACTERISTICS—MIXED 5 V/3 V OR 3 V/5 V OPERATION

All voltages are relative to their respective ground. 5 V/3 V operation: 4.5 V ≤ V_{DD1} ≤ 5.5 V, 2.7 V ≤ V_{DD2} ≤ 3.6 V; 3 V/5 V operation: 2.7 V ≤ V_{DD1} ≤ 3.6 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V; all minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted; all typical specifications are at T_A = 25°C; V_{DD1} = 3.0 V, V_{DD2} = 5 V or V_{DD1} = 5 V, V_{DD2} = 3.0 V.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current per Channel, Quiescent	$I_{DDI (Q)}$					
5 V/3 V Operation			0.50	0.53	mA	
3 V/5 V Operation			0.26	0.31	mA	
Output Supply Current per Channel, Quiescent	$I_{DDO (Q)}$					
5 V/3 V Operation			0.11	0.14	mA	
3 V/5 V Operation			0.19	0.21	mA	
ADuM1300 Total Supply Current, Three Channels[1]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$					
5 V/3 V Operation			1.6	2.5	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation			0.9	1.7	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (Q)}$					
5 V/3 V Operation			0.4	0.7	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation			0.7	1.0	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRW and CRW Grades Only)						
V_{DD1} Supply Current	$I_{DD1 (10)}$					
5 V/3 V Operation			6.5	8.1	mA	5 MHz logic signal freq.
3 V/5 V Operation			3.4	4.9	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (10)}$					
5 V/3 V Operation			1.1	1.6	mA	5 MHz logic signal freq.
3 V/5 V Operation			1.9	2.5	mA	5 MHz logic signal freq.
90 Mbps (CRW Grade Only)						
V_{DD1} Supply Current	$I_{DD1 (90)}$					
5 V/3 V Operation			57	77	mA	45 MHz logic signal freq.
3 V/5 V Operation			31	48	mA	45 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (90)}$					
5 V/3 V Operation			8	13	mA	45 MHz logic signal freq.
3 V/5 V Operation			16	18	mA	45 MHz logic signal freq.
ADuM1301 Total Supply Current, Three Channels[1]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$					
5 V/3 V Operation			1.3	2.1	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation			0.7	1.4	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (Q)}$					
5 V/3 V Operation			0.6	0.9	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation			1.0	1.4	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRW and CRW Grades Only)						
V_{DD1} Supply Current	$I_{DD1 (10)}$					
5 V/3 V Operation			5.0	6.2	mA	5 MHz logic signal freq.
3 V/5 V Operation			2.6	3.7	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (10)}$					
5 V/3 V Operation			1.8	2.5	mA	5 MHz logic signal freq.
3 V/5 V Operation			3.4	4.2	mA	5 MHz logic signal freq.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
90 Mbps (CRW Grade Only)						
V_{DD1} Supply Current	$I_{DD1\ (90)}$					
5 V/3 V Operation			43	57	mA	45 MHz logic signal freq.
3 V/5 V Operation			24	36	mA	45 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2\ (90)}$					
5 V/3 V Operation			16	23	mA	45 MHz logic signal freq.
3 V/5 V Operation			29	37	mA	45 MHz logic signal freq.
For All Models						
Input Currents	I_{IA}, I_{IB}, I_{IC}, I_{E1}, I_{E2}	−10	+0.01	+10	µA	$0\ V \le V_{IA}, V_{IB}, V_{IC} \le V_{DD1}$ or V_{DD2}, $0\ V \le V_{E1}, V_{E2} \le V_{DD1}$ or V_{DD2}
Logic High Input Threshold	V_{IH}, V_{EH}					
5 V/3 V Operation		2.0			V	
3 V/5 V Operation		1.6			V	
Logic Low Input Threshold	V_{IL}, V_{EL}					
5 V/3 V Operation				0.8	V	
3 V/5 V Operation				0.4	V	
Logic High Output Voltages	V_{OAH}, V_{OBH}, V_{OCH}	(V_{DD1} or V_{DD2}) − 0.1	(V_{DD1} or V_{DD2})		V	$I_{Ox} = -20\ \mu A$, $V_{Ix} = V_{IxH}$
		(V_{DD1} or V_{DD2}) − 0.4	(V_{DD1} or V_{DD2}) − 0.2		V	$I_{Ox} = -4\ mA$, $V_{Ix} = V_{IxH}$
Logic Low Output Voltages	V_{OAL}, V_{OBL}, V_{OCL}		0.0	0.1	V	$I_{Ox} = 20\ \mu A$, $V_{Ix} = V_{IxL}$
			0.04	0.1	V	$I_{Ox} = 400\ \mu A$, $V_{Ix} = V_{IxL}$
			0.2	0.4	V	$I_{Ox} = 4\ mA$, $V_{Ix} = V_{IxL}$
SWITCHING SPECIFICATIONS						
ADuM130xARW						
Minimum Pulse Width[2]	PW			1000	ns	$C_L = 15$ pF, CMOS signal levels
Maximum Data Rate[3]		1			Mbps	$C_L = 15$ pF, CMOS signal levels
Propagation Delay[4]	t_{PHL}, t_{PLH}	50	70	100	ns	$C_L = 15$ pF, CMOS signal levels
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$[4]	PWD			40	ns	$C_L = 15$ pF, CMOS signal levels
Change vs. Temperature			11		ps/°C	$C_L = 15$ pF, CMOS signal levels
Propagation Delay Skew[5]	t_{PSK}			50	ns	$C_L = 15$ pF, CMOS signal levels
Channel-to-Channel Matching[6]	t_{PSKCD}/t_{PSKOD}			50	ns	$C_L = 15$ pF, CMOS signal levels
ADuM130xBRW						
Minimum Pulse Width[2]	PW			100	ns	$C_L = 15$ pF, CMOS signal levels
Maximum Data Rate[3]		10			Mbps	$C_L = 15$ pF, CMOS signal levels
Propagation Delay[4]	t_{PHL}, t_{PLH}	15	35	50	ns	$C_L = 15$ pF, CMOS signal levels
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$[4]	PWD			3	ns	$C_L = 15$ pF, CMOS signal levels
Change vs. Temperature			5		ps/°C	$C_L = 15$ pF, CMOS signal levels
Propagation Delay Skew[5]	t_{PSK}			6	ns	$C_L = 15$ pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels[6]	t_{PSKCD}			3	ns	$C_L = 15$ pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels[6]	t_{PSKOD}			22	ns	$C_L = 15$ pF, CMOS signal levels
ADuM130xCRW						
Minimum Pulse Width[2]	PW		8.3	11.1	ns	$C_L = 15$ pF, CMOS signal levels
Maximum Data Rate[3]		90	120		Mbps	$C_L = 15$ pF, CMOS signal levels
Propagation Delay[4]	t_{PHL}, t_{PLH}	20	30	40	ns	$C_L = 15$ pF, CMOS signal levels
Pulse Width Distortion, $\|t_{PLH}-t_{PHL}\|$[4]	PWD		0.5	2	ns	$C_L = 15$ pF, CMOS signal levels
Change vs. Temperature			3		ps/°C	$C_L = 15$ pF, CMOS signal levels
Propagation Delay Skew[5]	t_{PSK}			14	ns	$C_L = 15$ pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels[6]	t_{PSKCD}			2	ns	$C_L = 15$ pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels[6]	t_{PSKOD}			5	ns	$C_L = 15$ pF, CMOS signal levels

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
For All Models						
Output Disable Propagation Delay (High/Low to High Impedance)	t_{PHZ}, t_{PLH}		6	8	ns	C_L = 15 pF, CMOS signal levels
Output Enable Propagation Delay (High Impedance to High/Low)	t_{PZH}, t_{PZL}		6	8	ns	C_L = 15 pF, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t_R/t_F					C_L = 15 pF, CMOS signal levels
5 V/3 V Operation			3.0		ns	
3 V/5 V Operation			2.5		ns	
Common-Mode Transient Immunity at Logic High Output[7]	$\|CM_H\|$	25	35		kV/µs	$V_{Ix} = V_{DD1}$ or V_{DD2}, V_{CM} = 1000 V transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output[7]	$\|CM_L\|$	25	35		kV/µs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r					
5 V/3 V Operation			1.2		Mbps	
3 V/5 V Operation			1.1		Mbps	
Input Dynamic Supply Current per Channel[8]	$I_{DDI (D)}$					
5 V/3 V Operation			0.19		mA/Mbps	
3 V/5 V Operation			0.10		mA/Mbps	
Output Dynamic Supply Current per Channel[8]	$I_{DDO (D)}$					
5 V/3 V Operation			0.03		mA/Mbps	
3 V/5 V Operation			0.05		mA/Mbps	

[1] The supply current values are for all three channels combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate may be calculated as described in the Power Consumption section. See Figure 6 through Figure 8 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 9 through Figure 12 for total V_{DD1} and V_{DD2} supply currents as a function of data rate for ADuM1300/ADuM1301 channel configurations.

[2] The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

[3] The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

[4] t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{Ix} signal to the 50% level of the falling edge of the V_{Ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{Ix} signal to the 50% level of the rising edge of the V_{Ox} signal.

[5] t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

[6] Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

[7] CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8 V_{DD2}$. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O < 0.8$ V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

[8] Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 6 through Figure 8 for information on per-channel supply current for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating the per-channel supply current for a given data rate.

PACKAGE CHARACTERISTICS

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Resistance (Input-to-Output)[1]	R_{I-O}		10^{12}		Ω	
Capacitance (Input-to-Output)[1]	C_{I-O}		1.7		pF	f = 1 MHz
Input Capacitance[2]	C_I		4.0		pF	
IC Junction-to-Case Thermal Resistance, Side 1	$θ_{JCI}$		33		°C/W	Thermocouple located at center of package underside
IC Junction-to-Case Thermal Resistance, Side 2	$θ_{JCO}$		28		°C/W	

[1] Device considered a 2-terminal device; Pin 1, Pin 2, Pin 3, Pin 4, Pin 5, Pin 6, Pin 7, and Pin 8 shorted together and Pin 9, Pin 10, Pin 11, Pin 12, Pin 13, Pin 14, Pin 15, and Pin 16 shorted together.
[2] Input capacitance is from any input data pin to ground.

REGULATORY INFORMATION

The ADuM130x are approved by the organizations listed in Table 5. Refer to Table 10 and the Insulation Lifetime section for details regarding recommended maximum working voltages for specific crossisolation waveforms and insulation levels.

Table 5.

UL	CSA	VDE	TÜV
Recognized under 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice #5A	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12[2]	Approved according to: IEC 61010-1:2001 (2nd Edition), EN 61010-1:2001 (2nd Edition), UL 61010-1:2004 CSA C22.2.61010.1:2005
Double/reinforced insulation, 2500 V rms isolation voltage	Basic insulation per CSA 60950-1-03 and IEC 60950-1, 800 V rms (1131 V peak) maximum working voltage Reinforced insulation per CSA 60950-1-03 and IEC 60950-1, 400 V rms (566 V peak) maximum working voltage	Reinforced insulation, 560 V peak	Reinforced insulation, 400 V rms maximum working voltage
File E214100	File 205078	File 2471900-4880-0001	Certificate U8V 05 06 56232 002

[1] In accordance with UL 1577, each ADuM130x is proof tested by applying an insulation test voltage ≥3000 V rms for 1 sec (current leakage detection limit = 5 µA).
[2] In accordance with DIN V VDE V 0884-10, each ADuM130x is proof tested by applying an insulation test voltage ≥1050 V peak for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN V VDE V 0884-10 approval.

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 6.

Parameter	Symbol	Value	Unit	Conditions
Rated Dielectric Insulation Voltage		2500	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L(I01)	7.7 min	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	8.1 min	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 INSULATION CHARACTERISTICS

These isolators are suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The * marking on packages denotes DIN V VDE V 0884-10 approval for 560 V peak working voltage.

Table 7.

Description	Conditions	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to III	
For Rated Mains Voltage ≤ 400 V rms			I to II	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	560	V peak
Input-to-Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{PR}$, 100% production test, $t_m = 1$ sec, partial discharge < 5 pC	V_{PR}	1050	V peak
Input-to-Output Test Voltage, Method A	$V_{IORM} \times 1.6 = V_{PR}$, $t_m = 60$ sec, partial discharge < 5 pC	V_{PR}		
After Environmental Tests Subgroup 1			896	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{PR}$, $t_m = 60$ sec, partial discharge < 5 pC		672	V peak
Highest Allowable Overvoltage	Transient overvoltage, $t_{TR} = 10$ seconds	V_{TR}	4000	V peak
Safety-Limiting Values	Maximum value allowed in the event of a failure (see Figure 3)			
Case Temperature		T_S	150	°C
Side 1 Current		I_{S1}	265	mA
Side 2 Current		I_{S2}	335	mA
Insulation Resistance at T_S	$V_{IO} = 500$ V	R_S	$>10^9$	Ω

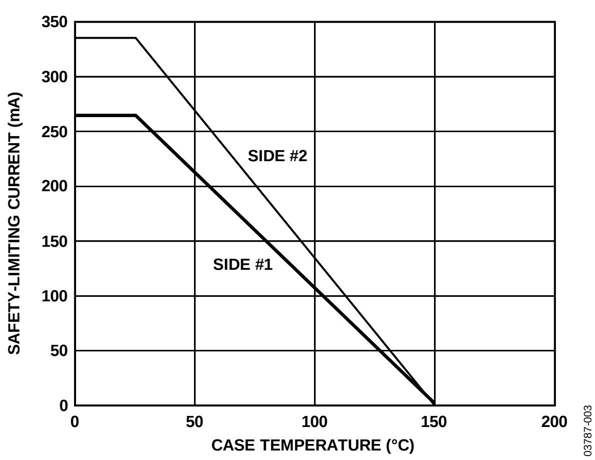


Figure 3. Thermal Derating Curve, Dependence of Safety-Limiting Values with Case Temperature per DIN V VDE V 0884-10

RECOMMENDED OPERATING CONDITIONS

Table 8.

Parameter	Rating
Operating Temperature (T_A)	−40°C to +105°C
Supply Voltages (V_{DD1}, V_{DD2})[1]	2.7 V to 5.5 V
Input Signal Rise and Fall Times	1.0 ms

[1] All voltages are relative to their respective ground. See the DC Correctness and Magnetic Field Immunity section for information on immunity to external magnetic fields.

ABSOLUTE MAXIMUM RATINGS

Ambient temperature = 25°C, unless otherwise noted.

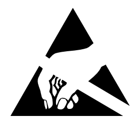
Table 9.

Parameter	Rating
Storage Temperature (T_{ST})	−65°C to +150°C
Ambient Operating Temperature (T_A)	−40°C to +105°C
Supply Voltages (V_{DD1}, V_{DD2})[1]	−0.5 V to +7.0 V
Input Voltage (V_{IA}, V_{IB}, V_{IC}, V_{E1}, V_{E2})[1, 2]	−0.5 V to V_{DDI} + 0.5 V
Output Voltage (V_{OA}, V_{OB}, V_{OC})[1, 2]	−0.5 V to V_{DDO} + 0.5 V
Average Output Current per Pin[3]	
Side 1 (I_{O1})	−23 mA to +23 mA
Side 2 (I_{O2})	−30 mA to +30 mA
Common-Mode Transients[4]	−100 kV/μs to +100 kV/μs

[1] All voltages are relative to their respective ground.
[2] V_{DDI} and V_{DDO} refer to the supply voltages on the input and output sides of a given channel, respectively. See the PC Board Layout section.
[3] See Figure 3 for maximum rated current values for various temperatures.
[4] Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the Absolute Maximum Ratings may cause latch-up or permanent damage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 10. Maximum Continuous Working Voltage[1]

Parameter	Max	Unit	Constraint
AC Voltage, Bipolar Waveform	565	V peak	50-year minimum lifetime
AC Voltage, Unipolar Waveform			
Basic Insulation	1131	V peak	Maximum approved working voltage per IEC 60950-1
Reinforced Insulation	560	V peak	Maximum approved working voltage per IEC 60950-1 and VDE V 0884-10
DC Voltage			
Basic Insulation	1131	V peak	Maximum approved working voltage per IEC 60950-1
Reinforced Insulation	560	V peak	Maximum approved working voltage per IEC 60950-1 and VDE V 0884-10

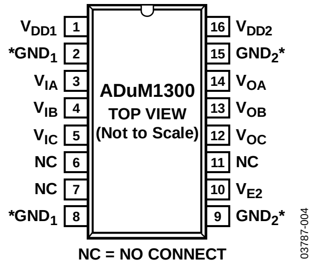
[1] Refers to continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more details.

Table 11. Truth Table (Positive Logic)

V_{Ix} Input[1]	V_{Ex} Input[1, 2]	V_{DDI} State[1]	V_{DDO} State[1]	V_{Ox} Output[1]	Notes
H	H or NC	Powered	Powered	H	
L	H or NC	Powered	Powered	L	
X	L	Powered	Powered	Z	
X	H or NC	Unpowered	Powered	H	Outputs return to the input state within 1 μs of V_{DDI} power restoration.
X	L	Unpowered	Powered	Z	
X	X	Powered	Unpowered	Indeterminate	Outputs return to the input state within 1 μs of V_{DDO} power restoration, if V_{Ex} state is H or NC. Outputs returns to high impedance state within 8 ns of V_{DDO} power restoration, if V_{Ex} state is L.

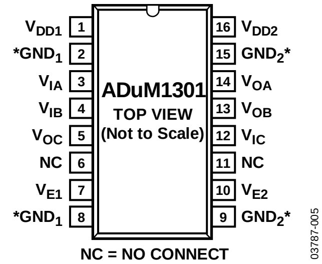
[1] V_{Ix} and V_{Ox} refer to the input and output signals of a given channel (A, B, or C). V_{Ex} refers to the output enable signal on the same side as the V_{Ox} outputs. V_{DDI} and V_{DDO} refer to the supply voltages on the input and output sides of the given channel, respectively.
[2] In noisy environments, connecting V_{Ex} to an external logic high or low is recommended.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



*PIN 2 AND PIN 8 ARE INTERNALLY CONNECTED, AND CONNECTING BOTH TO GND_1 IS RECOMMENDED. PIN 9 AND PIN 15 ARE INTERNALLY CONNECTED, AND CONNECTING BOTH TO GND_2 IS RECOMMENDED.

Figure 4. ADuM1300 Pin Configuration



*PIN 2 AND PIN 8 ARE INTERNALLY CONNECTED, AND CONNECTING BOTH TO GND_1 IS RECOMMENDED. PIN 9 AND PIN 15 ARE INTERNALLY CONNECTED, AND CONNECTING BOTH TO GND_2 IS RECOMMENDED.

Figure 5. ADuM1301 Pin Configuration

Table 12. ADuM1300 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1, 2.7 V to 5.5 V.
2	GND_1	Ground 1. Ground reference for Isolator Side 1.
3	V_{IA}	Logic Input A.
4	V_{IB}	Logic Input B.
5	V_{IC}	Logic Input C.
6	NC	No Connect.
7	NC	No Connect.
8	GND_1	Ground 1. Ground reference for Isolator Side 1.
9	GND_2	Ground 2. Ground reference for Isolator Side 2.
10	V_{E2}	Output Enable 2. Active high logic input. V_{OA}, V_{OB}, and V_{OC} outputs are enabled when V_{E2} is high or disconnected. V_{OA}, V_{OB}, and V_{OC} outputs are disabled when V_{E2} is low. In noisy environments, connecting V_{E2} to an external logic high or low is recommended.
11	NC	No Connect.
12	V_{OC}	Logic Output C.
13	V_{OB}	Logic Output B.
14	V_{OA}	Logic Output A.
15	GND_2	Ground 2. Ground reference for Isolator Side 2.
16	V_{DD2}	Supply Voltage for Isolator Side 2, 2.7 V to 5.5 V.

Table 13. ADuM1301 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1, 2.7 V to 5.5 V.
2	GND_1	Ground 1. Ground reference for Isolator Side 1.
3	V_{IA}	Logic Input A.
4	V_{IB}	Logic Input B.
5	V_{OC}	Logic Output C.
6	NC	No Connect.
7	V_{E1}	Output Enable 1. Active high logic input. V_{OC} output is enabled when V_{E1} is high or disconnected. V_{OC} is disabled when V_{E1} is low. In noisy environments, connecting V_{E1} to an external logic high or low is recommended.
8	GND_1	Ground 1. Ground reference for Isolator Side 1.
9	GND_2	Ground 2. Ground reference for Isolator Side 2.
10	V_{E2}	Output Enable 2. Active high logic input. V_{OA} and V_{OB} outputs are enabled when V_{E2} is high or disconnected. V_{OA} and V_{OB} outputs are disabled when V_{E2} is low. In noisy environments, connecting V_{E2} to an external logic high or low is recommended.
11	NC	No Connect.
12	V_{IC}	Logic Input C.
13	V_{OB}	Logic Output B.
14	V_{OA}	Logic Output A.
15	GND_2	Ground 2. Ground reference for Isolator Side 2.
16	V_{DD2}	Supply Voltage for Isolator Side 2, 2.7 V to 5.5 V.

TYPICAL PERFORMANCE CHARACTERISTICS

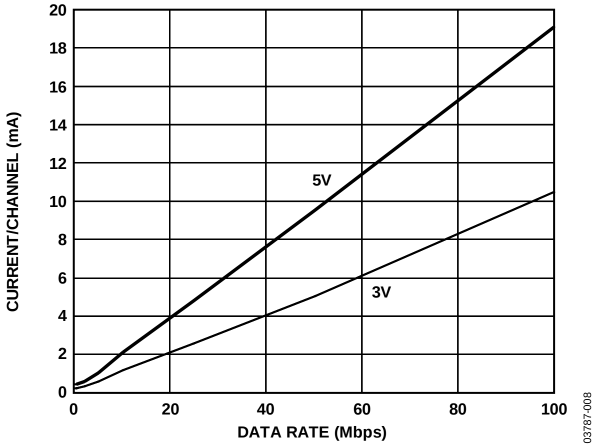


Figure 6. Typical Input Supply Current per Channel vs. Data Rate for 5 V and 3 V Operation

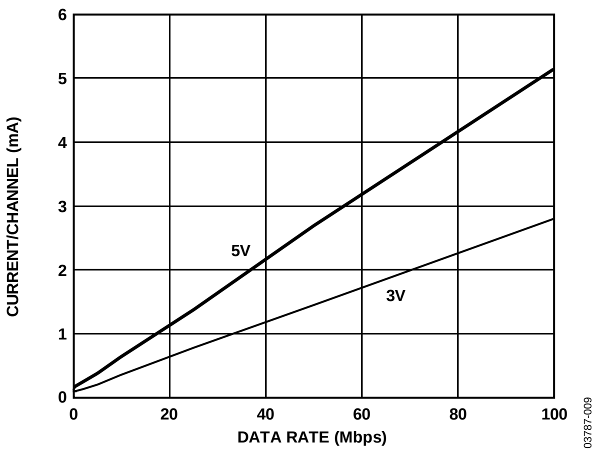


Figure 7. Typical Output Supply Current per Channel vs. Data Rate for 5 V and 3 V Operation (No Output Load)

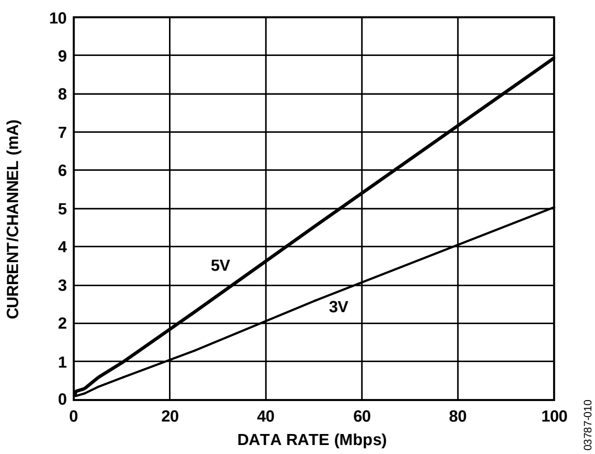


Figure 8. Typical Output Supply Current per Channel vs. Data Rate for 5 V and 3 V Operation (15 pF Output Load)

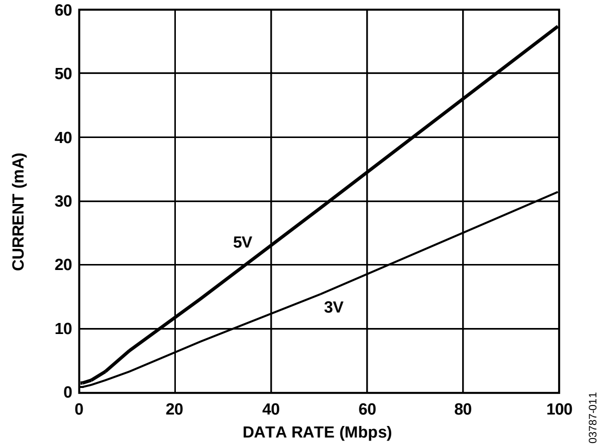


Figure 9. Typical ADuM1300 V_{DD1} Supply Current vs. Data Rate for 5 V and 3 V Operation

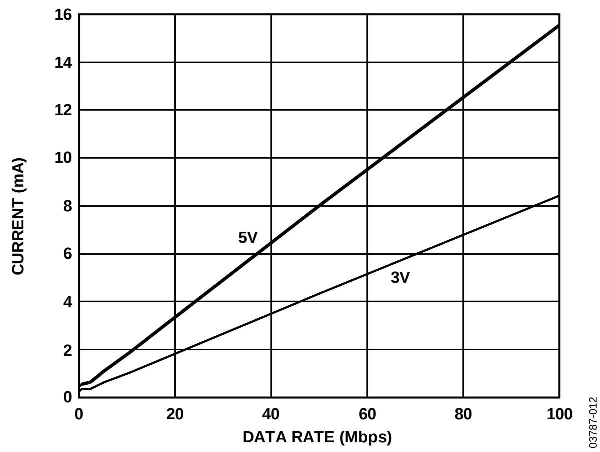


Figure 10. Typical ADuM1300 V_{DD2} Supply Current vs. Data Rate for 5 V and 3 V Operation

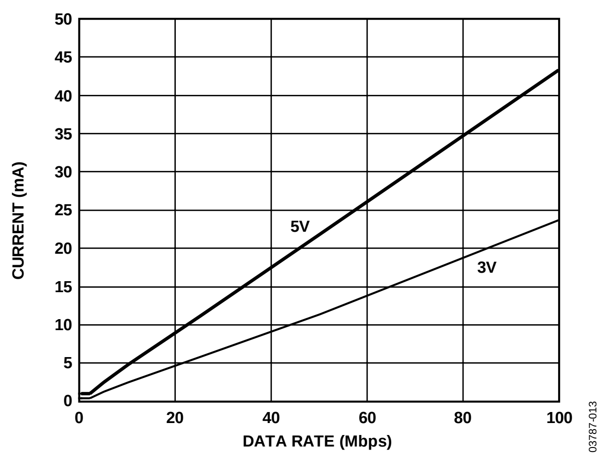


Figure 11. Typical ADuM1301 V_{DD1} Supply Current vs. Data Rate for 5 V and 3 V Operation

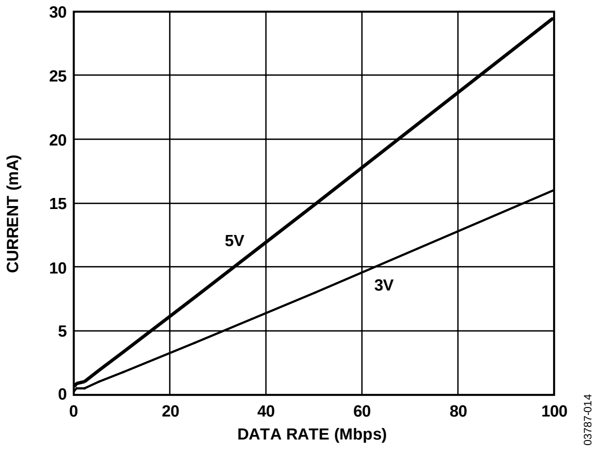


Figure 12. Typical ADuM1301 V_{DD2} Supply Current vs. Data Rate for 5 V and 3 V Operation

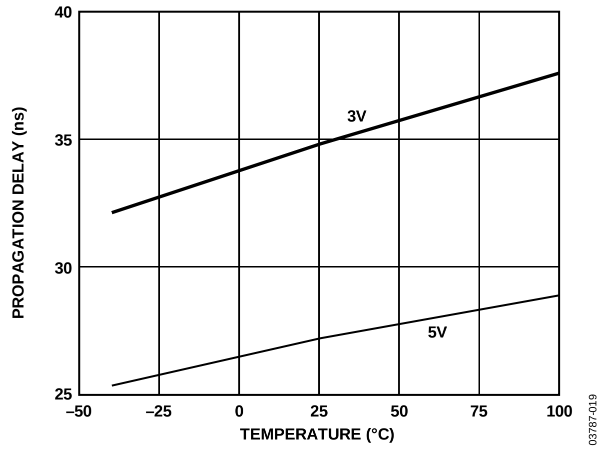


Figure 13. Propagation Delay vs. Temperature, C Grade

APPLICATIONS INFORMATION

PC BOARD LAYOUT

The ADuM130x digital isolator requires no external interface circuitry for the logic interfaces. Power supply bypassing is strongly recommended at the input and output supply pins (see Figure 14). Bypass capacitors are most conveniently connected between Pin 1 and Pin 2 for V_{DD1} and between Pin 15 and Pin 16 for V_{DD2}. The capacitor value should be between 0.01 µF and 0.1 µF. The total lead length between both ends of the capacitor and the input power supply pin should not exceed 20 mm. Bypassing between Pin 1 and Pin 8 and between Pin 9 and Pin 16 should also be considered unless the ground pair on each package side is connected close to the package.

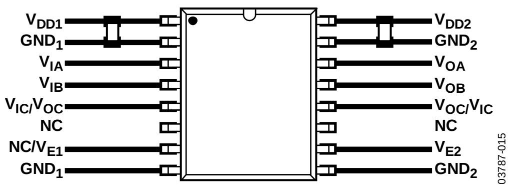


Figure 14. Recommended Printed Circuit Board Layout

In applications involving high common-mode transients, care should be taken to ensure that board coupling across the isolation barrier is minimized. Furthermore, the board layout should be designed such that any coupling that does occur equally affects all pins on a given component side. Failure to ensure this could cause voltage differentials between pins exceeding the absolute maximum ratings of the device, thereby leading to latch-up or permanent damage.

PROPAGATION DELAY-RELATED PARAMETERS

Propagation delay is a parameter that describes the time it takes a logic signal to propagate through a component. The propagation delay to a Logic low output may differ from the propagation delay to a Logic high output.

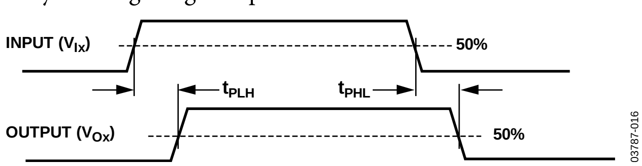


Figure 15. Propagation Delay Parameters

Pulse width distortion is the maximum difference between these two propagation delay values and is an indication of how accurately the timing of the input signal is preserved.

Channel-to-channel matching refers to the maximum amount that the propagation delay differs between channels within a single ADuM130x component.

Propagation delay skew refers to the maximum amount that the propagation delay differs between multiple ADuM130x components operating under the same conditions.

DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

Positive and negative logic transitions at the isolator input cause narrow (~1 ns) pulses to be sent to the decoder via the transformer. The decoder is bistable and is therefore either set or reset by the pulses, indicating input logic transitions. In the absence of logic transitions at the input for more than ~1 µs, a periodic set of refresh pulses indicative of the correct input state are sent to ensure dc correctness at the output. If the decoder receives no internal pulses for more than about 5 µs, the input side is assumed to be unpowered or nonfunctional, in which case the isolator output is forced to a default state (see Table 11) by the watchdog timer circuit.

The ADuM130x is extremely immune to external magnetic fields. The limitation on the magnetic field immunity of the ADuM130x is set by the condition in which induced voltage in the receiving coil of the transformer is sufficiently large enough to either falsely set or reset the decoder. The following analysis defines the conditions under which this may occur. The 3 V operating condition of the ADuM130x is examined because it represents the most susceptible mode of operation.

The pulses at the transformer output have an amplitude greater than 1.0 V. The decoder has a sensing threshold at about 0.5 V, thus establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt)\sum\prod r_n^2;\ n = 1, 2, \ldots, N$$

where:
β is magnetic flux density (gauss).
N is the number of turns in the receiving coil.
r_n is the radius of the n[th] turn in the receiving coil (cm).

Given the geometry of the receiving coil in the ADuM130x and an imposed requirement that the induced voltage be 50% at most of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated as shown in Figure 16.

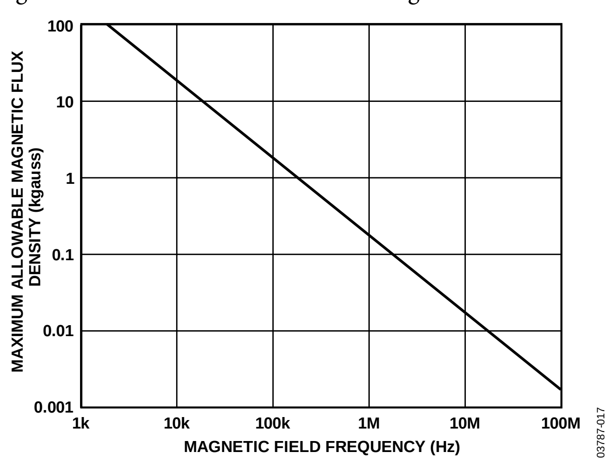


Figure 16. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurs during a transmitted pulse (and has the worst-case polarity), it reduces the received pulse from >1.0 V to 0.75 V—still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances from the ADuM130x transformers. Figure 17 expresses these allowable current magnitudes as a function of frequency for selected distances. The ADuM130x is extremely immune and can be affected only by extremely large currents operated at a high frequency very close to the component. For the 1 MHz example noted, one would have to place a 0.5 kA current 5 mm away from the ADuM130x to affect the operation of the component.

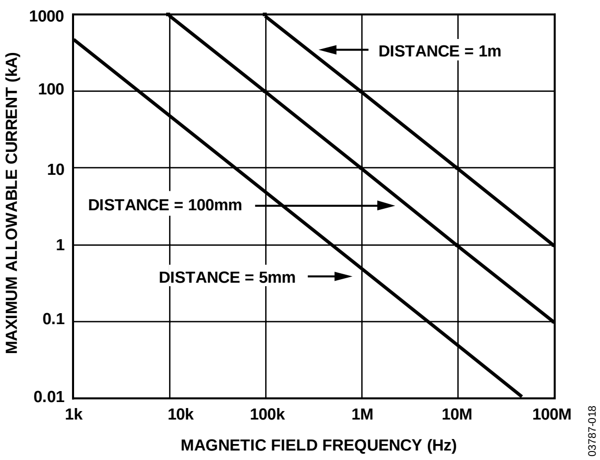


Figure 17. Maximum Allowable Current for Various Current-to-ADuM130x Spacings

Note that at combinations of strong magnetic field and high frequency, any loops formed by printed circuit board traces could induce error voltages sufficiently large enough to trigger the thresholds of succeeding circuitry. Care should be taken in the layout of such traces to avoid this possibility.

POWER CONSUMPTION

The supply current at a given channel of the ADuM130x isolator is a function of the supply voltage, the data rate of the channel, and the output load of the channel.

For each input channel, the supply current is given by

$$I_{DDI} = I_{DDI\,(Q)} \qquad f \leq 0.5\, f_r$$

$$I_{DDI} = I_{DDI\,(D)} \times (2f - f_r) + I_{DDI\,(Q)} \qquad f > 0.5\, f_r$$

For each output channel, the supply current is given by

$$I_{DDO} = I_{DDO\,(Q)} \qquad f \leq 0.5\, f_r$$

$$I_{DDO} = (I_{DDO\,(D)} + (0.5 \times 10^{-3}) \times C_L \times V_{DDO}) \times (2f - f_r) + I_{DDO\,(Q)} \qquad f > 0.5\, f_r$$

where:

$I_{DDI\,(D)}$, $I_{DDO\,(D)}$ are the input and output dynamic supply currents per channel (mA/Mbps).
C_L is the output load capacitance (pF).
V_{DDO} is the output supply voltage (V).
f is the input logic signal frequency (MHz); it is half of the input data rate expressed in units of Mbps.
f_r is the input stage refresh rate (Mbps).
$I_{DDI\,(Q)}$, $I_{DDO\,(Q)}$ are the specified input and output quiescent supply currents (mA).

To calculate the total V_{DD1} and V_{DD2} supply current, the supply currents for each input and output channel corresponding to V_{DD1} and V_{DD2} are calculated and totaled. Figure 6 and Figure 7 provide per-channel supply currents as a function of data rate for an unloaded output condition. Figure 8 provides per-channel supply current as a function of data rate for a 15 pF output condition. Figure 9 through Figure 12 provide total V_{DD1} and V_{DD2} supply current as a function of data rate for ADuM1300/ADuM1301 channel configurations.

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices carries out an extensive set of evaluations to determine the lifetime of the insulation structure within the ADuM130x.

Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage. The values shown in Table 10 summarize the peak voltage for 50 years of service life for a bipolar ac operating condition and the maximum CSA/VDE approved working voltages. In many cases, the approved working voltage is higher than the 50-year service life voltage. Operation at these high working voltages can lead to shortened insulation life in some cases.

The insulation lifetime of the ADuM130x depends on the voltage waveform type imposed across the isolation barrier. The *i*Coupler insulation structure degrades at different rates depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 18, Figure 19, and Figure 20 illustrate these different isolation voltage waveforms, respectively.

Bipolar ac voltage is the most stringent environment. The goal of a 50-year operating lifetime under the ac bipolar condition determines the Analog Devices recommended maximum working voltage.

In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower, which allows operation at higher working voltages while still achieving a 50-year service life. The working voltages listed in Table 10 can be applied while maintaining the 50-year minimum lifetime provided the voltage conforms to either the unipolar ac or dc voltage cases. Any crossinsulation voltage waveform that does not conform to Figure 19 or Figure 20 should be treated as a bipolar ac waveform, and its peak voltage should be limited to the 50-year lifetime voltage value listed in Table 10.

Note that the voltage presented in Figure 19 is shown as sinusoidal for illustration purposes only. It is meant to represent any voltage waveform varying between 0 V and some limiting value. The limiting value can be positive or negative, but the voltage cannot cross 0 V.

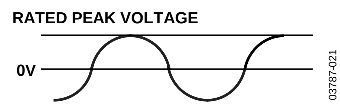


Figure 18. Bipolar AC Waveform

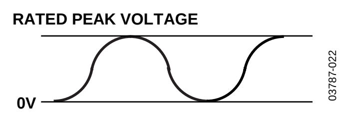


Figure 19. Unipolar AC Waveform

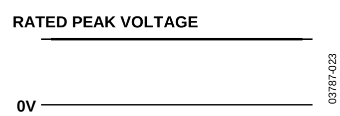


Figure 20. DC Waveform

OUTLINE DIMENSIONS

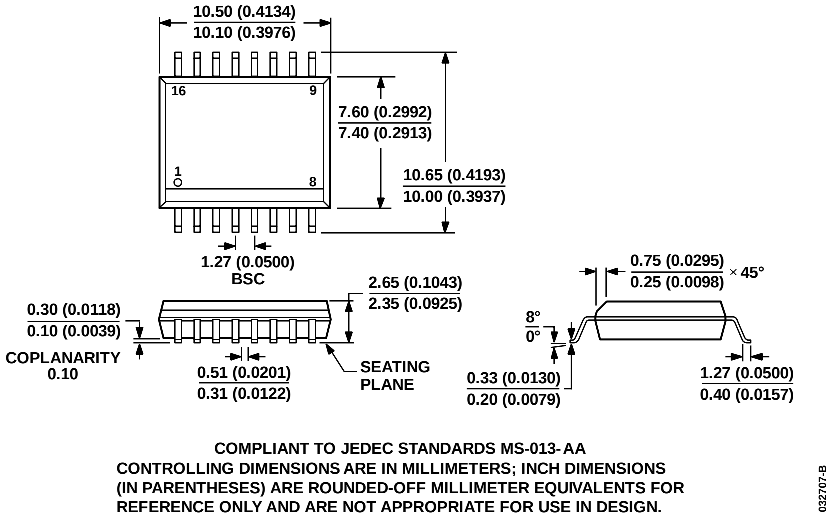


Figure 21. 16-Lead Standard Small Outline Package [SOIC_W]
Wide Body (RW-16)
Dimensions shown in millimeters (and inches)

ORDERING GUIDE

Model	Number of Inputs, V_{DD1} Side	Number of Inputs, V_{DD2} Side	Maximum Data Rate (Mbps)	Maximum Propagation Delay, 5 V (ns)	Maximum Pulse Width Distortion (ns)	Temperature Range (°C)	Package Option[1]
ADuM1300ARW[2]	3	0	1	100	40	−40 to +105	RW-16
ADuM1300BRW[2]	3	0	10	50	3	−40 to +105	RW-16
ADuM1300CRW[2]	3	0	90	32	2	−40 to +105	RW-16
ADuM1300ARWZ[2, 3]	3	0	1	100	40	−40 to +105	RW-16
ADuM1300BRWZ[2, 3]	3	0	10	50	3	−40 to +105	RW-16
ADuM1300CRWZ[2, 3]	3	0	90	32	2	−40 to +105	RW-16
ADuM1301ARW[2]	2	1	1	100	40	−40 to +105	RW-16
ADuM1301BRW[2]	2	1	10	50	3	−40 to +105	RW-16
ADuM1301CRW[2]	2	1	90	32	2	−40 to +105	RW-16
ADuM1301ARWZ[2, 3]	2	1	1	100	40	−40 to +105	RW-16
ADuM1301BRWZ[2, 3]	2	1	10	50	3	−40 to +105	RW-16
ADuM1301CRWZ[2, 3]	2	1	90	32	2	−40 to +105	RW-16

[1] RW-16 = 16-lead wide body SOIC.
[2] Tape and reel are available. The addition of an -RL suffix designates a 13” (1,000 units) tape-and-reel option.
[3] Z = RoHS Compliant Part.

NOTES

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