Single chip 2.4 GHz Transceiver with Embedded ANT protocol

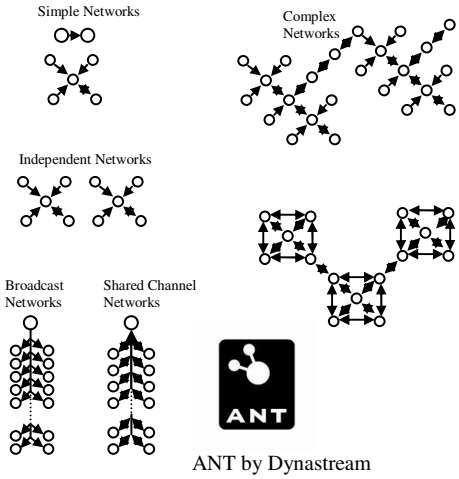
nRF24AP1

FEATURES

- Integrated PAN (Personal Area Network)
- Drop in wireless networking with simple serial interface
- 2.4GHz Worldwide ISM Band
- Ultra-low power (coin cell battery)
- Fully scaleable
- Broadcast, Acknowledged or Burst Data
- Message rates 0.5Hz -> 200Hz (8byte data payload)
- Burst transfer rates up to 20kbps (true data throughput)
- Public and private networks
- 1 Mbps RF data rate
- 125 RF channels

APPLICATIONS

- Sensor Networks
- Industrial Automation
- Home Automation
- Sports Monitoring



GENERAL DESCRIPTION

The nRF24AP1 is an ultra-low power single-chip radio transceiver with embedded ANT protocol for personal area networks. The transceiver's RF operating frequency range falls within the world-wide 2.4 - 2.5 GHz RF ISM band, allowing for regulatory compliance and product sales into global markets.

QUICK REFERENCE DATA

Parameter	Value	Unit
Minimum supply voltage	1.9	V
Maximum output power	0	dBm
Maximum data rate (over the air)	1000	kbps
Temperature range	-40 to +85	°C
Sensitivity	-80	dBm
Average current consumption as low as	40	µA
Peak current consumption TX @-5dBm	13.5mA for 350us	mA
Peak current consumption RX	22mA for 600us	mA
Max # of simultaneous connections[1]	>65000	connections
Max # of simultaneous independent 2-way connections	4	2-way connections
Maximum sustained transfer rate (all data – no overhead)[2]	20	kbps
CR2032 Battery life in a typical sensor application[3]	5	years

Table 1: nRF24AP1 quick reference data

[1] Using Shared Channel Network
[2] Transfer rate refers to data rate of the end application's message payload
[3] Message interval of 2s, 1 hour/day usage

The transceiver consists of the ANT fully integrated protocol engine, frequency synthesizer, power amplifier, crystal oscillator and modulator, and can be interfaced to a host microcontroller over either a synchronous or asynchronous serial interface. Designed to run on a wrist-watch coin cell battery, current consumption of the device is extremely low - a typical sensor application can operate on approximately 40µA average current consumption. Short, low peak current transitions are battery friendly.

The embedded ANT protocol makes for easy, low cost integration. Eliminating the need for 3rd party RF protocol implementation, the on-chip ANT protocol combined with the 2.4GHz transceiver enables system and application developers to interact with the nRF24AP1 as a black box wireless solution. The simple serial interface (asynchronous or synchronous) to the device allows for flexibility and scalability from ultra-low power sensors (40µA) through to higher data rate (20kbps) applications implemented in a multitude of network configurations. Networks can be scaled from as little as two nodes to thousands. With 2^{32} unique IDs, multiple radio frequencies, public and private network management and scalable data rates, an unlimited number of network configurations and applications are possible.

Prior to reading this document, the "ANT Message Protocol and Usage" document should be read to gain understanding of the ANT protocol capabilities.

ORDERING INFORMATION

Type Number	Description	Version
nRF24AP1	24 pin QFN 5x5, lead free (green)	A
nRF24AP1-EVKIT	4 node network evaluation and development kit	A

Table 2: nRF24AP1 ordering information

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1. BLOCK DIAGRAM

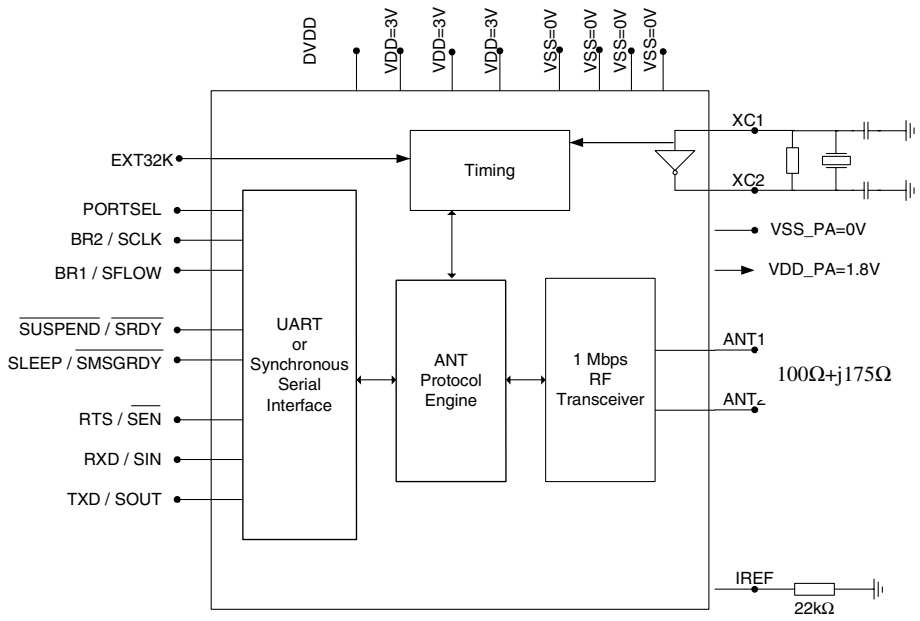


Figure 1: nRF24AP1 with external components.

The “ANT Protocol Engine” shown in Figure 1 is described in the “ANT Message Protocol and Usage” document.

2. PIN FUNCTIONS

Pin	Name	Pin function	Description
1	BR2 / SCLK	Digital IO	Asynchronous baud rate select / Synchronous clock signal
2	BR1 / SFLOW	Digital Input	Asynchronous baud rate select / Synch. Bit or byte flow select
3	EXT32K	Digital Input	Optional External 32kHz clock, tied to GND when not used
4	RXD / SIN	Digital Input	Asynchronous UART receive data / Synchronous receive data
5	TXD / SOUT	Digital Output	Asynchronous UART transmit data / Synchronous transmit data
6	$\overline{\text{SUSPEND}}$ / $\overline{\text{SRDY}}$	Digital Input	Asynchronous suspend control / Synchronous port ready signal
7	SLEEP / $\overline{\text{SMSGRDY}}$	Digital Input	Asynchronous sleep enable / Synchronous message ready signal
8	RTS / $\overline{\text{SEN}}$	Digital Output	Asynchronous flow control RTS /Synchronous serial enable
9	DVDD	Power Output	Positive Digital Supply output for de-coupling purposes
10	VSS	Power	Ground (0V)
11	XC2	Analog Output	Crystal Pin 2
12	XC1	Analog Input	Crystal Pin 1
13	VDD_PA	Power Output	Power Supply (+1.8V) to Power Amplifier
14	ANT1	RF	Antenna interface 1
15	ANT2	RF	Antenna interface 2
16	VSS_PA	Power	Ground (0V)
17	VDD	Power	Power Supply (+3V DC)
18	VSS	Power	Ground (0V)
19	IREF	Analog Input	Reference current
20	VSS	Power	Ground (0V)
21	VDD	Power	Power Supply (+3V DC)
22	VSS	Power	Ground (0V)
23	PORTSEL	Digital Input	Asynchronous / Synchronous port selection
24	VDD	Power	Power Supply (+3V DC)

Table 3: nRF24AP1 pin function

3. PIN ASSIGNMENT

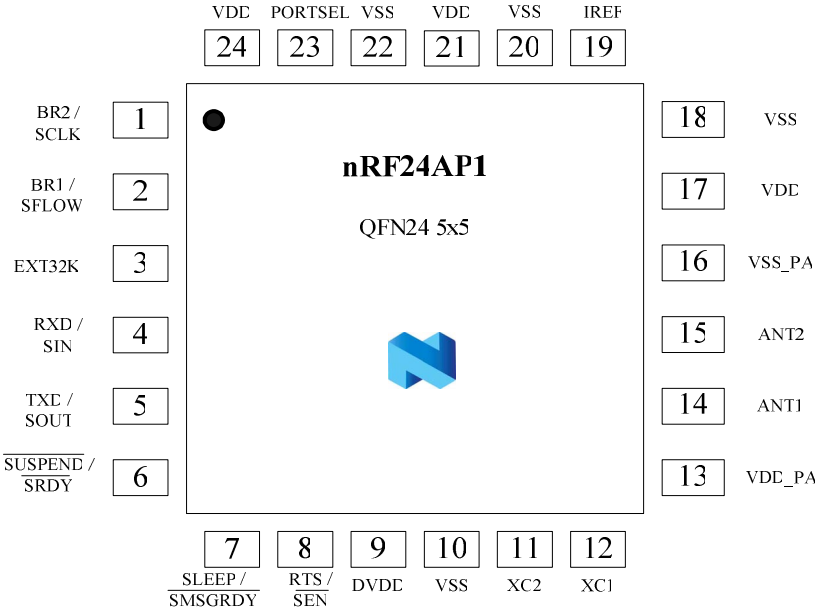


Figure 2: nRF24AP1 pin assignment (top view) for a QFN24 5x5 package.

4. ELECTRICAL SPECIFICATIONS

Conditions: VDD = +3V, VSS = 0V, TA = - 40ºC to + 85ºC

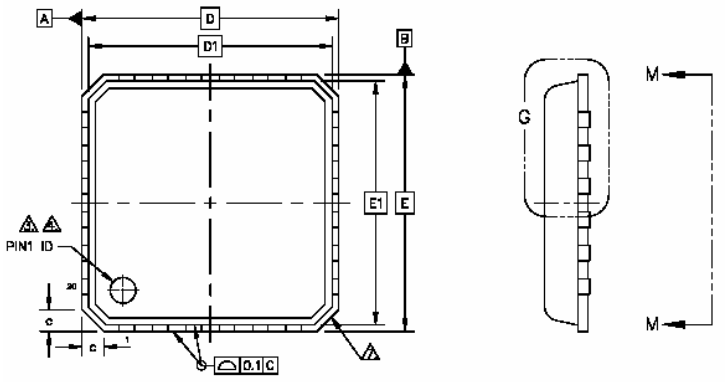
Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
	Operating conditions					
VDD	Supply voltage		1.9	3.0	3.6	V
TEMP	Operating Temperature		-40	+27	+85	ºC
	Digital input pin					
V_{IH}	HIGH level input voltage		0.7VDD		VDD	V
V_{IL}	LOW level input voltage		Vss		0.3VDD	V
	Digital output pin					
V_{OH}	HIGH level output voltage (I_{OH}=-0.5mA)		VDD- 0.3		VDD	V
V_{OL}	LOW level output voltage (I_{OL}=0.5mA)		Vss		0.3	V
	Crystals and clocks					
f_{XTAL}	RF Crystal frequency			16		MHz
$f_{XTAL-OFFSET}$	RF Crystal offset (Initial, Temp & Aging)				30	PPM
f_{EXT32K}	EXT32K – external 32.768kHz clock			32.768		kHz
$f_{EXT32K-ERROR}$	Maximum error for 32.768kHz clock				50	PPM
	Synchronous Serial Timing					
sclk freq.	Synchronous clock frequency (byte mode)			150-175		kHz
$t_{ReadValid}$	Data is valid on read before low to high transition on the clock (byte mode)		0.5			µs
$t_{WriteValid}$	Data must be valid on write within this time after a high to low transition on the clock (byte mode)				2	µs
t_{SRDY_MinLow}	Minimum $\overline{\text{SRDY}}$ low time		2.5			µs
t_{Reset}	Synchronous Reset. $\overline{\text{SRDY}}$ falling edge to $\overline{\text{SMSGRDY}}$ falling edge		250			µs
	General RF conditions					
f_{OP}	Operating frequency	1)	2400		2524	MHz
$F_{CHANNEL}$	Channel spacing			1		MHz
Δf	Frequency deviation			±156		kHz
	Current Consumption					
I_{Idle}	No active channels – No communications			2		µA
I_{Peak}	Peak Current consumption, RX	2)		22		mA
I_{PeakTX}	Peak Current – TX @ 0dBm	3)		16		mA
	Transmitter operation					
P_{RF}	Maximum Output Power	4)		0	+4	dBm
P_{RFC}	RF Power Control Range		16	20		dB
P_{RFCR}	RF Power Control Range Resolution				±3	dB
P_{BW}	20dB Bandwidth for Modulated Carrier				1000	kHz
P_{RF2}	2^{nd} Adjacent Channel Transmit Power 2MHz				-20	dBm
P_{RF3}	3^{rd} Adjacent Channel Transmit Power 3MHz				-40	dBm
I_{VDD}	Supply peak current @ 0dBm output power	4)		16		mA
I_{VDD}	Supply peak current @ -20dBm output power	4)		13		mA
	Receiver operation					
I_{VDD}	Supply peak current receive mode	4)		22		mA
RX_{SENS}	Sensitivity at 0.1%BER (@1000kbps)			-80		dBm
C/I_{CO}	C/I Co-channel			10/4		dB
C/I_{1ST}	1^{st} Adjacent Channel Selectivity C/I 1MHz			-20/0		dB
C/I_{2ND}	2^{nd} Adjacent Channel Selectivity C/I 2MHz			-37/-20		dB
C/I_{3RD}	3^{rd} Adjacent Channel Selectivity C/I 3MHz			-43/-30		dB

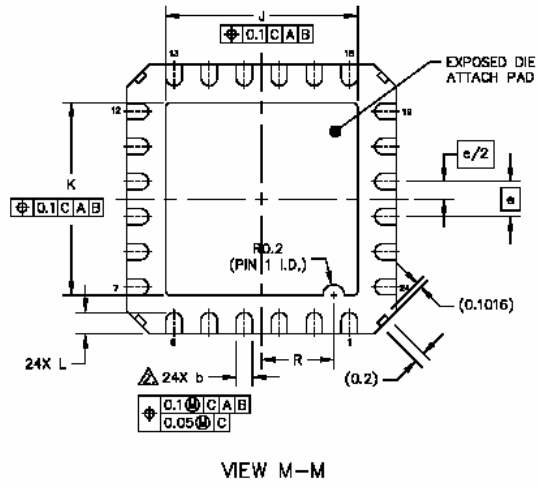
1) Usable band is determined by local regulations
2) Time of Maximum Current consumption in RX is typical 600us and maximum 960us
3) Time of Maximum TX Only Current is typical 350us and maximum 350us.
4) Antenna load impedance = 100Ω+j175Ω

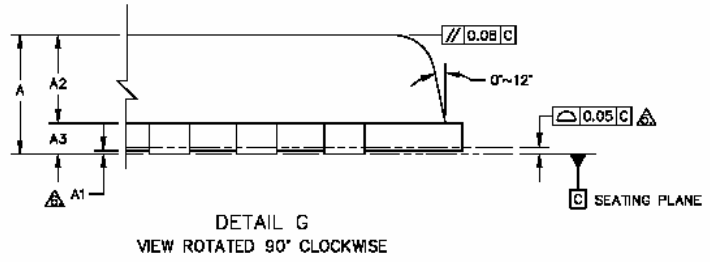
Table 4: nRF24AP1 RF specifications

5. PACKAGE OUTLINE

nRF24AP1 uses the GREEN QFN24 5x5 package, with matt tin plating.







Package Type		A	A_1	A2	b	D/E	D1/E1	e	J	K	L	R
Punch QFN24 (5x5 mm)	**Min**	0.8	0.0	0.65	0.25				3.47	3.47	0.3	1.235
	typ.		0.02		0.3	5 BSC	4.75	0.65 BSC	3.57	3.57	0.4	1.335
	Max	0.9	0.05	0.69	0.35		BSC		3.67	3.67	0.5	1.435

Figure 3: nRF24AP1G GREEN Package outline.

6. ABSOLUTE MAXIMUM RATINGS

Supply voltages
VDD ..... - 0.3V to + 3.6V
VSS 0V

Input voltage
V_I ..... - 0.3V to VDD + 0.3V

Output voltage
V_O ..... - 0.3V to VDD

Total Power Dissipation
P_D (T_A=85°C) 90mW

Temperatures
Operating Temperature…. - 40°C to + 85°C
Storage Temperature……. - 40°C to + 125°C

Note: Stress exceeding one or more of the limiting values may cause permanent damage to the device.

ATTENTION!
Electrostatic Sensitive Device
Observe Precaution for handling.

Glossary of Terms

Term	Description
Acknowledged Data	Master sends an acknowledged packet in place of broadcast
ANT	Ultra-low power embedded RF protocol
Broadcast Data	Default transmission type. Data sent on every time slot
Burst Data	Bulk data transmission between two nodes
Channel	Basic building block of ANT. Connects two devices together
Device ID	Device ID – Identifier for the master end of the channel
Device Number	Device Number is a subcomponent of Device ID, uniquely identifying this device
Device Type	Device Type is a subcomponent of Device ID, uniquely identifying the type of this device
Forward Channel	Data transmission from Master to Slave on a channel
GFSK	Gaussian Frequency Shift Keying
HOST MCU	The MCU which interfaces and controls the nRF24AP1
ISM	Industrial-Scientific-Medical
ISM Band	Industrial, Scientific and Medical Band
Manufacturer ID	Manufacturer ID is a subcomponent of Device ID, uniquely identifying the manufacturer of this device
Master	Primary transmitter of the ANT network channel
MCU	Micro controller unit
Message Data rate	Number of messages per second sent over a channel
Message Payload	User portion of a data packet. Each data packet contains a payload of 8 bytes.
Message	Data packet sent over a channel from one device to another
Networks	A group of ANT nodes connected together via channels forms a network in which the nodes may communicate with one another
Node	An application running on a host controller connected to an nRF24AP1, which communicates with other ANT nodes.
Pairing	The process in which a Slave obtains the Master's ID in order to establish communications.
Reverse Channel	Data transmission from Slave to Master on a channel
RF data rate	The on air data rate. This rate is 1Mbps.
RF Frequency	RF Frequency used for communications. The nRF24AP1 can be configured to one of 125 different RF frequencies.
RX	Receive
Slave	Primary receiver of the ANT network channel
TX	Transmit

Table 5: Glossary

7. ARCHITECTURAL OVERVIEW

The nRF24AP1 is a single-chip silicon solution that integrates a 2.4GHz transceiver and the ANT RF protocol stack. The ANT protocol stack is stored on-chip and is executed by the nRF24AP1's internal MCU core.

Functionally, the nRF24AP1 is composed of 4 main building blocks as shown in Figure 1. Together, the 4 blocks enable the drop-in RF and protocol solution. As shown, the 4 main blocks are the serial interface, the timing interface, the ANT protocol engine, and the RF transceiver. Both the ANT protocol engine and the RF transceiver are embedded within the device and interact with the external host environment through a UART or synchronous serial interface. This functional approach allows the nRF24AP1 to be treated as a black box wireless solution from the system application perspective. Integration of an RF protocol with the RF physical layer is not required. Application developers provides channel configuration and message data information to the device through the serial interface, and the nRF24AP1 executes the configuration and sends/receives the message data packets over the air to other waiting devices.

ANT is a 2.4GHz bidirectional wireless Personal Area Network (PAN) communications technology optimized for transferring low data-rate, low latency data between multiple ANT-enabled devices. The ultra-low power consumption of ANT guarantees an extended battery life even from low capacity supplies such as a coin cell battery, such as are required for heart rate monitors, bicycle computers, and wrist watches. The small size and low-cost implementation of ANT proves essential in allowing effortless integration into the tiny form factor of wrist watches, PDAs, and mobile phones.

The ANT – HOST interface has been designed with utmost simplicity in mind so that it can be easily and quickly implemented into new devices and applications. The encapsulation of the wireless protocol complexity within the ANT chipset vastly reduces the burden on the application host controller, allowing a low-cost 4-bit or 8-bit Microcontroller (MCU) to establish and maintain complex wireless networks with remote devices. Data transfers can be scheduled in a deterministic or ad-hoc fashion, and a burst mode allows for the efficient transfer of large amounts of stored data to and from a PC or other computing device. The ANT system aggressively balances functionality, cost, size, and power consumption within the constraints of a mobile Personal Area Network.

The ANT protocol implements layers 1-4 of the OSI networking stack as well as automatically providing session authentication of network devices. For description of layer 3 and 4, please refer to the "ANT Message Protocol and Usage" document.

8. ANT INTERFACE

8.1 Physical Layer – Serial Interfacing

The ANT serial interface between host controller and nRF24AP1 can be implemented over either a synchronous or asynchronous connection, which can be selected by the product developer as preferred for a given implementation. The precise details of the physical and electrical interface are provided in this document along with signaling specifics and basic message formats.

8.2 ANT Message Summary

The table in Section 8.3 summarizes the message types employed between the host controller and the nRF24AP1, which are used to establish and maintain RF connections to remote devices. Further details of the message fields and data contents can be found in the 'ANT Message Protocol and Usage' document.

8.3 Message Summary

Class	Type	ANT PC Interface Function	Response	From	Len	Msg ID	Data 1	Data 2	Data 3	Data 4	Data 5	Data 6	Data 7	Data 8	Data 9
Channel Event Messages	Channel Response / Event	->ChannelEventFunc(Chan, MessageCode) or ->ResponseFunc(Chan, MsgID);	-	ANT	3	0x40	Channel Number	Message ID	Message Code						
Requested Response Messages	Channel Status	->ResponseFunc(Chan,0x52)	-	ANT	2	0x52	Channel Number	Channel Status							
	Channel ID	->ResponseFunc(Chan,0x51)	-	ANT	5	0x51	Channel Number	Device Number		Device Type ID	Man ID				
	ANT Version	->ResponseFunc(-, 0x3D)	-	ANT	9	0x3D	Ver0	Ver1	Ver2	Ver3	Ver4	Ver5	Ver6	Ver7	Ver8
	Capabilities	->ResponseFunc(-, 0x54)	-	ANT	4	0x54	Max Channels	Max Networks	Standard Options	Advanced Options					
Config. Messages	Unassign Channel	ANT_UnAssignChannel()	Yes	HOST	1	0x41	Channel Number								
	Assign Channel	ANT_AssignChannel()	Yes	HOST	3	0x42	Channel Number	Channel Type	Network Number						
	Channel ID	ANT_SetChannelID()	Yes	HOST	5	0x51	Channel Number	Device Number		Device Type ID	Man ID				
	Channel Period	ANT_SetChannelPeriod()	Yes	HOST	3	0x43	Channel Number	Messaging Period							
	Search Timeout	ANT_SetChannelSearchTimeout()	Yes	HOST	2	0x44	Channel Number	Search Timeout							
	Channel RF Frequency	ANT_SetChannelRFFreq()	Yes	HOST	2	0x45	Channel Number	RF Frequency							
	Set Network	ANT_SetNetworkKey()	No	HOST	9	0x46	Net #	Key 0	Key 1	Key 2	Key 3	Key 4	Key 5	Key 6	Key 7
	Transmit Power	ANT_SetTransmitPower()	Yes	HOST	2	0x47	0	TX Power							
Test Mode	CW Init	ANT_InitCWTestMode()	Yes	HOST	1	0x53	0								
	CW Test	ANT_SetCWTestMode()	Yes	HOST	3	0x48	0	TX Power	RF Freq						
Control Messages	SystemReset	ANT_ResetSystem()	No	HOST	1	0x4A	0								
	Open Channel	ANT_OpenChannel()	Yes	HOST	1	0x4B	Channel Number								
	Close Channel	ANT_CloseChannel()	Yes	HOST	1	0x4C	Channel Number								
	Request Message	ANT_RequestMessage()	Yes	HOST	2	0x4D	Channel Number	Message ID							
Data Messages	Broadcast Data	ANT_SendBroadcastData() ->ChannelEventFunc(Chan, EV)	No	ANT/ HOST	9	0x4E	Channel Number	Data0	Data1	Data2	Data3	Data4	Data5	Data6	Data7
	Acknowledge Data	ANT_SendAcknowledgedData() ->ChannelEventFunc(Chan, EV)	No	ANT/ HOST	9	0x4F	Channel Number	Data0	Data1	Data2	Data3	Data4	Data5	Data6	Data7
	Burst Transfer Data	ANT_SendBurstTransferPacket() ->ChannelEventFunc(Chan, EV)	No	ANT/ HOST	9	0x50	Sequence/ Channel Number	Data0	Data1	Data2	Data3	Data4	Data5	Data6	Data7

9. APPLICATION SPECIFIC CURRENT CONSUMPTION

Symbol	Parameter (condition)	Typ.	Units
I_{Idle}	No active channels – No communications	2	µA
$I_{Suspend}$	Asynchronous suspend Activated	2	µA
$I_{Base-Ext}$	Active base current when EXT32K used	35	µA
$I_{Base-Int}$	Active base current with no EXT32K	75	µA
$I_{MessageTX}$	Average RF Current / TX Message	9	µA
$I_{MessageRX}$	Average RF Current / RX Message	15	µA
$I_{MessageAck}$	Average RF Current / Acknowledge Message	43	µA
$I_{MessageSync}$	Average Synchronous Message Currrent	5	µA
$I_{Message50k}$	Average Asynchronous 50kbaud Message Current	7.5	µA
$I_{Message38.4k}$	Average Asynchronous 38.4kbaud Message Current	9.5	µA
$I_{Message19.2k}$	Average Asynchronous 19.2kbaud Message Current	19	µA
$I_{Message4800}$	Average Asynchronous 4800 baud Message Current	75	µA
I_{Peak}	Peak Current consumption, RX	22	mA
I_{PeakTX}	Peak Current – TX @ 0dBm	16	mA
I_{Ave}	Broadcast TX@ 0.5Hz synchronous,EXT32K	42	µA
I_{Ave}	Broadcast TX @ 2 Hz synchronous,EXT32K	65	µA
I_{Ave}	Broadcast RX @ 0.5Hz synchronous,EXT32K	45	µA
I_{Ave}	Acknowledged @ 0.5 Hz synchronous,EXT32K	60	µA
I_{Ave}	Burst[1] continuous @ 15kbps, synchronous	4.5	mA
I_{Ave}	Burst[1] continuous @ 20kbps	6	mA
I_{Ave}	Broadcast TX @ 250Hz (16kbps)	3.4	mA

Table 6: Application specific current consumption

[1] Burst traffic based on Nordic Semiconductors ShockBurst™ technology

10. ASYNCHRONOUS SERIAL COMMUNICATION

10.1 Description

This section details the asynchronous serial interface. The figure below shows the interface between ANT (In the documentation that follows ANT shall refer to the nRF24AP1 device and its serial interface) and the HOST MCU. This mode is selected by tying the PORTSEL input low. For details on the alternative synchronous serial interface, refer to Section 11.

10.2 Interconnect

The asynchronous serial interface between ANT and the HOST MCU is shown next:

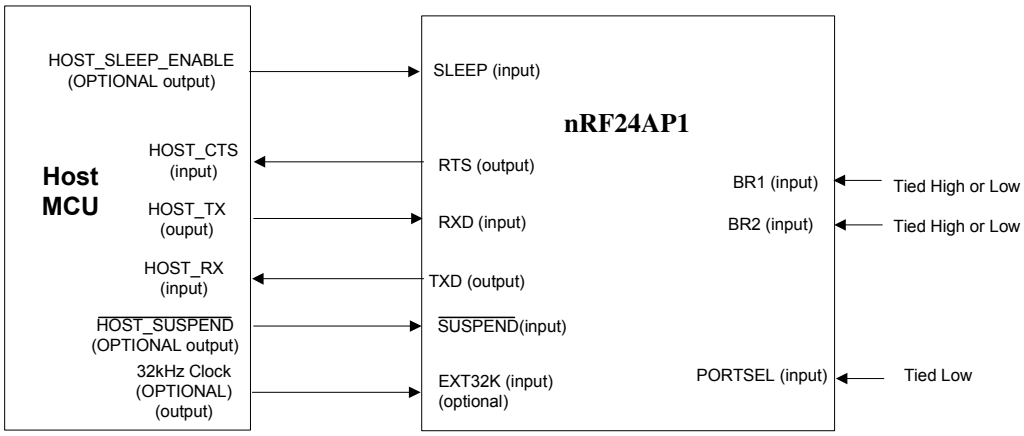


Figure 4: The asynchronous serial interface between ANT and the HOST MCU

10.3 Port Select (PORTSEL)

The PORTSEL signal should be tied low for asynchronous serial mode.

10.4 Speed Select (BR1,BR2)

Please note that all UART communication settings are for one start bit, one stop bit, 8 bits of data and no parity. Data is sent and received LSBit first.

Two Speed Select signals control the baud rate of the asynchronous UART as follows:

BR1	BR2	Baud Rate
0	0	4800
0	1	19200
1	0	38400
1	1	50000

Table 7: Baud rate selection

Baud rate selections have a significant effect on system current consumption. Please study the following table to select the appropriate baud rate.

Estimated current consumption of serial port (uA).

- N = Number of Channels,
- R = Data Rate (# of messages sent per second)

Baud Rate	Single Chip Solution nRF24AP1 Current (uA)**
4800	75*N*R
19200	18.75*N*R
38400	9.4*N*R
50000	7.2*N*R

Table 8: Baud rate vs. current consumption

** Current consumption values shown assume that the SLEEP signal is used. Failure to use this signal will result in an average current consumption of approximately 3mA.

10.5 Suspend Control ($\overline{\text{SUSPEND}}$)

The $\overline{\text{SUSPEND}}$ signal will cause ANT to suspend all RF and serial port activity and power down when the $\overline{\text{SUSPEND}}$ signal goes low. This will happen immediately, regardless of what state the ANT system is currently in. The system will remain in this state until the $\overline{\text{SUSPEND}}$ signal is raised again. When the $\overline{\text{SUSPEND}}$ signal is raised, all previous transactions and configuration is lost – ANT will be in its power-up state. This signal provides support for use in USB applications, where USB devices are required to quickly enter a low power state through hardware control.

10.6 32kHz Clock Signal (EXT32K)

A 32.768kHz clock signal may optionally be provided to the ANT MCU. If this signal is not used, it must be connected to ground. Please see the electrical specification section for external clock specifications. Use of an external clock is recommended for power sensitive applications.

10.7 Asynchronous Port Control (RTS)

When ANT is configured in asynchronous mode, a full duplex asynchronous serial port is provided with flow control for data transmission from the host to ANT. The flow control is performed by the RTS signal, which conforms to standard hardware flow control CMOS signal levels. The signal may therefore be attached to a PC serial port (with use of an RS-232 level shifter), or to any other RS-232 device. The RTS signal is de-asserted for approximately 50 µs after each correctly formatted message has been received. This RTS signal duration is independent of the baud rate. Incorrect messages or partial messages are not acknowledged.
When ANT raises the RTS signal high, the HOST MCU may not send any more data until the RTS signal is lowered again. There is no flow control for data being transmitted

from ANT to the host controller, and therefore the host controller must be able to receive data at any time.

10.8 SLEEP ENABLE (SLEEP)

ANT also has a SLEEP input signal to allow ANT to sleep when the serial port is not required, which allows the ANT system to conserve power. This control mechanism is illustrated below.
Note this signal is essential for power savings in the single chip ANT solution, but has minimal effect for the dual chip solutions[1].

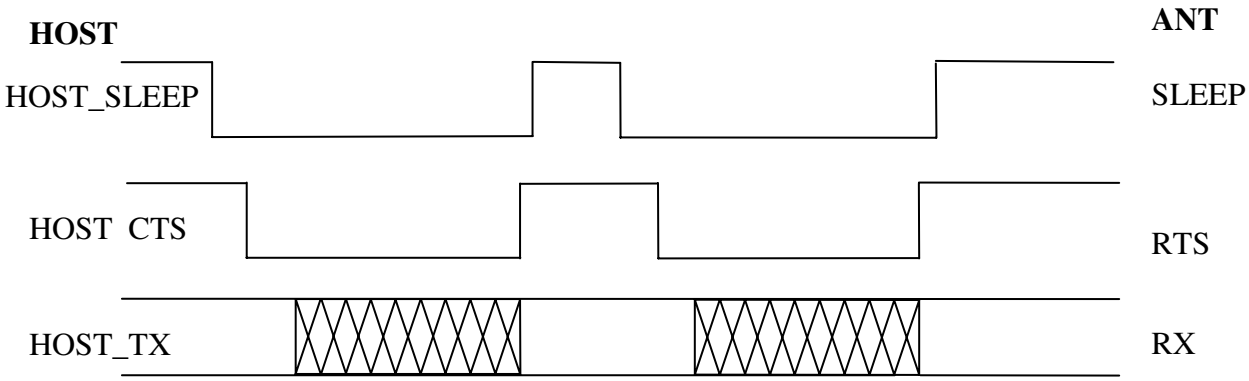


Figure 5: Illustration of usage of the SLEEP signal

If the SLEEP signal is not used, then it must be tied low. In this configuration, the ANT system will never sleep and will always be ready to receive data. This implementation should only be considered for the single chip ANT system when power consumption is not an issue, as the ANT system will consume significantly higher power. (Approximately 3mA higher on average).

Note that the SLEEP and RTS signals only affect data being transferred from the HOST MCU to ANT. ANT will send data to the HOST, when available, regardless of the state of these two signals.

NOTE: The RTS signal is raised by ANT after the last byte of a message has been received, and ANT will therefore lose any bytes that were sent, or in the process of being sent, before the RTS signal is acted upon by the HOST MCU, and the transmission is halted. To avoid this problem, either the messages need to be spaced apart by the HOST MCU, or 0-pad bytes need to be added to the end of each message being transmitted to handle whatever byte pipeline is in place. For example, when considering PC communication, two 0-bytes must be appended to every message, since PCs interpret CTS at the driver rather than the hardware level. ANT will discard 0-pad bytes received. This is usually only an issue when using burst transfers from the HOST to ANT.

[1] Please refer to the 'ANT Message Protocol and Usage' document for descriptions of different solutions

10.9 Link Layer Protocol

10.9.1 Characteristics

The ANT interface protocol has the following characteristics:

- Binary protocol
- Packets are of variable length.
- Each packet contains an 8-bit Checksum
- Asynchronous data is transmitted with 1 start, 8 data bits,1 stop bit and no parity, with standard CMOS level signalling
- Full duplex serial port

10.9.2 Message Structure

ANT and the host MCU communicate by transmitting messages to each other. Each message is formatted as shown below.

SYNC	LENGTH	ID	DATA_1	DATA_2	…	DATA_N	CHECKSUM	Opt. Zero Pad1	Opt. Zero Pad2

Figure 6: ANT message format

Each variable length message is sent starting with the SYNC byte and ending with the CHECKSUM. Bytes are sent LSBit first.

10.9.3 Message Details

Byte #	Bit #	Name	Length	Description
0	7:0	SYNC	1 Byte	Fixed SYNC field = 10100100 (MSB:LSB)
1	-	LENGTH	1 Byte	Number of data byes in the message (Length should be between 1 and 9)
2	-	ID	1 Byte	Data type identifier 0 : Invalid 1..255 : Valid data type ID
3..N+2	-	DATA_1 ... DATA_N	N Bytes	Message data bytes (There may be between 1 and 9 data bytes)
N+3	-	CHECKSUM	1 Byte	XOR of all previous bytes (including SYNC)
N+4, N+5	-	Optional Zero PAD Bytes	1or2 Bytes	Zero PAD bytes may be required in conjunction with flow control when doing BURST transfers. Please see the note in timing diagrams above.

Table 9: Message details

The following is an example of how to encode/decode a message:

ANT_OpenChannel(1) -> SerialData (0xA4, 0x01, 0x4B, 0x01, 0xEF)

Byte #	Name	Length	Data	Description
0	SYNC	1 Byte	0xA4	SYNC is always 0xA4
1	LENGTH	1 Byte	0x01	Number of Data bytes in this message = 1
2	ID	1 Byte	0x4B	ANT_OpenChannel message ID is 0x4B
3	DATA_1	1 Byte	0x01	There is 1 Data Byte in this message: This byte is Channel #. It has been set to Channel = 1
4	CHECKSUM	1 Byte	0xEF	0xA4 xor 0x01 xor 0x4B xor 0x01 = 0xEF

Table 10: Encode/decode example of message

The Command ANT_OpenChannel(1) results in a 5 byte message which is encoded as above, and then sent serially to ANT.

10.10 ANT Messages

Please refer to the “ANT Message Protocol and Usage” document.

11. SYNCHRONOUS SERIAL COMMUNICATION

11.1 Description

This section details the synchronous serial interface between ANT and a HOST MCU. This mode is selected by connecting the PORTSEL input to a logic high. For details on the alternative asynchronous serial interface, refer to Section 9.

Careful attention to reset behavior is required to prevent inadvertent deadlock conditions between the ANT and host modules.

In synchronous mode, ANT uses a half duplex synchronous master serial interface with message flow control. The host must be configured as a synchronous slave. The interface is meant to accommodate either a hardware synchronous slave port or simple I/O control on the host processor. The HOST processor retains full control of the message flow, and thus can halt incoming messages as required.

11.2 Interconnect

The synchronous serial interface between ANT and the HOST MCU is shown below:

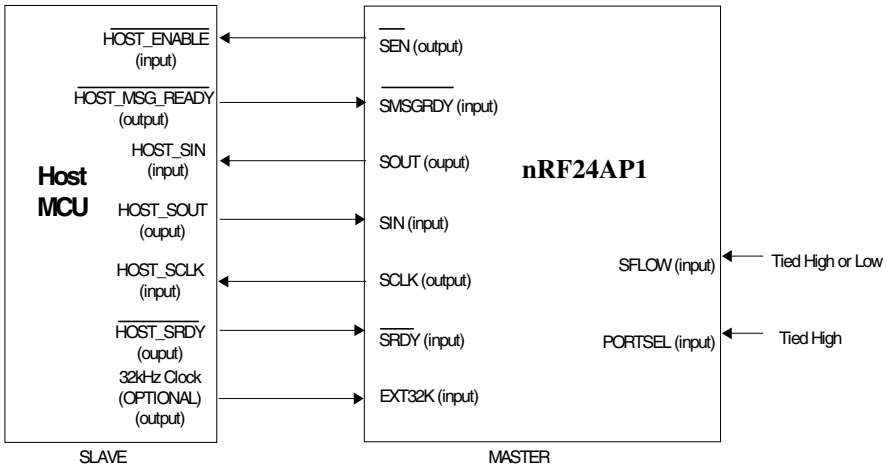


Figure 7: The synchronous serial interface between ANT and the HOST MCU

11.3 Port Select (PORTSEL)

The PORTSEL signal should be tied high for synchronous serial mode.

11.4 Flow Control Select (SFLOW)

The Flow Control Select signal is used to configure the synchronous serial port for either Byte or Bit flow control.

SFLOW	Flow Control
0	Byte Flow Control
1	Bit Flow Control

Table 11: Flow control configuration

Byte flow control assumes that the host contains synchronous communications hardware which can be configured for synchronous slave communications. Bit flow control can be used when all serial lines are taken care of in software on the HOST MCU. The differences between byte and bit flow control are detailed below.

11.5 32kHz Clock Signal (EXT32K)

See description in the asynchronous section, above.

11.6 Operating Mechanism

A basic description of the communications mechanism follows.
By default, the HOST MCU is in receive mode, and ANT is in transmit mode. In this state, the HOST MCU will forward all incoming radio messages to the HOST as they are available. The HOST controls its readiness for incoming messages using the $\overline{\text{SRDY}}$ flow control signal.
If the HOST MCU wishes to send a message to ANT (for example to open a communications channel), it indicates its' wish to enter into transmit mode by asserting the $\overline{\text{SMSGRDY}}$ signal.

$\overline{\text{SRDY}}$ must be in the asserted state for communication to begin.

In either receive or transmit mode, ANT always transmits the first byte of information output from SOUT, which is clocked with the SCLK signal (see Section on Electrical Specifications for details of clock frequency). The LSBit of this byte indicates the direction of future bytes (0 : Message Receive, ANT → HOST; (0 : Message Transmit, HOST → ANT)
If the HOST MCU is in receive mode (default), additional message bytes will be transmitted the same way as the first byte, from ANT → HOST MCU.
If the HOST MCU is in transmit mode, it must output its data to the ANT SIN input at the clock rate provided by the ANT SCLK signal.

11.7 Power Down / Power Up

ANT will automatically place itself into deep sleep mode when all radio channels are closed and there is no activity on the $\overline{\text{SMSGRDY}}$ input signal. The HOST MCU should ensure these conditions during those times that the ANT radio is not required in order to maximize product battery life.

When the HOST MCU wishes to begin communications with ANT, it must first apply a stable clock (if it is supplying the clock), followed by lowering the $\overline{\text{SMSGRDY}}$ signal. At this time ANT will exit from deep sleep. After a wake-up delay (see Electrical Specifications), the HOST MCU can begin to open communication channels.
In the case where the host is unexpectedly reset, while ANT is sending a message to the host, ANT will stall while waiting for $\overline{\text{SRDY}}$ pulses. If the host MCU detects $\overline{\text{SEN}}$ active on startup, it should assert $\overline{\text{SRDY}}$ until ANT deasserts $\overline{\text{SEN}}$. Any data received by the host during this interval may be discarded.

11.8 General Synchronous Port Operation

The synchronous serial port provided by ANT is a half duplex synchronous master, with full flow control in both directions of communication.
Flow control of data transmitted to the HOST MCU is controlled by the $\overline{\text{SRDY}}$ signal, and flow control of data transmitted to ANT is controlled by the master SCLK signal.
By default, the HOST MCU will be in receive mode, and the ANT MCU will be transmit mode. In this state, the HOST MCU will forward all incoming radio messages to the HOST as they are available, based on flow control provided by the host ($\overline{\text{SRDY}}$).
If the HOST MCU wishes to send a message to ANT (for example to open a communications channel), it indicates it wishes to enter into transmit mode by lowering the $\overline{\text{SMSGRDY}}$ signal.
Both transmit and receive transactions, begin with ANT transmitting a control byte to the HOST MCU, which indicates if the rest of the transaction will be a transmit, or a receive transaction.

Data is transmitted LSBit first.

11.9 Link Layer Protocol

11.9.1 Characteristics

The ANT interface protocol has the following characteristics:

- Binary protocol
- Packets are of variable length.
- Each packet contains an 8-bit Checksum
- Data is transmitted LSB first.

11.9.2 Message Structure

ANT and the host MCU communicate by transmitting messages to each other. Each message is formatted as shown below.

SYNC R/W	LENGTH	ID	DATA_1	DATA_2	…	DATA_N	CHECKSUM

Figure 8: The ANT message format

11.9.3 Message Details

Byte	Bit	Name	Length	Description
0	7:1	SYNC	7 bits	Fixed Sync Field = 1010010 (MSB:LSB)
0	0	R/W	1 bit	0 : Write (Message ANT → HOST) 1 : Read (Message HOST → ANT)
1	-	LENGTH	1 Byte	Number of Data bytes in the message (Length should be between 1 and 9)
2	-	ID	1 Byte	Data type indentifier 0 : Invalid 1..255 : Valid data type ID
3..N+2	-	DATA_1	1 Byte	Message data bytes (There may be between 1 and 9 bytes)
N + 3	-	CHECKSUM	1 Byte	XOR of all previous bytes (**including** SYNC)

Table 12: Message details

The following is an example of how to encode a message to send from the HOST to ANT:
ANT_OpenChannel(1)

- ← SerialData (0xA5) // 0xA5 is read indicating that the HOST may send a message to ANT
- → SerialData (0x01, 0x4B, 0x01, 0xEE) // The HOST can then send ANT the 4 byte message

Byte	Name	Length	Direction	Data	Description
0	SYNC	1 Byte	ANT->HOST	0xA5	SYNC is 0xA5 for a HOST->ANT transaction
1	LENGTH	1 Byte	HOST->ANT	0x01	Number of Data bytes in this message = 1
2	ID	1 Byte	HOST->ANT	0x4B	ANT_OpenChannel message ID is 0x4B
3	DATA_1	1 Byte	HOST->ANT	0x01	There is 1 Data Byte in this message: This byte is Channel #. It has been set to Channel = 1
4	CHECKSUM	1 Byte	HOST->ANT	0xEE	0xA5 xor 0x01 xor 0x4B xor 0x01 = 0xEE

Table 13: Example of message from HOST to ANT

The following is an example of how to decode a message received from ANT by the host:

- ← SerialData (0xA4, 0x02, 0x52, 0x01, 0x03, 0xF6) // The HOST receives 6 byte message
- ← Channel_Status(1, 3) // Decodes into a channel status message

Byte	Name	Length	Direction	Data	Description
0	SYNC	1 Byte	ANT->HOST	0xA4	SYNC is 0xA4 for an ANT->HOST transaction
1	LENGTH	1 Byte	ANT->HOST	0x02	Number of Data bytes in this message = 2
2	ID	1 Byte	ANT->HOST	0x52	Channel_Status Message is 0x52
3	DATA_1	1 Byte	ANT->HOST	0x01	There is 2 Data Bytes in this message: This byte is Channel #. Channel = 1
4	DATA_2	1 Byte	ANT->HOST	0x03	This byte is the status. Status = 3, which indicates the channel is tracking.
5	CHECKSUM	1 Byte	ANT->HOST	0xF6	0xA5 xor 0x02 xor 0x52 xor 0x01 xor 0x03 = 0xF6

Table 14: Example of message from ANT to HOST

11.10 ANT Messages

Please refer to the "ANT Message Protocol and Usage" document.

11.11 Synchronous Messaging with Byte Flow Control

Byte flow control mode is used when a synchronous hardware serial port is available. The HOST MCU flow control signal $\overline{\text{SRDY}}$ can either be implemented with a software controlled IO line, or in some cases may be controlled by the HOST's hardware serial port (e.g. EPSON MCU USART support for $\overline{\text{SRDY}}$). Data bits change state on the falling edge of SCLK, and are read on the rising edge of SCLK. This is true for transactions in either direction. The first byte in the transaction sequence is always sent from the ANT MCU to the HOST MCU. The first bit of the first byte (the LSBit of the first byte) dictates the direction for the remaining bytes in the transaction.

11.11.1 ANT → HOST Transaction (Hardware $\overline{\text{SRDY}}$, with SEN signal)

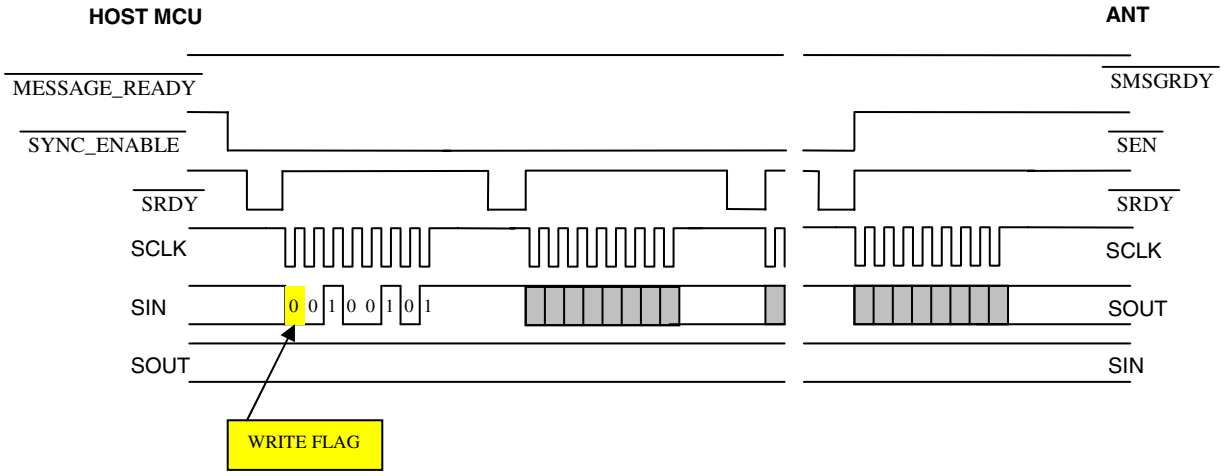


Figure 9: ANT → HOST Transaction (Hardware $\overline{\text{SRDY}}$, with SEN signal)

11.11.2 HOST → ANT Transaction (Hardware $\overline{\text{SRDY}}$, with SEN signal)

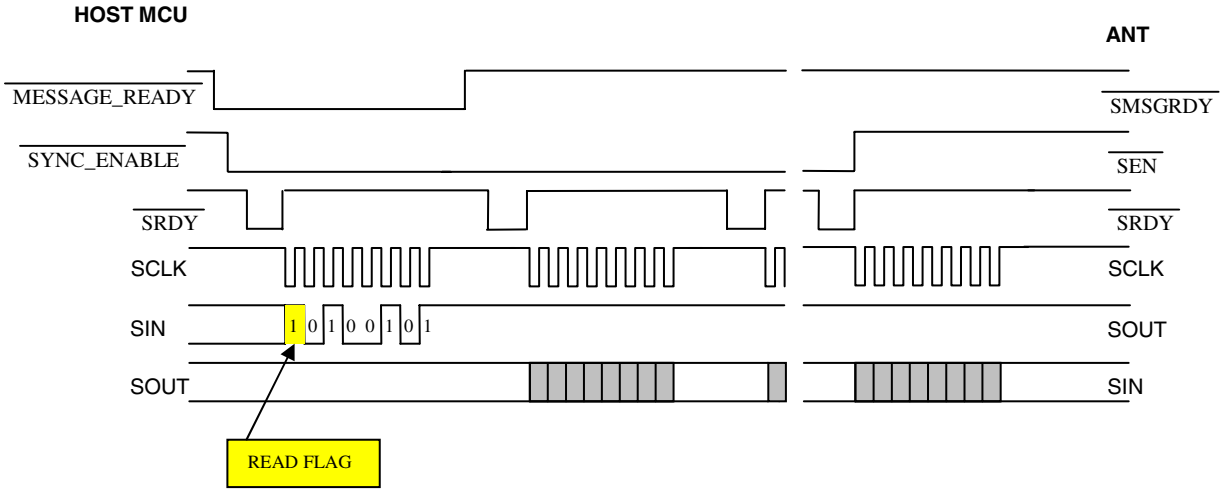


Figure 10: HOST → ANT Transaction (Hardware SRDY, with SEN signal)

11.11.3 ANT → HOST Transaction (Software $\overline{\text{SRDY}}$)

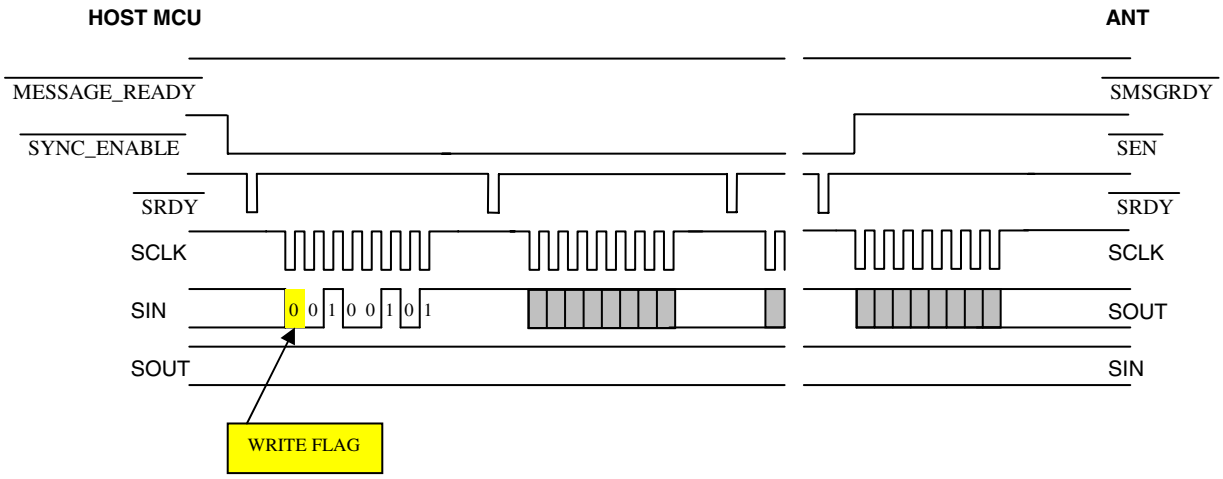


Figure 11: ANT → HOST Transaction (Software SRDY)

11.11.4 HOST → ANT Transaction (Software $\overline{\text{SRDY}}$)

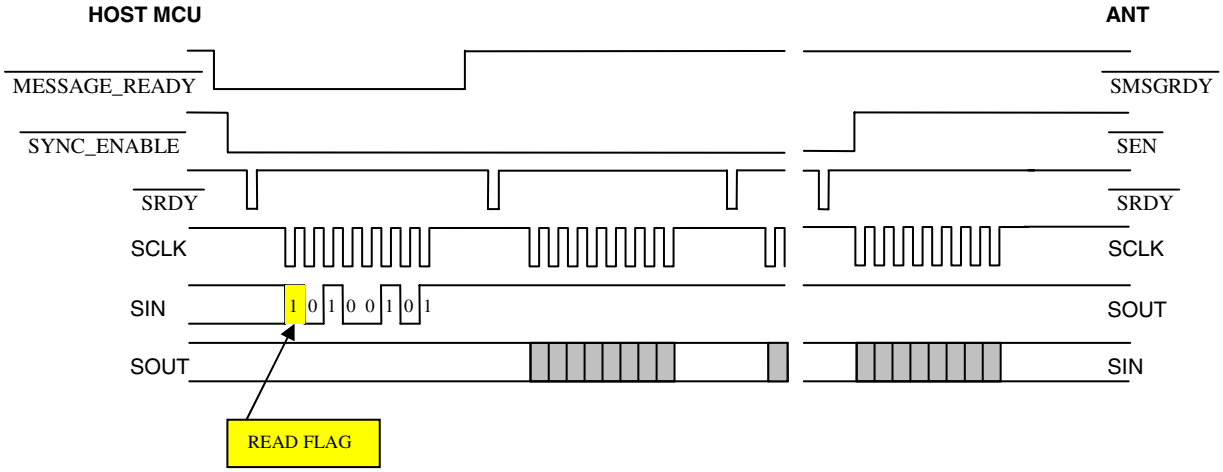


Figure 12: HOST → ANT Transaction (Software SRDY)

Consecutive Messaging

At the end of every byte the HOST will check to make sure the $\overline{\text{SEN}}$ signal is still low, and then assert the $\overline{\text{SRDY}}$ signal for the next byte to proceed. This is still true at the end of a message, where if the $\overline{\text{SEN}}$ signal is still low, then $\overline{\text{SRDY}}$ will be asserted so that a new message transaction can begin.

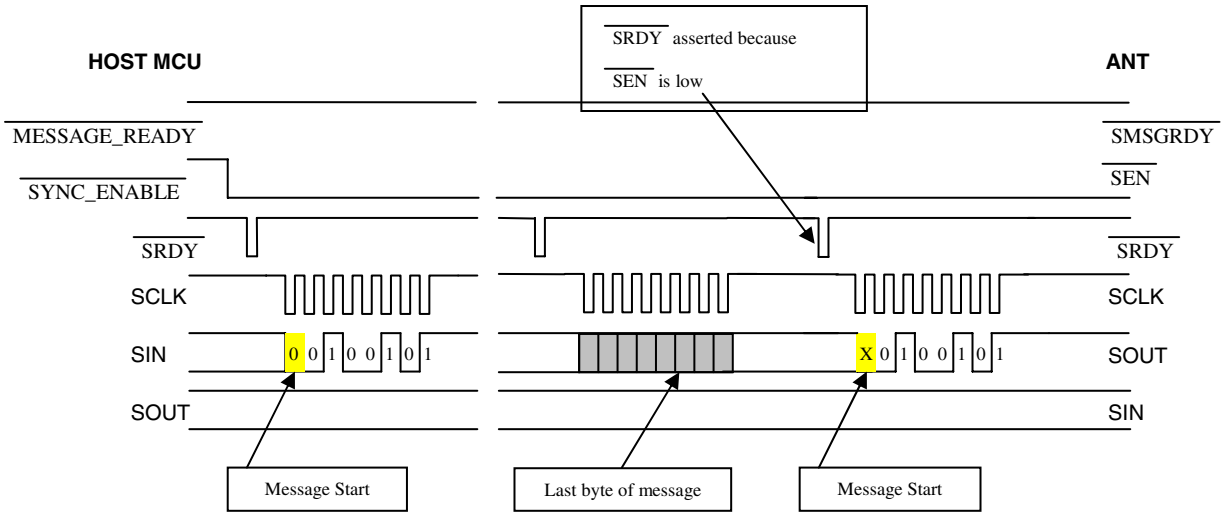


Figure 13: Consecutive messaging

11.12 Synchronous Messaging with Bit Flow Control

If no hardware serial port is available on the HOST MCU, it is still possible to control the ANT MCU, using bit flow control. Using this method, the serial lines are implemented with software controlled IO lines. All of the messaging signaling remains the same as above, but at the byte level the signaling becomes the following:

11.12.1 ANT → HOST Byte Transaction (Software Bit Flow Control)

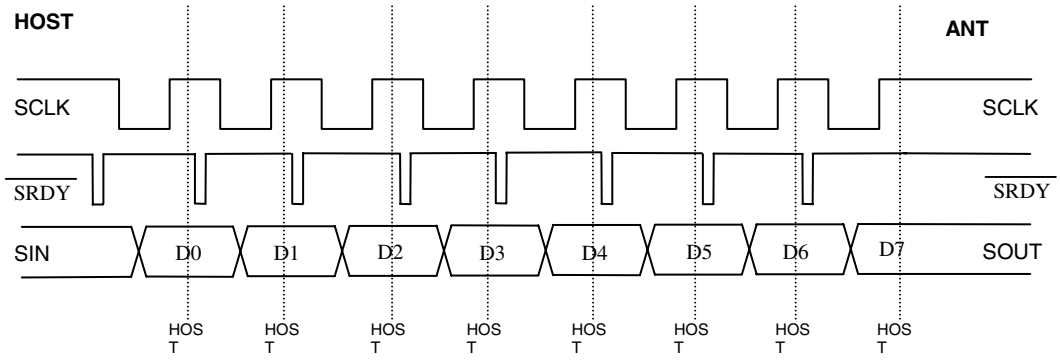


Figure 14: ANT → HOST Byte Transaction (Software Bit Flow Control)

11.12.2 HOST → ANT Byte Transaction (Software Bit Flow Control)

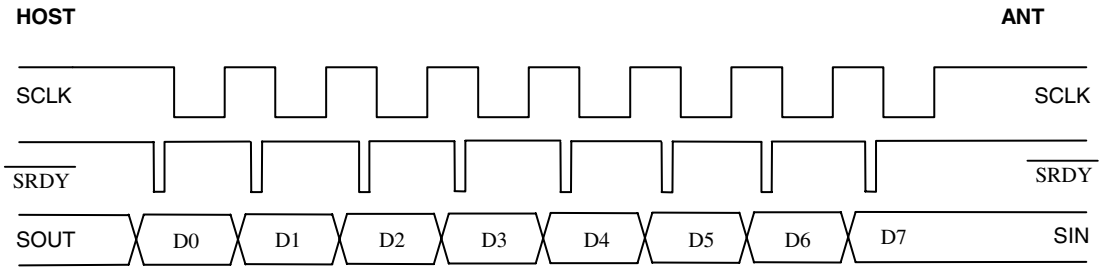


Figure 15: HOST → ANT Byte Transaction (Software Bit Flow Control)

It is important to note that the HOST MCU will do all bit processing on the rising edge of the SCLK signal, with the exception of the transmitting a byte from the HOST MCU to the ANT, where the first data bit will be asserted before the first clock edge. The final rising edge of the byte transaction will be the event to drive byte processing from.

11.13 Optional Serial Enable Control (ANT → HOST)

The HOST MCU may optionally monitor the $\overline{\text{SEN}}$ signal, which is driven by the ANT MCU. This signal will be asserted by the ANT MCU prior to message transmission. It can therefore be used as a serial port enable signal, which is useful in cases where the host serial port requires hardware activation.

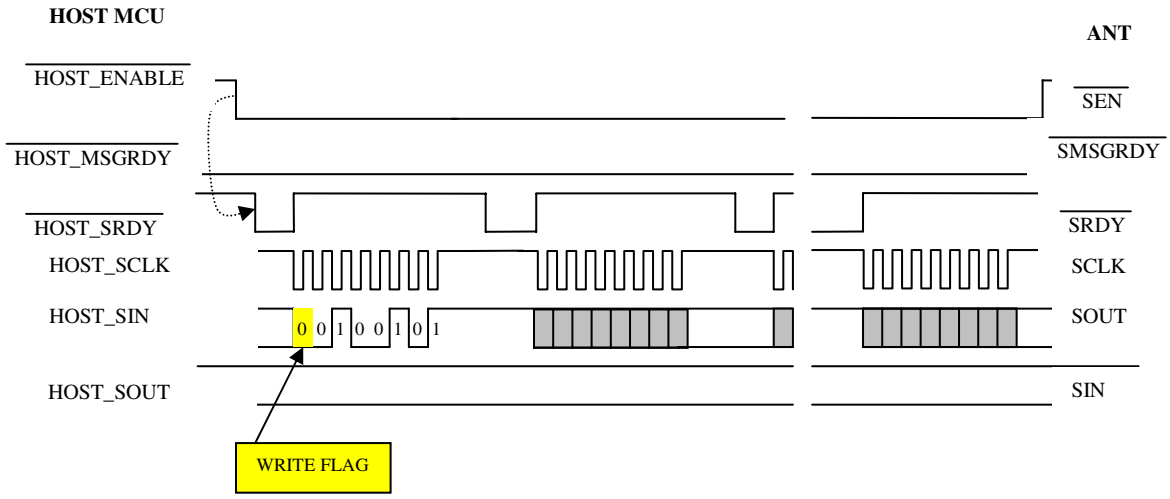


Figure 16: Optional Serial Enable Control (ANT → HOST)

11.14 Synchronization

The following sequence will cause the nRF24AP1 to reset. This is useful to guarantee that the host processor is in synchronization with the nRF24AP1 in startup conditions when using synchronous mode.

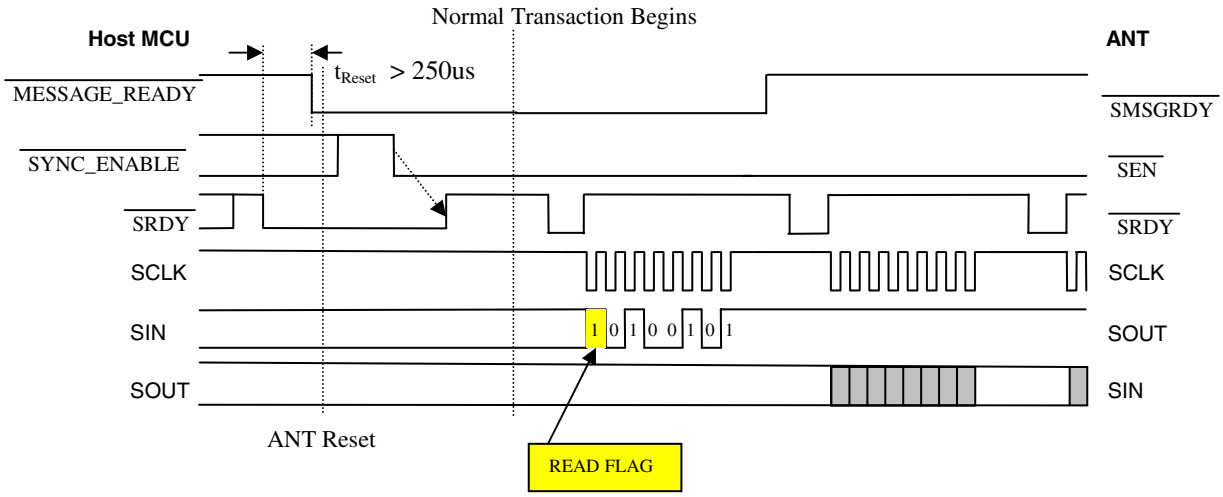


Figure 17: Synchronization

11.15 Using an Epson MCU as a host controller

The interface has been designed to easily interface with an EPSON microcontroller with a built in USART. The EPSON should be configured in the following manner:

1. HOST_SIN is connected to the SIN pin
2. HOST_SOUT is connected to the SOUT pin
3. HOST_SCLK is connected to the SCLK pin
4. $\overline{\text{HOST\_SRDY}}$ is connected to the $\overline{\text{SRDY}}$ pin
5. 32KHZ_OUT is connected to the FOUT pin
6. $\overline{\text{HOST\_ENABLE}}$ is connected to a GPIO configured as an input
7. $\overline{\text{HOST\_MSG\_READY}}$ is connected to a GPIO configured as an output
8. FOUT is configured to output 32kHz on this pin
9. Set the USART to Slave synchronous
10. Configure the $\overline{\text{SRDY}}$ pin to be controlled by the USART
11. The firmware can now communicate with the ANT MCU on a byte wise basis
12. The USART hardware will control the signaling on the $\overline{\text{HOST\_SRDY}}$, HOST_SCLK, HOST_SIN and HOST_SOUT lines
13. The firmware controls the signaling on $\overline{\text{HOST\_ENABLE}}$ and $\overline{\text{HOST\_MSG\_READY}}$

12. PERIPHERAL RF INFORMATION

12.1 Antenna output

The ANT1 & ANT2 output pins provide a balanced RF output to the antenna. The pins must have a DC path to VDD, either via a RF choke or via the center point in a dipole antenna. A load of 100Ω+j175Ω between the ANT1/ANT2 is recommended for maximum output power (0dBm). Lower load impedance (for instance 50 Ω) can be obtained by fitting a simple matching network.

12.2 Output Power adjustment

RF output power	Peak current consumption
0 dBm ±3dB	16.0 mA
-5 dBm ±3dB	13.5 mA
-10 dBm ±3dB	12.5 mA
-20 dBm ±3dB	12 mA

Conditions: VDD = 3.0V, VSS = 0V, T_A = 27ºC, Load impedance = 100Ω+j175Ω.

Table 15: RF output power setting for the nRF24AP1.

12.3 Crystal Specification

Tolerance includes initially accuracy and tolerance over temperature and aging.

Frequency	C_L	ESR	C_{0max}	Tolerance
16	12pF	100 Ω	7.0pF	±50ppm

Table 16: Crystal specification of the nRF24AP1

To achieve a crystal oscillator solution with low power consumption and fast start-up time, it is recommended to specify the crystal with a low value of crystal load capacitance. Specifying C_L=12pF is OK, but it is possible to use up to 16pF. Specifying a lower value of crystal parallel equivalent capacitance, C_0 will also work, but this can increase the price of the crystal itself. Typically C_0=1.5pF at a crystal specified for C_{0max}=7.0pF.

12.4 Sharing crystal with micro controller.

When using a micro controller to drive the crystal reference input XC1 of the nRF24AP1 transceiver some rules must be followed.

12.5 Crystal parameters:

When the micro controller drives the nRF24AP1 clock input, the requirement of load capacitance C_L is set by the micro controller only. The frequency accuracy of ±50 ppm is still required to get a functional radio link. The nRF24AP1 will load the crystal by 0.5pF at XC1 in addition to the PBC routing.

12.6 Input crystal amplitude & Current consumption

The input signal should not have amplitudes exceeding any rail voltage, but any DC-voltage within this is OK. Exceeding rail voltage will excite the ESD structure and the radio performance is degraded below specification. If testing the nRF24AP1 with a RF source with no DC offset as the reference source, the input signal will go below the ground level, which is not acceptable.

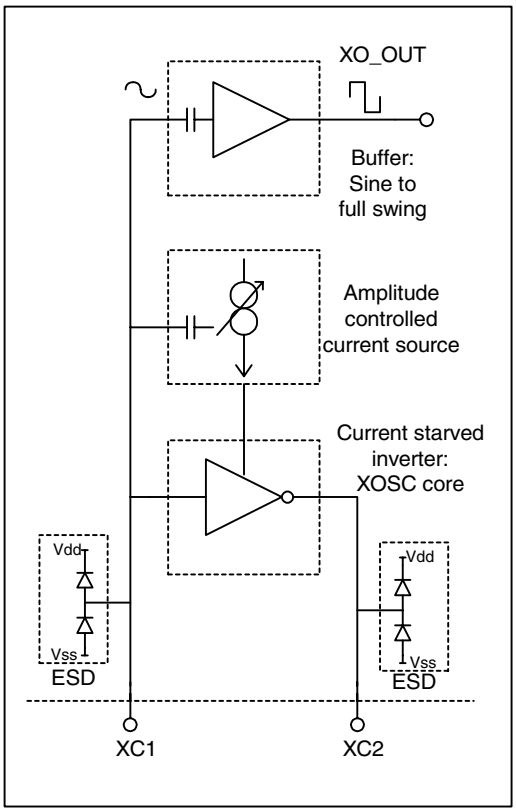


Figure 18: Principle of crystal oscillator

It is recommended to use a DC-block before the XC1 pin so that the internal ESD structures will self bias the XC1 voltage .

The nRF24AP1 crystal oscillator is amplitude regulated. To achieve low current consumption and also good signal-to-noise ratio, it is recommended to use an input signal larger than 0.4 V-peak. The needed input swing is independent of the crystal frequency. When clocking the nRF24AP1 externally, XC2 is not used and can be left as an open pin.

12.7 PCB layout and de-coupling guidelines

A well-designed PCB is necessary to achieve good RF performance. Keep in mind that a poor layout may lead to loss of performance, or even functionality, if due care is not taken. A fully qualified RF-layout for the nRF24AP1 and its surrounding components, including matching networks, can be downloaded from **www.nordicsemi.no**.

A PCB with a minimum of two layers including a ground plane is recommended for optimum performance. The nRF24AP1 DC supply voltage should be de-coupled as close as possible to the VDD pins with high performance RF capacitors, see Table 17. It is preferable to mount a large surface mount capacitor (e.g. 4.7µF tantalum) in parallel with the smaller value capacitors. The nRF24AP1 supply voltage should be filtered and routed separately from the supply voltages of any digital circuitry.

Long power supply lines on the PCB should be avoided. All device grounds, VDD connections and VDD bypass capacitors must be connected as close as possible to the nRF24AP1 IC. For a PCB with a topside RF ground plane, the VSS pins should be connected directly to the ground plane. For a PCB with a bottom ground plane, the best technique is to have via holes as close as possible to the VSS pads. One via hole should be used for each VSS pin.

Full swing digital data or control signals should not be routed close to the crystal or the power supply lines.

13. APPLICATION EXAMPLE

13.1 nRF24AP1 with single ended matching network

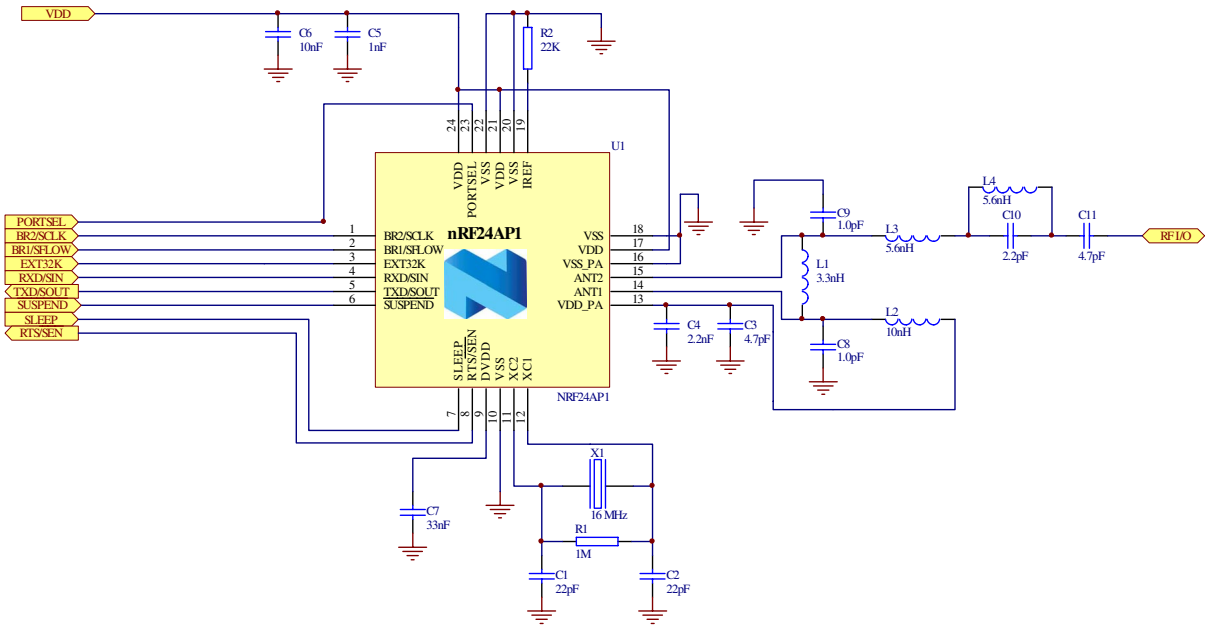


Figure 19: nRF24AP1 schematic for RF layouts with single end 50Ω antenna

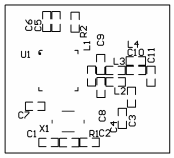
Component	Description	Size	Value	Tolerance	Units
C1	Capacitor ceramic, 50V, NPO	0603	22	±5%	pF
C2	Capacitor ceramic, 50V, NPO	0603	22	±5%	pF
C3	Capacitor ceramic, 50V, NPO	0603	4.7	±5%	pF
C4	Capacitor ceramic, 50V, X7R	0603	2.2	±10%	nF
C5	Capacitor ceramic, 50V, X7R	0603	1.0	±10%	nF
C6	Capacitor ceramic, 50V, X7R	0603	10	±10%	nF
C7	Capacitor ceramic, 50V, X7R	0603	33	±10%	nF
R1	Resistor	0603	1.0	±10%	MΩ
R2	Resistor	0603	22	±1%	kΩ
U1	nRF24AP1 transceiver	QFN24 / 5x5	nRF24AP1		
X1	Crystal, CL = 12pF, ESR < 100 ohm	LxWxH = 4.0x2.5x0.8	16	+/- 50 ppm	MHz
L1	Inductor	0603	3.3	± 5%	nH
L2	Inductor	0603	10	± 5%	nH
L3	Inductor	0603	5.6	± 5%	nH
L4	Inductor	0603	5.6	± 5%	nH
C8	Ceramic capacitor, 50V, NP0	0603	1.0	± 0.1 pF	pF
C9	Ceramic capacitor, 50V, NP0	0603	1.0	± 0.1 pF	pF
C10	Ceramic capacitor, 50V, NP0	0603	2.2	± 0.25 pF	pF
C11	Ceramic capacitor, 50V, NP0	0603	4.7	± 0.25 pF	pF

Table 17: Recommended components (BOM) in nRF24AP1 with antenna matching network

13.2 PCB layout example

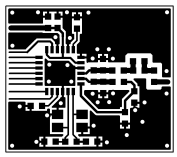
Figure 20 shows a PCB layout example for the application schematic in Figure 19.

A double-sided FR-4 board of 1.6mm thickness is used. This PCB has a ground plane on the bottom layer. Additionally, there are ground areas on the component side of the board to ensure sufficient grounding of critical components. A large number of via holes connect the top layer ground areas to the bottom layer ground plane.

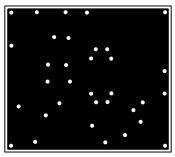


Top silk screen

No components in bottom layer



Top view



Bottom view

Figure 20: nRF24AP1 RF layout with single ended connection to 50Ω antenna and 0603 size passive components

14. DEFINITIONS

Data sheet status	
Objective product specification	This data sheet contains target specifications for product development.
Preliminary product specification	This data sheet contains preliminary data; supplementary data may be published from Nordic Semiconductor ASA later.
Product specification	This data sheet contains final product specifications. Nordic Semiconductor ASA reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Limiting values	
Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Specifications sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

Table 18: Definitions

Nordic Semiconductor ASA reserves the right to make changes without further notice to the product to improve reliability, function or design. Nordic Semiconductor ASA does not assume any liability arising out of the application or use of any product or circuits described herein.

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Nordic Semiconductor ASA customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Nordic Semiconductor ASA for any damages resulting from such improper use or sale.

Preliminary Product Specification: Revision Date: 29.04.2005.

Data sheet order code: 290405-nRF24AP1

YOUR NOTES

14.1 Nordic Semiconductor ASA – World Wide Distributors

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