

**IRFZ44Z**  
**IRFZ44ZS**  
**IRFZ44ZL**

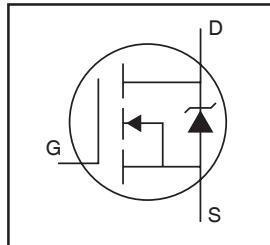
HEXFET® Power MOSFET

### Features

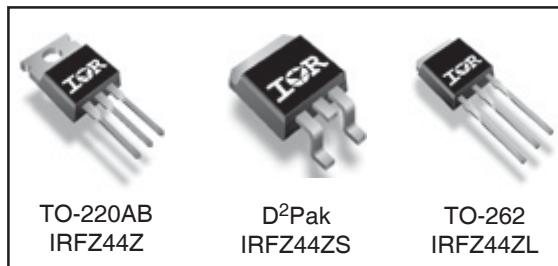
- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax

### Description

Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.



$V_{DSS} = 55V$   
 $R_{DS(on)} = 13.9m\Omega$   
 $I_D = 51A$



### Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_c = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Silicon Limited)	51	A
$I_D @ T_c = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (See Fig. 9)	36	
$I_{DM}$	Pulsed Drain Current ①	200	
$P_D @ T_c = 25^\circ C$	Maximum Power Dissipation	80	W
	Linear Derating Factor	0.53	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$E_{AS}$	Single Pulse Avalanche Energy (Thermally Limited) ②	86	mJ
$E_{AS}$ (tested)	Single Pulse Avalanche Energy Tested Value ⑦	105	
$I_{AR}$	Avalanche Current ①	See Fig.12a,12b,15,16	A
$E_{AR}$	Repetitive Avalanche Energy ⑥		mJ
$T_J$	Operating Junction and	-55 to + 175	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		
	Mounting torque, 6-32 or M3 screw	300 (1.6mm from case )	
		10 lbf·in (1.1N·m)	

### Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{0JC}$	Junction-to-Case	—	1.87	°C/W
$R_{0CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{0JA}$	Junction-to-Ambient	—	62	
$R_{0JA}$	Junction-to-Ambient (PCB Mount, steady state) ⑧	—	40	

HEXFET® is a registered trademark of International Rectifier.

**Static @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(\text{BR})\text{DSS}}$	Drain-to-Source Breakdown Voltage	55	—	—	V	$V_{\text{GS}} = 0\text{V}$ , $I_D = 250\mu\text{A}$
$\Delta V_{\text{DSS}/\Delta T_J}$	Breakdown Voltage Temp. Coefficient	—	0.054	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}$ , $I_D = 1\text{mA}$
$R_{\text{DS}(\text{on})}$	Static Drain-to-Source On-Resistance	—	11.1	13.9	$\text{m}\Omega$	$V_{\text{GS}} = 10\text{V}$ , $I_D = 31\text{A}$ ④
$V_{\text{GS}(\text{th})}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{\text{DS}} = V_{\text{GS}}$ , $I_D = 250\mu\text{A}$
$g_{\text{fs}}$	Forward Transconductance	22	—	—	S	$V_{\text{DS}} = 25\text{V}$ , $I_D = 31\text{A}$
$I_{\text{DSS}}$	Drain-to-Source Leakage Current	—	—	20	$\mu\text{A}$	$V_{\text{DS}} = 55\text{V}$ , $V_{\text{GS}} = 0\text{V}$
		—	—	250		$V_{\text{DS}} = 55\text{V}$ , $V_{\text{GS}} = 0\text{V}$ , $T_J = 125^\circ\text{C}$
$I_{\text{GSS}}$	Gate-to-Source Forward Leakage	—	—	200	nA	$V_{\text{GS}} = 20\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-200		$V_{\text{GS}} = -20\text{V}$
$Q_g$	Total Gate Charge	—	29	43	nC	$I_D = 31\text{A}$
$Q_{\text{gs}}$	Gate-to-Source Charge	—	7.2	11		$V_{\text{DS}} = 44\text{V}$
$Q_{\text{gd}}$	Gate-to-Drain ("Miller") Charge	—	12	18	ns	$V_{\text{GS}} = 10\text{V}$ ④
$t_{\text{d}(\text{on})}$	Turn-On Delay Time	—	14	—		$V_{\text{DD}} = 28\text{V}$
$t_r$	Rise Time	—	68	—	ns	$I_D = 31\text{A}$
$t_{\text{d}(\text{off})}$	Turn-Off Delay Time	—	33	—		$R_G = 15\Omega$
$t_f$	Fall Time	—	41	—	ns	$V_{\text{GS}} = 10\text{V}$ ④
$L_D$	Internal Drain Inductance	—	4.5	—		Between lead, 6mm (0.25in.) from package and center of die contact
$L_S$	Internal Source Inductance	—	7.5	—	pF	
$C_{\text{iss}}$	Input Capacitance	—	1420	—		$V_{\text{GS}} = 0\text{V}$
$C_{\text{oss}}$	Output Capacitance	—	240	—		$V_{\text{DS}} = 25\text{V}$
$C_{\text{rss}}$	Reverse Transfer Capacitance	—	130	—		$f = 1.0\text{MHz}$ , See Fig. 5
$C_{\text{oss}}$	Output Capacitance	—	830	—		$V_{\text{GS}} = 0\text{V}$ , $V_{\text{DS}} = 1.0\text{V}$ , $f = 1.0\text{MHz}$
$C_{\text{oss}}$	Output Capacitance	—	190	—		$V_{\text{GS}} = 0\text{V}$ , $V_{\text{DS}} = 44\text{V}$ , $f = 1.0\text{MHz}$
$C_{\text{oss eff.}}$	Effective Output Capacitance	—	300	—		$V_{\text{GS}} = 0\text{V}$ , $V_{\text{DS}} = 0\text{V}$ to $44\text{V}$

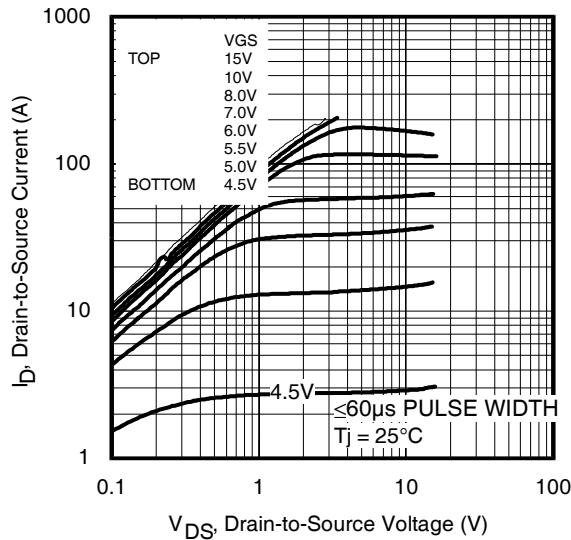
**Diode Characteristics**

	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_s$	Continuous Source Current (Body Diode)	—	—	51	A	MOSFET symbol showing the integral reverse p-n junction diode.
$I_{\text{SM}}$	Pulsed Source Current (Body Diode) ①	—	—	200		
$V_{\text{SD}}$	Diode Forward Voltage	—	—	1.2	V	$T_J = 25^\circ\text{C}$ , $I_S = 31\text{A}$ , $V_{\text{GS}} = 0\text{V}$ ④
$t_{\text{rr}}$	Reverse Recovery Time	—	23	35		$T_J = 25^\circ\text{C}$ , $I_F = 31\text{A}$ , $V_{\text{DD}} = 28\text{V}$
$Q_{\text{rr}}$	Reverse Recovery Charge	—	17	26	nC	$dI/dt = 100\text{A}/\mu\text{s}$ ④
$t_{\text{on}}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

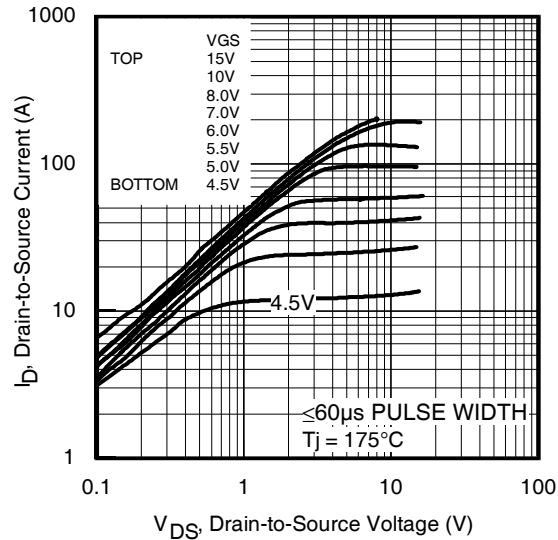
**Notes:**

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).
- ② Limited by  $T_{J\text{max}}$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.18\text{mH}$ ,  $R_G = 25\Omega$ ,  $I_{AS} = 31\text{A}$ ,  $V_{GS} = 10\text{V}$ . Part not recommended for use above this value.
- ③  $I_{SD} \leq 31\text{A}$ ,  $di/dt \leq 840\text{A}/\mu\text{s}$ ,  $V_{\text{DD}} \leq V_{(\text{BR})\text{DSS}}$ ,  $T_J \leq 175^\circ\text{C}$ .
- ④ Pulse width  $\leq 1.0\text{ms}$ ; duty cycle  $\leq 2\%$ .

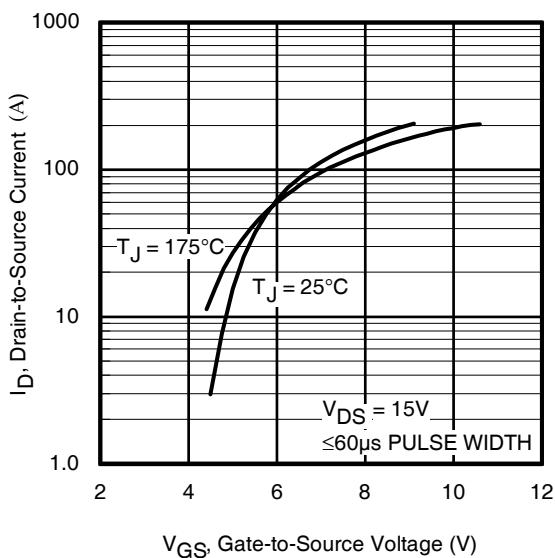
- ⑤  $C_{\text{oss eff.}}$  is a fixed capacitance that gives the same charging time as  $C_{\text{oss}}$  while  $V_{\text{DS}}$  is rising from 0 to 80%  $V_{\text{DSS}}$ .
- ⑥ Limited by  $T_{J\text{max}}$ , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.
- ⑦ This value determined from sample failure population. 100% tested to this value in production.
- ⑧ This is applied to D<sup>2</sup>Pak, when mounted on 1" square PCB ( FR-4 or G-10 Material ). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑨  $R_\theta$  is rated at  $T_J$  of approximately  $90^\circ\text{C}$ .



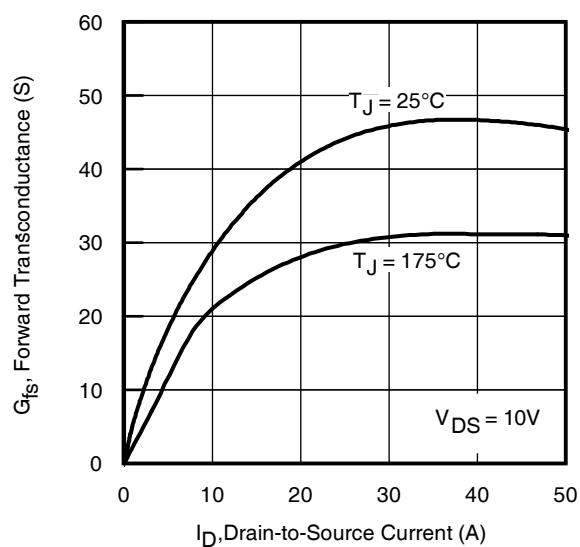
**Fig 1.** Typical Output Characteristics



**Fig 2.** Typical Output Characteristics



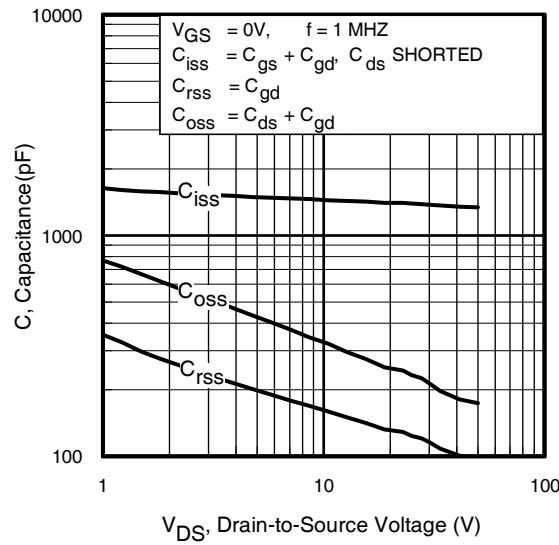
**Fig 3.** Typical Transfer Characteristics



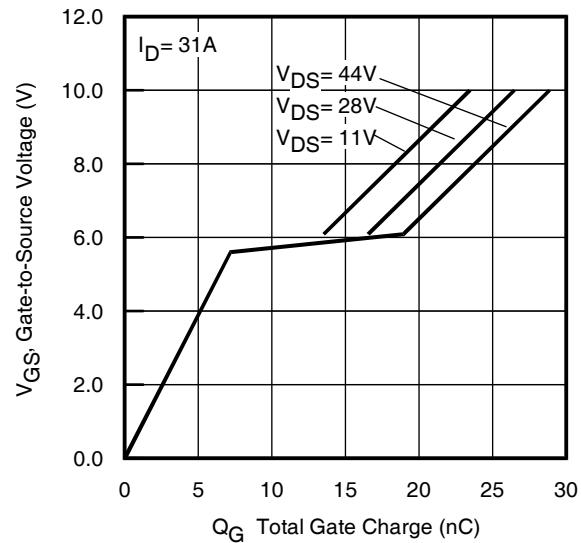
**Fig 4.** Typical Forward Transconductance  
vs. Drain Current

# IRFZ44Z/S/L

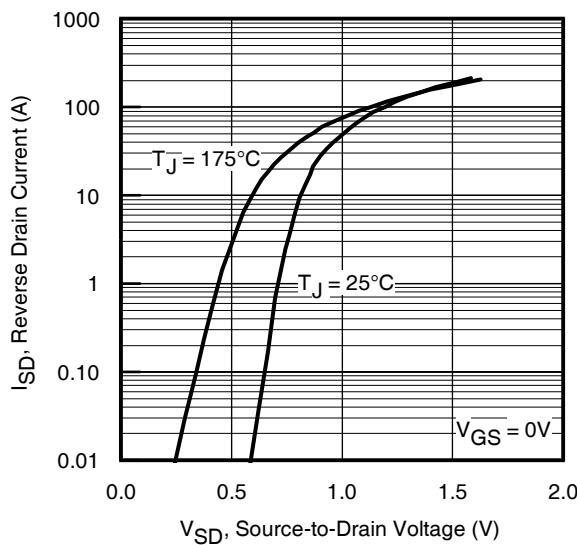
International  
Rectifier



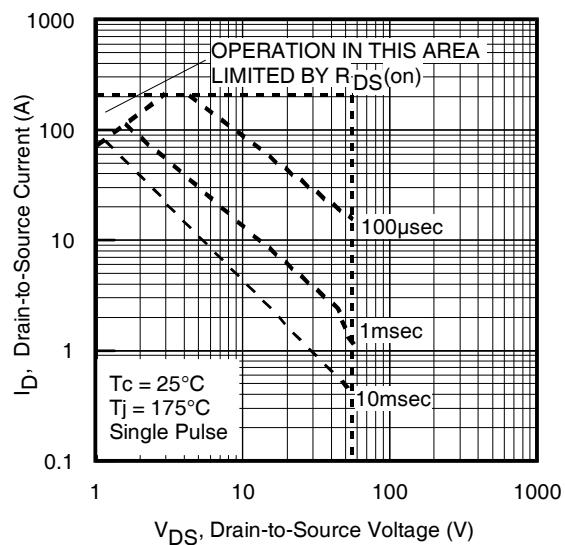
**Fig 5.** Typical Capacitance vs.  
Drain-to-Source Voltage



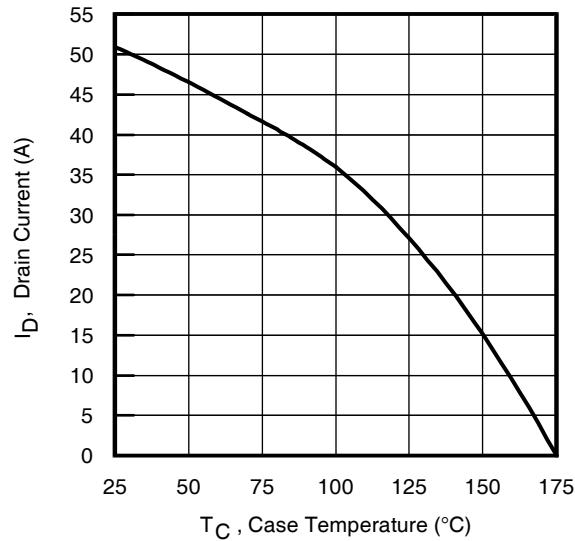
**Fig 6.** Typical Gate Charge vs.  
Gate-to-Source Voltage



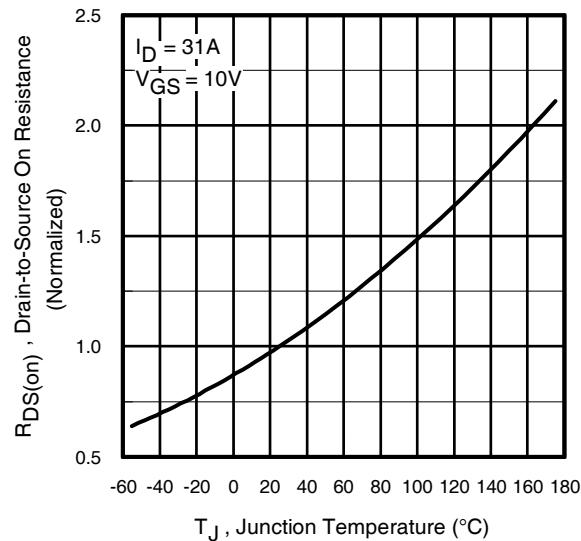
**Fig 7.** Typical Source-Drain Diode  
Forward Voltage



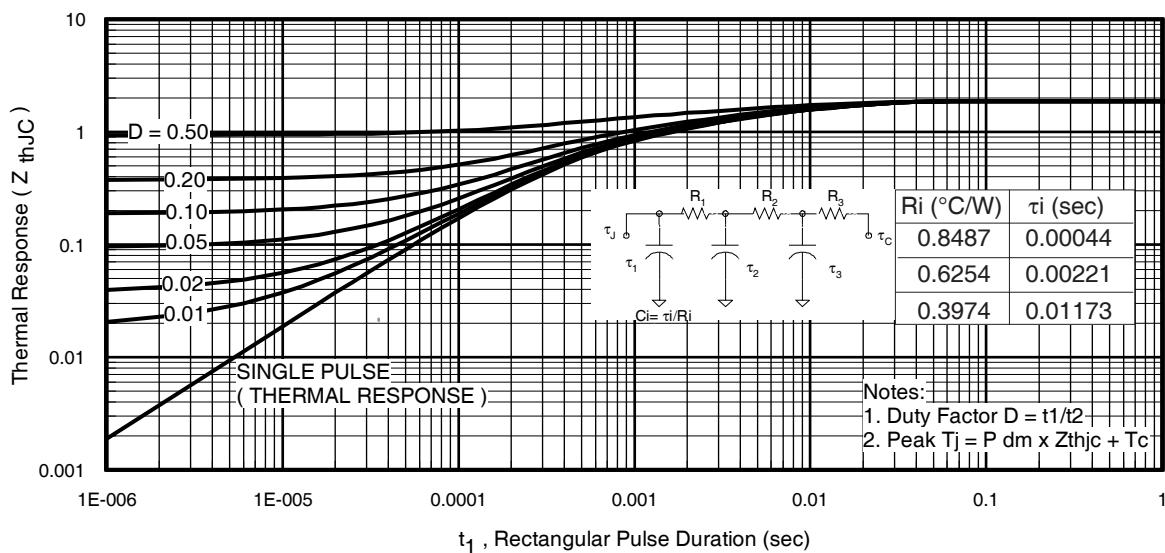
**Fig 8.** Maximum Safe Operating Area



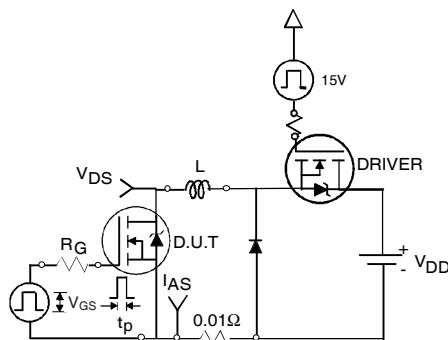
**Fig 9.** Maximum Drain Current vs.  
Case Temperature



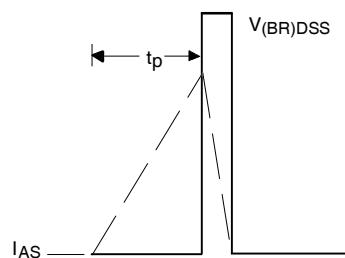
**Fig 10.** Normalized On-Resistance  
vs. Temperature



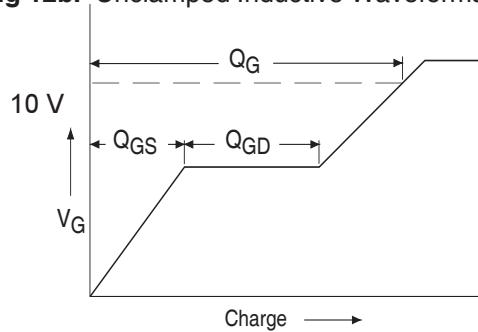
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case



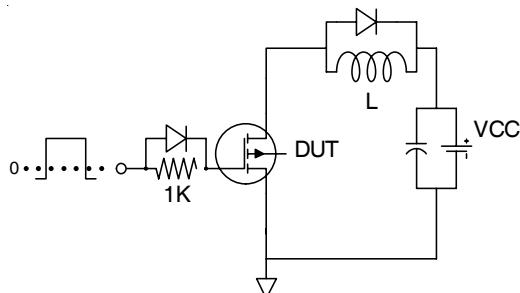
**Fig 12a.** Unclamped Inductive Test Circuit



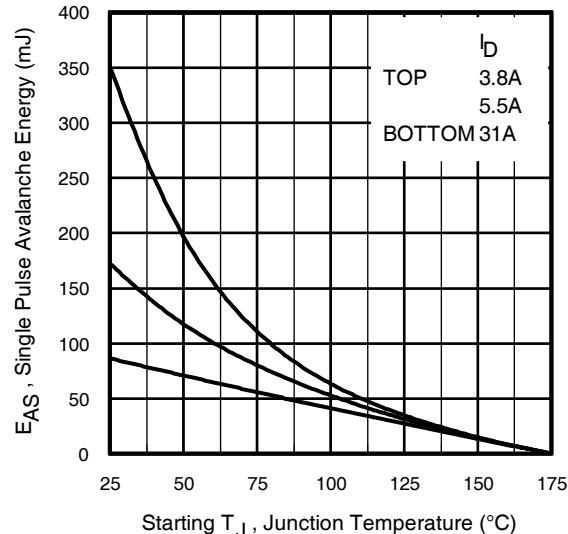
**Fig 12b.** Unclamped Inductive Waveforms



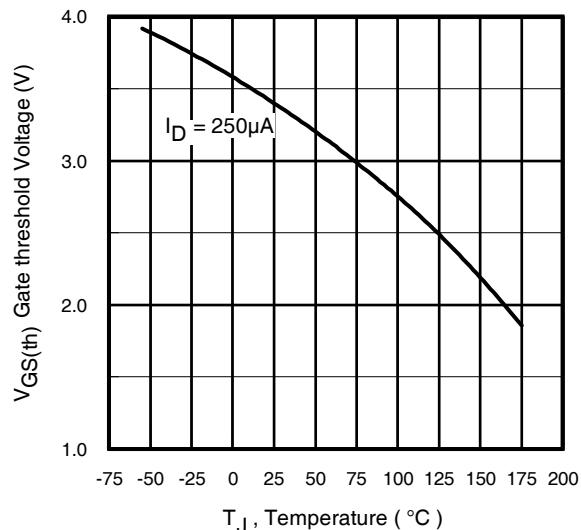
**Fig 13a.** Basic Gate Charge Waveform



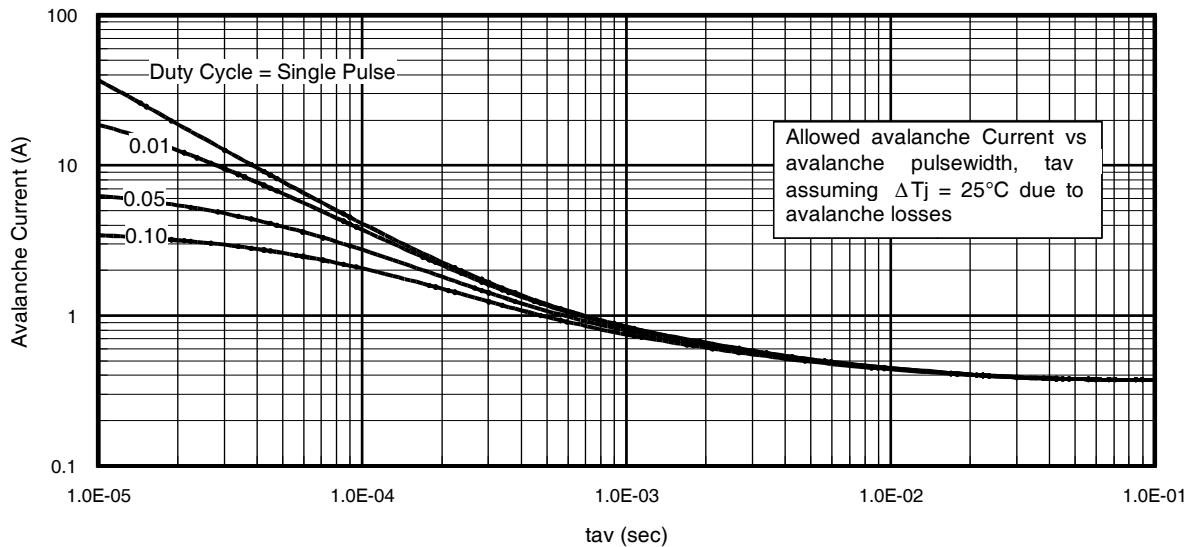
**Fig 13b.** Gate Charge Test Circuit



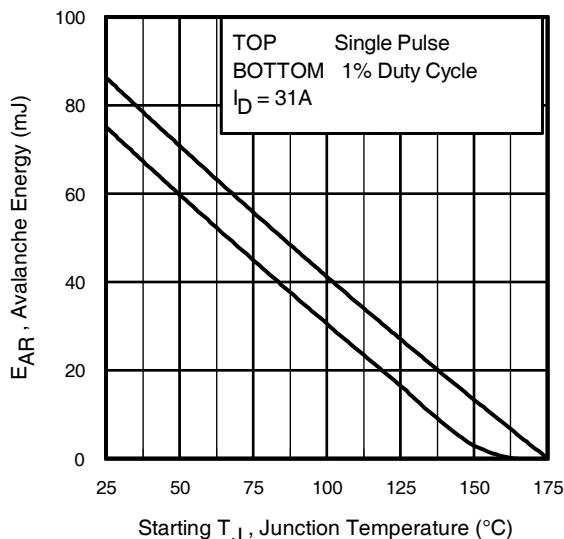
**Fig 12c.** Maximum Avalanche Energy vs. Drain Current



**Fig 14.** Threshold Voltage vs. Temperature



**Fig 15.** Typical Avalanche Current vs.Pulsewidth



**Fig 16.** Maximum Avalanche Energy vs. Temperature

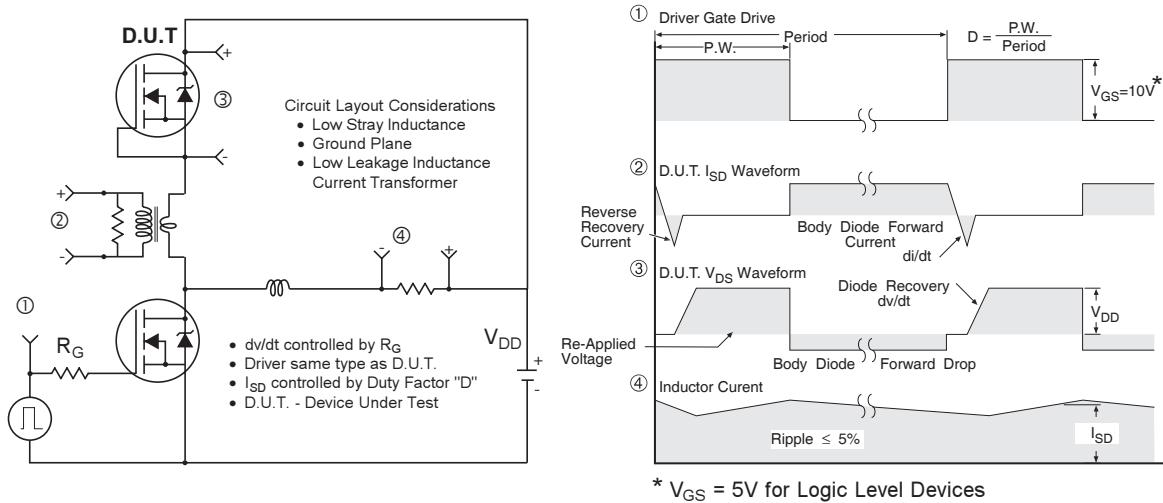
**Notes on Repetitive Avalanche Curves , Figures 15, 16:  
 (For further info, see AN-1005 at [www.irf.com](http://www.irf.com))**

1. Avalanche failures assumption:  
 Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 15, 16).
- $t_{av}$  = Average time in avalanche.
- $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$
- $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see figure 11)

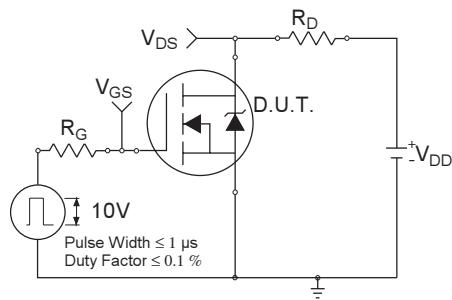
$$P_{D(ave)} = 1/2 ( 1.3 \cdot BV \cdot I_{av} ) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

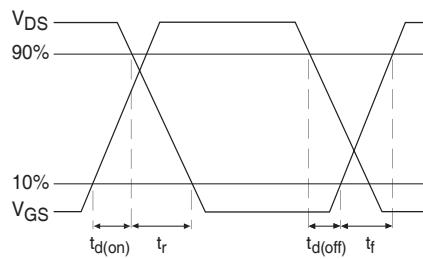
$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$



**Fig 17.** Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET® Power MOSFETs



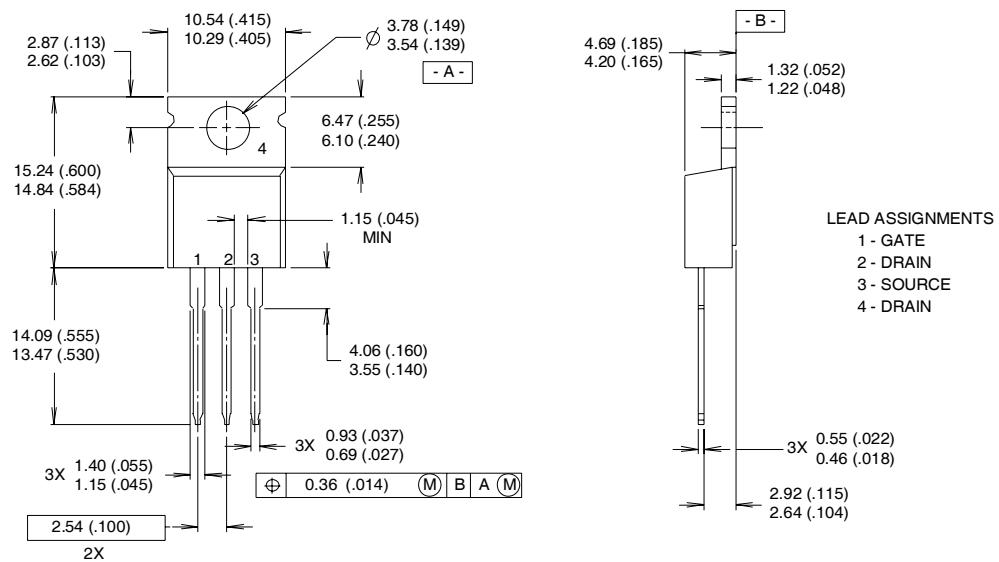
**Fig 18a.** Switching Time Test Circuit



**Fig 18b.** Switching Time Waveforms

## TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



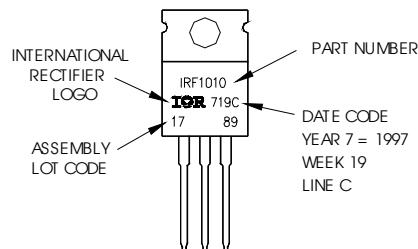
NOTES:

- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 2 CONTROLLING DIMENSION : INCH

- 3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
- 4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

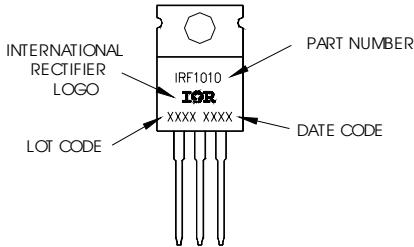
## TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010  
 LOT CODE 1789  
 ASSEMBLED ON WW 19, 1997  
 IN THE ASSEMBLY LINE "C"



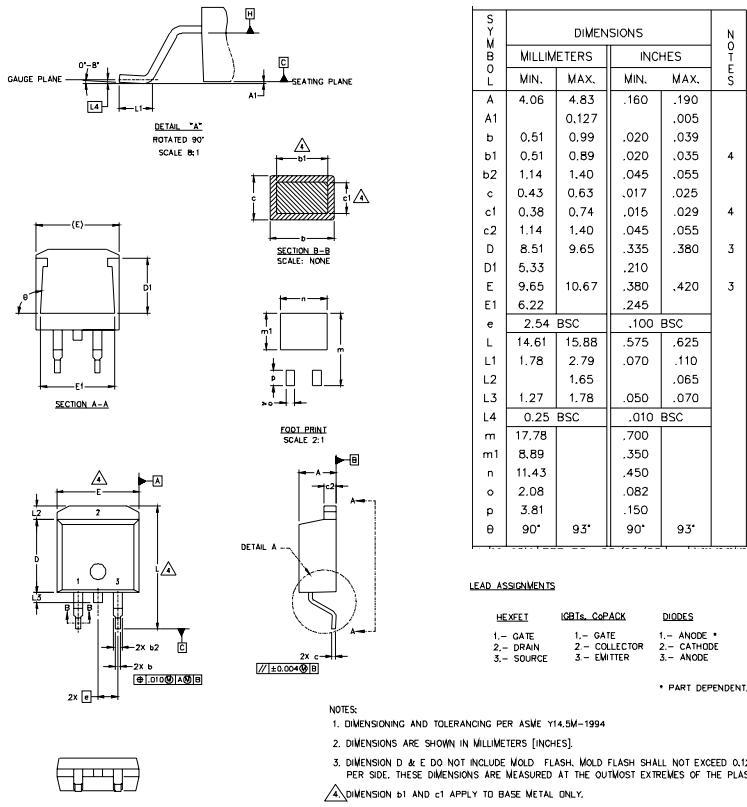
### For GB Production

EXAMPLE: THIS IS AN IRF1010  
 LOT CODE 1789  
 ASSEMBLED ON WW 19, 1997  
 IN THE ASSEMBLY LINE "C"



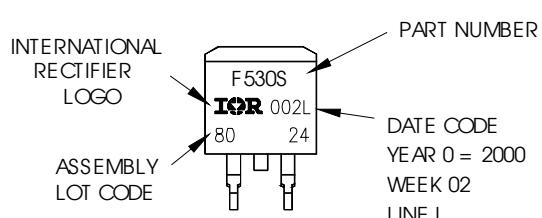
## D<sup>2</sup>Pak Package Outline

Dimensions are shown in millimeters (inches)

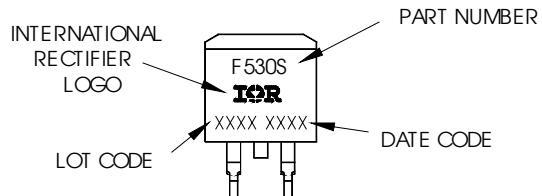


## D<sup>2</sup>Pak Part Marking Information

EXAMPLE: THIS IS AN IRF530S WITH  
LOT CODE 8024  
ASSEMBLED ON WW 02, 2000  
IN THE ASSEMBLY LINE "L"

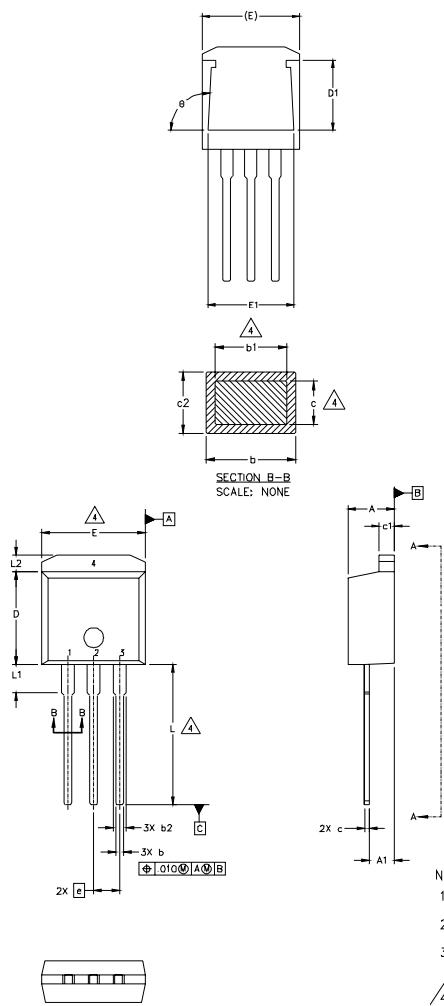


For GB Production  
EXAMPLE: THIS IS AN IRF530S WITH  
LOT CODE 8024  
ASSEMBLED ON WW 02, 2000  
IN THE ASSEMBLY LINE "L"



## TO-262 Package Outline

Dimensions are shown in millimeters (inches)



SYM BO L	DIMENSIONS				NOTES	
	MILLIMETERS		INCHES			
	MIN.	MAX.	MIN.	MAX.		
A	4.06	4.83	.160	.190		
A1	2.03	2.92	.080	.115		
b	0.51	0.99	.020	.039		
b1	0.51	0.89	.020	.035	4	
b2	1.14	1.40	.045	.055		
c	0.38	0.63	.015	.025	4	
c1	1.14	1.40	.045	.055		
c2	0.43	.063	.017	.029		
D	8.51	9.65	.335	.380	3	
D1	5.33		.210			
E	9.65	10.67	.380	.420	3	
E1	6.22		.245			
e	2.54	BSC	.100	BSC		
L	13.46	14.09	.530	.555		
L1	3.56	3.71	.140	.146		
L2		1.65		.065		

### LEAD ASSIGNMENTS

#### HEXFET

- 1. GATE
- 2. DRAIN
- 3. SOURCE
- 4. DRAIN

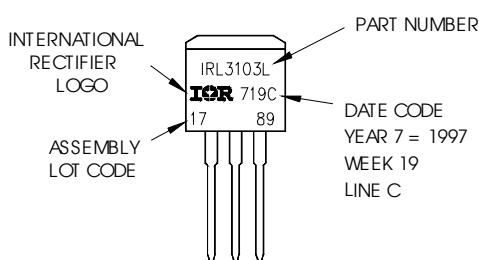
#### IGBT

- 1- GATE
- 2- COLLECTOR
- 3- Emitter

- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
  2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
  3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
  4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
  5. CONTROLLING DIMENSION: INCH.

## TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L  
LOT CODE 1789  
ASSEMBLED ON WW 19, 1997  
IN THE ASSEMBLY LINE "C"

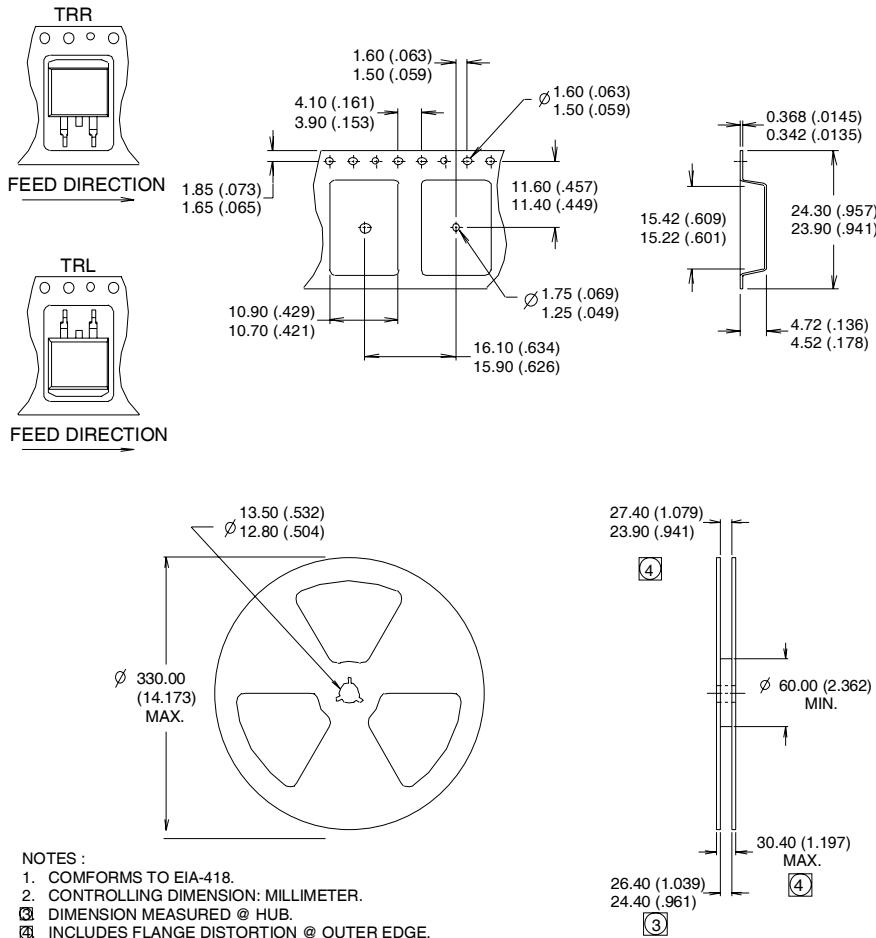


# IRFZ44Z/S/L

International  
**IR** Rectifier

## D<sup>2</sup>Pak Tape & Reel Information

Dimensions are shown in millimeters (inches)



TO-220AB package is not recommended for Surface Mount Application.

Data and specifications subject to change without notice.  
This product has been designed and qualified for the Automotive [Q101] market.  
Qualification Standards can be found on IR's Web site.

International  
**IR** Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105  
TAC Fax: (310) 252-7903

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