Noninverting Buffer / CMOS Logic Level Shifter

with LSTTL-Compatible Inputs

The MC74VHC1GT125 is a single gate noninverting buffer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The MC74VHC1GT125 requires the 3–state control input (\overline{OE}) to be set High to place the output into the high impedance state.

The device input is compatible with TTL-type input thresholds and the output has a full 5 V CMOS level output swing. The input protection circuitry on this device allows overvoltage tolerance on the input, allowing the device to be used as a logic-level translator from 3.0 V CMOS logic to 5.0 V CMOS Logic or from 1.8 V CMOS logic to 3.0 V CMOS Logic while operating at the high-voltage power supply.

The MC74VHC1GT125 input structure provides protection when voltages up to 7 V are applied, regardless of the supply voltage. This allows the MC74VHC1GT125 to be used to interface 5 V circuits to 3 V circuits. The output structures also provide protection when $V_{CC}=0\ V$. These input and output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

- High Speed: $t_{PD} = 3.5 \text{ ns (Typ)}$ at $V_{CC} = 5 \text{ V}$
- Low Power Dissipation: $I_{CC} = 1 \mu A \text{ (Max)}$ at $T_A = 25 \text{°C}$
- TTL-Compatible Inputs: $V_{IL} = 0.8 \text{ V}$; $V_{IH} = 2.0 \text{ V}$
- CMOS-Compatible Outputs: $V_{OH} > 0.8 V_{CC}$; $V_{OL} < 0.1 V_{CC}$ @Load
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Pin and Function Compatible with Other Standard Logic Families
- Chip Complexity: FETs = 62; Equivalent Gates = 16

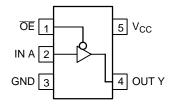


Figure 1. Pinout (Top View)



Figure 2. Logic Symbol



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MARKING DIAGRAMS

SC-88A / SOT-353/SC-70 DF SUFFIX CASE 419A



Pin 1 d = Date Code

TSOP-5/SOT-23/SC-59 DT SUFFIX CASE 483



Pin 1

d = Date Code

PIN ASSIGNMENT						
1 ŌE						
2	IN A					
3	GND					
4	OUT Y					
5	V _{CC}					

FUNCTION TABLE

A Input	OE Input	Y Output
L	L	L
Н	L	Н
X	н	Z

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

MAXIMUM RATINGS (Note 1)

Symbol	Charac	teristics	Value	Unit
V _{CC}	DC Supply Voltage		-0.5 to +7.0	V
V _{IN}	DC Input Voltage		-0.5 to +7.0	V
V _{OUT}	DC Output Voltage	$V_{CC} = 0$ High or Low State	-0.5 to 7.0 -0.5 to V _{CC} + 0.5	V
I _{IK}	Input Diode Current		-20	mA
I _{OK}	Output Diode Current	V _{OUT} < GND; V _{OUT} > V _{CC}	+20	mA
I _{OUT}	DC Output Current, per Pin		+25	mA
Icc	DC Supply Current, V _{CC} and GND		+50	mA
P _D	Power Dissipation in Still Air	SC-88A, TSOP-5	200	mW
θ_{JA}	Thermal Resistance	SC-88A, TSOP-5	333	°C/W
TL	Lead Temperature, 1 mm from Case for 10 s		260	°C
TJ	Junction Temperature Under Bias		+150	°C
T _{stg}	Storage Temperature		-65 to +150	°C
V _{ESD}	ESD Withstand Voltage	Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	> 2000 > 200 N/A	V
I _{Latch-Up}	Latch–Up Performance	Above V _{CC} and Below GND at 125°C (Note 5)	±500	mA

Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those
indicated may adversely affect device reliability. Functional operation under absolute—maximum—rated conditions is not implied. Functional
operation should be restricted to the Recommended Operating Conditions.

- 2. Tested to EIA/JESD22-A114-A
- 3. Tested to EIA/JESD22-A115-A
- 4. Tested to JESD22-C101-A
- 5. Tested to EIA/JESD78

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristic	s	Min	Max	Unit
V _{CC}	DC Supply Voltage		3.0	5.5	V
V _{IN}	DC Input Voltage	0.0	5.5	V	
V _{OUT}	DC Output Voltage	0.0	V _{CC}	V	
T _A	Operating Temperature Range		-55	+125	°C
t _r , t _f	Input Rise and Fall Time	$V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$	0	20	ns/V

Device Junction Temperature versus Time to 0.1% Bond Failures

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

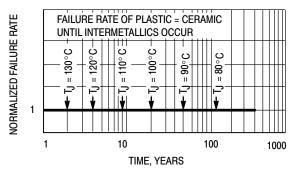


Figure 3. Failure Rate vs. Time Junction Temperature

DC ELECTRICAL CHARACTERISTICS

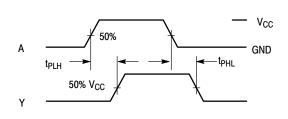
		V _{CC} T _A = 25°C		Č	T _A ≤	85°C	-55 ≤ T _A ≤ 125°C				
Symbol	Parameter	Test Conditions	(V)	Min	Тур	Max	Min	Max	Min	Max	Unit
V _{IH}	Minimum High-Level Input Voltage		3.0 4.5 5.5	1.4 2.0 2.0			1.4 2.0 2.0		1.4 2.0 2.0		V
V _{IL}	Maximum Low–Level Input Voltage		3.0 4.5 5.5			0.53 0.8 0.8		0.53 0.8 0.8		0.53 0.8 0.8	V
V _{OH}	Minimum High–Level Output Voltage	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OH} = -50 \mu A$	3.0 4.5	2.9 4.4	3.0 4.5		2.9 4.4		2.9 4.4		V
$V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -4$ mA $I_{OH} = -8$ mA	3.0 4.5	2.58 3.94			2.48 3.80		2.34 3.66			
V _{OL} Maximum Low-Level Output Voltage V _{IN} = V _{IH} or V _{IL}	Output Voltage	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OL} = 50 \mu\text{A}$	3.0 4.5		0.0 0.0	0.1 0.1		0.1 0.1		0.1 0.1	V
	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52		
I _{IN}	Maximum Input Leakage Current	V _{IN} = 5.5 V or GND	0 to 5.5			± 0.10		± 1.0		± 1.0	μΑ
I _{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	5.5			1.0		20		40	μΑ
I _{CCT}	Quiescent Supply Current	Input: $V_{IN} = 3.4 \text{ V}$ Other Input: V_{CC} or GND	5.5			1.35		1.50		1.65	mA
I _{OPD}	Output Leakage Current	V _{OUT} = 5.5 V	0.0			0.5		5.0		10	μΑ
I _{OZ}	Maximum 3–State Leakage Current	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $V_{OUT} = V_{CC} \text{ or GND}$	5.5			± 0.25		± 2.5		± 2.5	μΑ
I _{OPD}	Output Leakage Current	V _{OUT} = 5.5 V	0.0			0.5		5.0		10	μΑ

AC ELECTRICAL CHARACTERISTICS Input $t_{\rm f} = t_{\rm f} = 3.0~{\rm ns}$

			T _A = 25°C		T _A ≤	85°C	-55 ≤ T _A	≤ 125°C		
Symbol	Parameter	Test Conditions	Min	Тур	Max	Min	Max	Min	Max	Unit
t _{PLH} , t _{PHL}	Maximum Propagation Delay, A to Y	$V_{CC} = 3.3 \pm 0.3 \text{ V}$ $C_L = 15 \text{pF}$ $C_L = 50 \text{pF}$		5.6 8.1	8.0 11.5	1.0 1.0	9.5 13.0		12.0 16.0	ns
	(Figures 3. and 5.)	$V_{CC} = 5.0 \pm 0.5 \text{ V}$ $C_L = 15 \text{pF}$ $C_L = 50 \text{pF}$		3.8 5.3	5.5 7.5	1.0 1.0	6.5 8.5		8.5 10.5	5
t _{PZL} , t _{PZH}	· ==	$V_{CC} = 3.3 \pm 0.3 \text{ V}$ $C_L = 15 \text{pF}$ $R_L = R_I = 500 \Omega$ $C_L = 50 \text{pF}$		5.4 7.9	8.0 11.5	1.0 1.0	9.5 13.0		11.5 15.0	ns
	(Figures 4. and 5.)	$ \begin{array}{cccccccccccccccccccccccccccccccccccc$		3.6 5.1	5.1 7.1	1.0 1.0	6.0 8.0		7.5 9.5	5
t _{PLZ} , t _{PHZ}	Maximum Output Disable Time, OE to Y	$\begin{array}{c} V_{CC} = 3.3 \pm 0.3 \; V & C_L = 15 pF \\ R_L = R_I = 500 \; \Omega & C_L = 50 pF \end{array}$		6.5 8.0	9.7 13.2	1.0 1.0	11.5 15.0		14.5 18.0	ns
	(Figures 4. and 5.)	$ \begin{array}{cccccccccccccccccccccccccccccccccccc$		4.8 7.0	6.8 8.8	1.0 1.0	8.0 10.0		10.0 12.0	
C _{in}	Maximum Input Capacitance			4	10		10		10	pF
C _{out}	Maximum Three–State Output Capacitance (Output in High Impedance State)			6						pF
						Typical	@ 25°C	, V _{CC} = 5.0) V	
C _{PD}	Power Dissipation Capacitan	ce (Note 6)					14			pF

^{6.} C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}/4 (per buffer). C_{PD} is used to determine the no–load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

SWITCHING WAVEFORMS



V_{CC}

GND

T_{PZL} t_{PLZ}

HIGH
IMPEDANCE

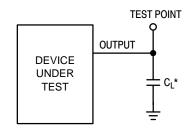
V_{OL} + 0.3V

V_{OH} - 0.3V

HIGH
IMPEDANCE

Figure 4. Switching Waveforms

Figure 5.



*Includes all probe and jig capacitance

DEVICE UNDER TEST TEST C_L^* CONNECT TO V_{CC} WHEN TESTING t_{PLZ} AND t_{PZL} CONNECT TO GND WHEN TESTING t_{PHZ} AND t_{PZH} .

*Includes all probe and jig capacitance

Figure 6. Test Circuit

Figure 7. Test Circuit

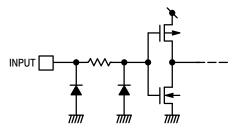


Figure 8. Input Equivalent Circuit

DEVICE ORDERING INFORMATION

	Device Nomenclature							
Device Order Number	Circuit Indicator	Temp Range Identifier	Technology	Device Function	Package Suffix	Tape & Reel Suffix	Package Type (Name/SOT#/ Common Name)	Tape and Reel Size [†]
MC74VHC1GT125DF1	MC	74	VHC1G	T125	DF	1	SC-88A / SOT-353 / SC-70	178 mm (7") 3000 Unit
MC74VHC1GT125DF2	МС	74	VHC1G	T125	DF	2	SC-88A / SOT-353 / SC-70	178 mm (7") 3000 Unit
MC74VHC1GT125DT1	MC	74	VHC1G	T125	DT	1	TSOPS / SOT-23 / SC-59	178 mm (7") 3000 Unit

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

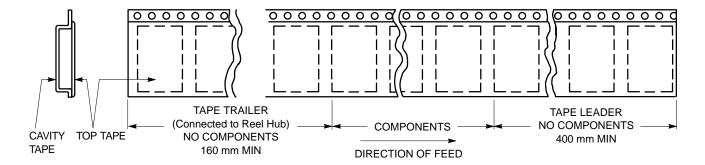


Figure 9. Tape Ends for Finished Goods

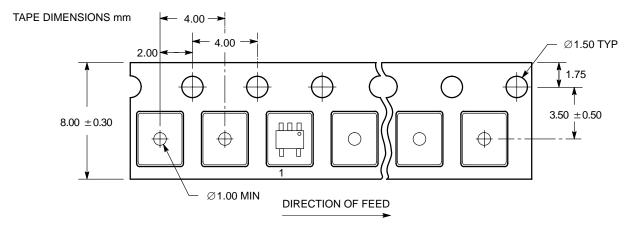


Figure 10. SC-70-5/SC-88A/SOT-353 DF1 Reel Configuration/Orientation

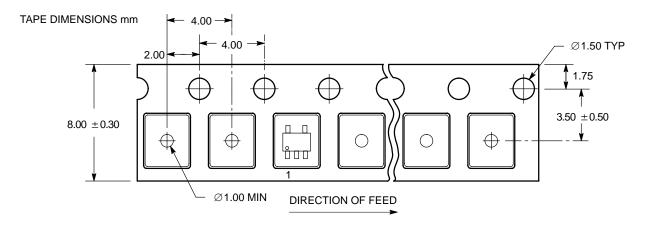


Figure 11. SC-70/SC-88A/SOT-353 DF2 and SOT23-5/TSOP-5/SC59-5 DT1 Reel Configuration/Orientation

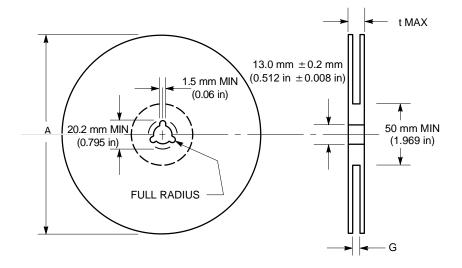


Figure 12. Reel Dimensions

REEL DIMENSIONS

Tape Size	T and R Suffix	A Max	G	t Max
8 mm	1, 2	178 mm (7 in)	8.4 mm, + 1.5 mm, -0.0 (0.33 in + 0.059 in, -0.00)	14.4 mm (0.56 in)

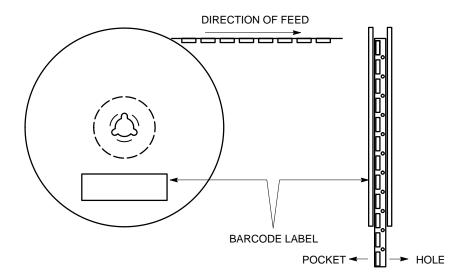
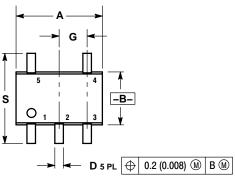


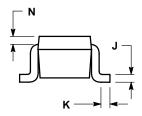
Figure 13. Reel Winding Direction

PACKAGE DIMENSIONS

SC70-5/SC-88A/SOT-353 **DF SUFFIX**

5-LEAD PACKAGE CASE 419A-02 ISSUE G





- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. 419A-01 OBSOLETE. NEW STANDARD
- 419A-02.
 DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	INC	HES	MILLIM	ETERS
DIM	MIN	MAX	MIN	MAX
Α	0.071	0.087	1.80	2.20
В	0.045	0.053	1.15	1.35
С	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026	BSC	0.65	BSC
Н		0.004		0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20	REF
S	0.079	0.087	2.00	2.20

SOLDERING FOOTPRINT*

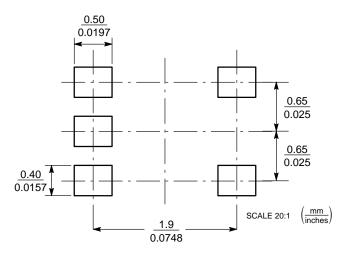


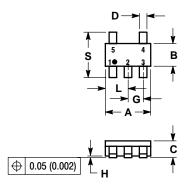
Figure 14. SC-88A/SC70-5/SOT-353

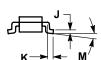
^{*}For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

SOT23-5/TSOP-5/SC59-5 **DT SUFFIX**

5-LEAD PACKAGE CASE 483-01 ISSUE C





NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- ANSI 114-3M, 1992.
 CONTROLLING DIMENSION: MILLIMETER.
 MAXIMUM LEAD THICKNESS INCLUDES
 LEAD FINISH THICKNESS. MINIMUM LEAD
 THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
- A AND B DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	2.90	3.10	0.1142	0.1220
В	1.30	1.70	0.0512	0.0669
С	0.90	1.10	0.0354	0.0433
D	0.25	0.50	0.0098	0.0197
G	0.85	1.05	0.0335	0.0413
н	0.013	0.100	0.0005	0.0040
J	0.10	0.26	0.0040	0.0102
K	0.20	0.60	0.0079	0.0236
L	1.25	1.55	0.0493	0.0610
М	0	10	0	10
S	2.50	3.00	0.0985	0.1181

SOLDERING FOOTPRINT*

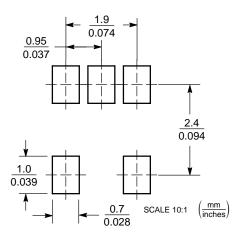


Figure 15. THIN SOT23-5/TSOP-5/SC59-5

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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