

Digital Control Compatible Dual Low-Side ± 4 Amp MOSFET Drivers with Single Common Current Sense

FEATURES

- Adjustable Current Limit Protection
- 3.3-V, 10-mA Internal Regulator
- DSP/ μ C Compatible Inputs
- Dual ± 4 -A TrueDrive™ High Current Drivers
- 10-ns Typical Rise and Fall Times with 2.2-nF Loads
- 25-ns Input-to-Output Propagation Delay
- Programmable Current Limit Threshold
- Digital Output Current Limit Flag
- 4.5-V to 15-V Supply Voltage Range
- Rated from -40°C to 105°C
- Lead(Pb)-Free Packaging

APPLICATIONS

- Digitally Controlled Power Supplies
- DC/DC Converters
- Motor Controllers
- Line Drivers

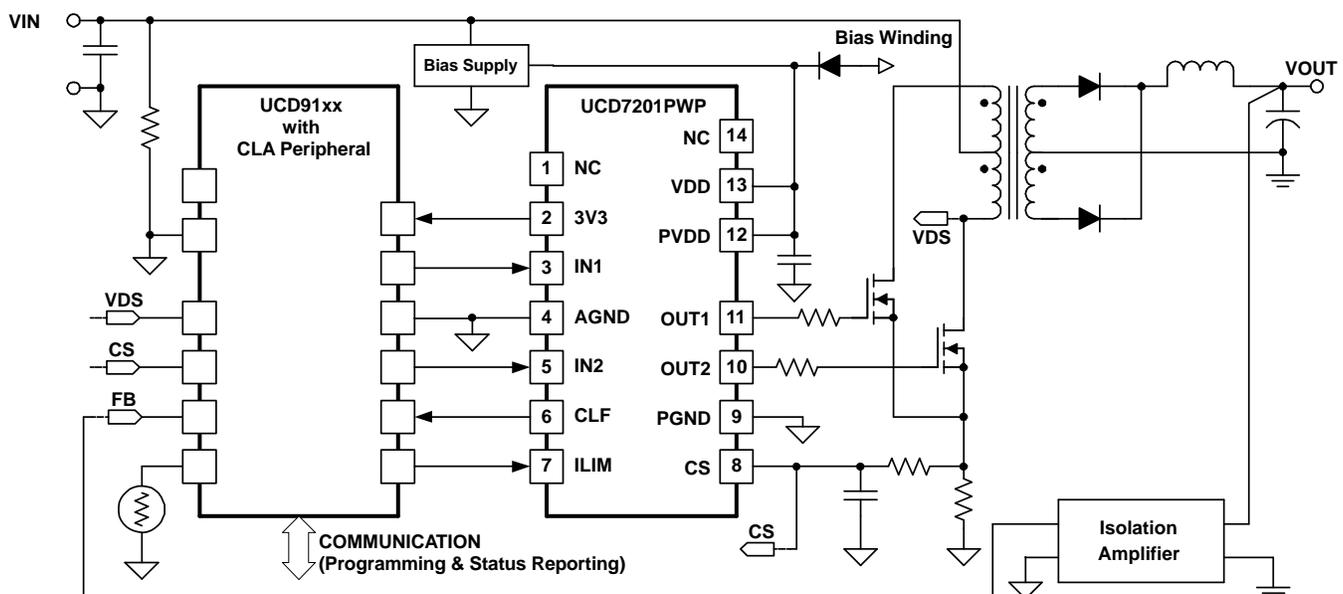
DESCRIPTION

The UCD7201 is a member of the UCD7K family of digital control compatible drivers for applications utilizing digital control techniques or applications requiring fast local peak current limit protection.

The UCD7201 includes dual low-side ± 4 -A high-current MOSFET gate drivers. It allows the digital power controllers such as UCD9110 or UCD9501 to interface to the power stage in double ended topologies. It provides a cycle-by-cycle current limit function for both driver channels, a programmable threshold and a digital output current limit flag which can be monitored by the host controller. With a fast cycle-by-cycle current limit protection, the driver can turn off the power stage in the event of an overcurrent condition.

For fast switching speeds, the UCD7201 output stages use the TrueDrive™ output architecture, which delivers rated current of ± 4 A into the gate of a MOSFET during the Miller plateau region of the switching transition. It also includes a 3.3-V, 10-mA linear regulator to provide power to the digital controller.

TYPICAL APPLICATION DIAGRAMS



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

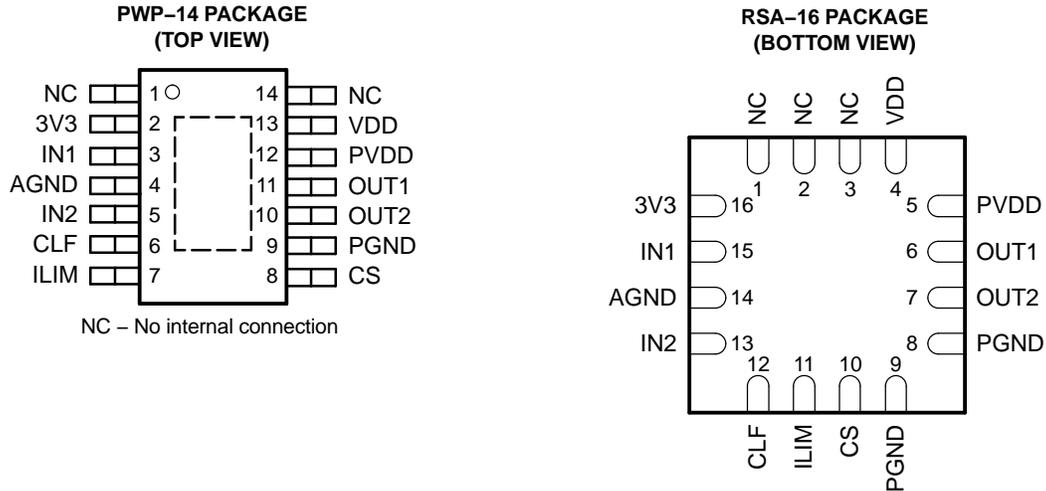
TrueDrive, PowerPAD are trademarks of Texas Instruments.

DESCRIPTION (CONT.)

For similar applications requiring direct start-up capability from higher voltages such as the 48-V telecom input line, the UCD7601 includes 110-V high-voltage startup circuit.

The UCD7K driver family is compatible with standard 3.3-V I/O ports of DSPs, Microcontrollers, or ASICs. UCD7201 is offered in PowerPAD™ HTSSOP-14 or space-saving QFN-16 packages.

CONNECTION DIAGRAMS



ORDERING INFORMATION

TEMPERATURE RANGE	CURRENT SENSE LIMIT PER CHANNEL	110-V HV STARTUP CIRCUIT	PACKAGED DEVICES ⁽¹⁾⁽²⁾	
			PowerPAD™ HTSSOP-14 (PWP)	QFN-16 (RSA)
-40°C to 105°C	Common	No	UCD7201PWP	UCD7201RSA

- (1) These products are packaged in Pb-Free and Green lead finish of Pd-Ni-Au which is compatible with MSL level 1 at 255°C to 260°C peak reflow temperature to be compatible with either lead free or Sn/Pb soldering operations.
- (2) HTSSOP-14 (PWP) and QFN-16 (RSA), packages are available taped and reeled. Add R suffix to device type (e.g. UCD7201PWPR) to order quantities of 2,000 devices per reel for the PWP package and 1,000 devices per reel for the RSA packages.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾⁽²⁾

SYMBOL	PARAMETER		UCD7201	UNIT
V _{DD}	Supply Voltage		16	V
I _{DD}	Supply Current	Quiescent	20	mA
		Switching	200	
V _{OUT}	Output Gate Drive Voltage	OUT	-1 to PVDD	V
I _{OUT(sink)}	Output Gate Drive Current	OUT	4.0	A
I _{OUT(source)}			-4.0	
	Analog Input	ISET, CS	-0.3 to 3.6	V
		ILIM	-0.3 to 3.6	
	Digital I/O's	IN, CLF	-0.3 to 3.6	
	Power Dissipation	T _A = 25°C (PWP-14 package)	2	W
		T _A = 25°C (QFN-16 package)	2	
T _J	Junction Operating Temperature	UCD7201	-55 to 150	°C
T _{str}	Storage Temperature		-65 to 150	
HBM	ESD Rating	Human body model	2000	V
CDM		Change device model	500	
T _{SOL}	Lead Temperature (Soldering, 10 sec)		+300	°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	TYP	MAX	UNIT
Supply voltage, VDD	4.25	12	14.5	V
Supply bypass capacitance	4.7			μF
Reference bypass capacitance	0.22			
Operating junction temperature	-40		105	°C

ELECTRICAL CHARACTERISTICS

$V_{DD} = 12\text{ V}$, 4.7- μF capacitor from V_{DD} to GND, $T_A = T_J = -40^\circ\text{C}$ to 105°C , (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY SECTION					
Supply current, OFF	$V_{DD} = 4.2\text{ V}$		200	400	μA
Supply current	Outputs not switching IN = LOW		2	4	mA
LOW VOLTAGE UNDER-VOLTAGE LOCKOUT					
VDD UVLO ON		4.25	4.5	4.75	V
VDD UVLO OFF		4.05	-	4.45	
VDD UVLO hysteresis		150	250	350	mV
REFERENCE / EXTERNAL BIAS SUPPLY					
3V3 initial set point	$T_A = 25^\circ\text{C}$	3.267	0	3.333	mV
3V3 over temperature		3.234	0	3.366	
3V3 load regulation	$I_{LOAD} = 1\text{ mA}$ to 10 mA , $V_{DD} = 5\text{ V}$		1	7	
3V3 line regulation	$V_{DD} = 4.75\text{ V}$ to 12 V , $I_{LOAD} = 10\text{ mA}$		1	7	
Short circuit current	$V_{DD} = 4.75$ to 12 V	11	20	35	mA
3V3 OK threshold, ON	3.3 V rising	2.9	3.0	3.1	V
3V3 OK threshold, OFF	3.3 V falling	2.7	2.8	2.8	
INPUT SIGNAL					
HIGH, positive-going input threshold voltage (VIT+)		1.65		2.08	V
LOW negative-going input threshold voltage (VIT-)		1.16		1.5	
Input voltage hysteresis, (VIT+ - VIT-)		0.6		0.8	
Frequency				2	MHz
CURRENT LIMIT (ILIM)					
ILIM internal current limit threshold	ILIM = OPEN	0.51	0.55	0.58	V
ILIM maximum current limit threshold	$I_{LIM} = 3.3\text{ V}$	1.05	1.10	1.15	V
ILIM current limit threshold	$I_{LIM} = 0.75\text{ V}$	0.700	0.725	0.750	
ILIM minimum current limit threshold	$I_{LIM} = 0.25\text{ V}$	0.21	0.23	0.25	mV
CLF output high level	$CS > I_{LIM}$, $I_{LOAD} = 7\text{ mA}$	2.64			V
CLF output low level	$CS \leq I_{LIM}$, $I_{LOAD} = 7\text{ mA}$			0.66	
Propagation delay from IN to CLF	IN rising to CLF falling after a current limit event		15	20	ns
CURRENT SENSE COMPARATOR					
Bias voltage	Includes CS comp offset	5	25	50	mV
Input bias current			-1		μA
Propagation delay from CS to OUTx	$I_{LIM} = 0.5\text{ V}$, measured on OUTx, CS = threshold + 60 mV		25	40	ns
Propagation delay from CS to CLF	$I_{LIM} = 0.5\text{ V}$, measured on CLF, CS = threshold + 60 mV		25	50	
CURRENT SENSE DISCHARGE TRANSISTOR					
Discharge resistance	IN = low, resistance from CS to AGND	10	35	75	Ω

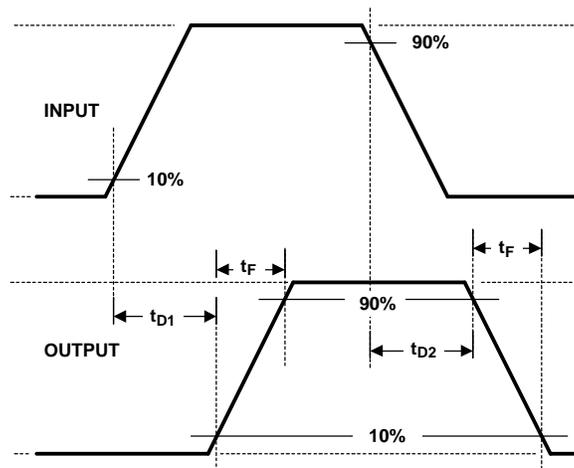
ELECTRICAL CHARACTERISTICS (continued)

$V_{DD} = 12\text{ V}$, $4.7\text{-}\mu\text{F}$ capacitor from V_{DD} to GND, $T_A = T_J = -40^\circ\text{C}$ to 105°C , (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT DRIVERS					
Source current ⁽¹⁾	$V_{DD} = 12\text{ V}$, IN = high, OUTx = 5 V		4		A
Sink current ⁽¹⁾	$V_{DD} = 12\text{ V}$, IN = low, OUTx = 5 V		4		
Source current ⁽¹⁾	$V_{DD} = 4.75\text{ V}$, IN = high, OUTx = 0		2		
Source current ⁽¹⁾	$V_{DD} = 4.75\text{ V}$, IN = low, OUTx = 4.75 V		3		
Rise Time	$C_{LOAD} = 2.2\text{ nF}$, $V_{DD} = 12\text{ V}$		10	20	ns
Fall time	$C_{LOAD} = 2.2\text{ nF}$, $V_{DD} = 12\text{ V}$		10	15	
Output with $V_{DD} < UVLO$	$V_{DD} = 1.0\text{ V}$, $I_{SINK} = 10\text{ mA}$		0.8	1.2	V
Propagation delay from IN to OUTx	$C_{LOAD} = 2.2\text{ nF}$, $V_{DD} = 12\text{ V}$, CLK rising		20	35	ns

(1) Ensured by design. Not 100% tested in production

FUNCTIONAL BLOCK DIAGRAM



NOTE:

The 10% and 90% thresholds depict the dynamics of the bipolar output devices that dominate the power MOSFET transition through the Miller regions of operation.

FUNCTIONAL BLOCK DIAGRAM (continued)

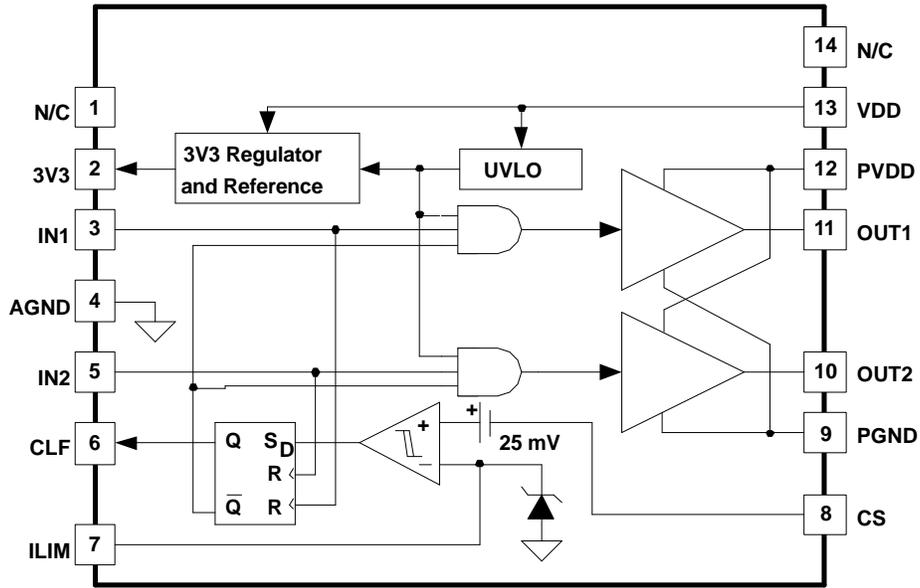


Figure 1. UCD7201

TERMINAL FUNCTIONS

UCD7201		PIN NAME	I/O	FUNCTION
HTSSOP -14 PIN #	QFN-16 PIN #			
1	-	N/C	-	No Connection
2	1	3V3	O	Regulated 3.3-V rail. The onboard linear voltage regulator is capable of sourcing up to 10 mA of current. Place a minimum of 0.22 μ F of ceramic capacitance from the pin to ground.
3	2	IN1	I	The IN pin is a high impedance digital input capable of accepting 3.3-V logic level signals up to 2 MHz. There is an internal Schmitt trigger comparator which isolates the internal circuitry from any external noise.
4	3	AGND	-	Analog ground return.
5	4	IN2	I	The IN pin is a high impedance digital input capable of accepting 3.3-V logic level signals up to 2 MHz. There is an internal Schmitt trigger comparator which isolates the internal circuitry from any external noise.
6	5	CLF	O	Current limit flag. When the CS level is greater than the ILIM voltage minus 25 mV, the output of the driver is forced low and the current limit flag (CLF) is set high. The CLF signal is latched high until the UCD7K device receives the next rising edge on the IN pin.
7	6	ILIM	I	Current limit threshold set pin. The current limit threshold can be set to any value between 0.25 V and 1.0 V.
8	7	CS	I	Current sense pin. Fast current limit comparator connected to the CS pin is used to protect the power stage by implementing cycle-by-cycle current limiting.
9	8, 9	PGND	-	Power ground return. Connect the two PGNDs together. These ground pins should be connected very closely to the source of the power MOSFET.
10	10	OUT2	O	The high-current TrueDrive™ driver output. Connect the two OUT pins together.
11	11	OUT1	O	The high-current TrueDrive™ driver output. Connect the two OUT pins together.
12	12	PVDD	I	Supply pin provides power for the output drivers. It is not connected internally to the VDD supply rail. Connect the two PVDD pins together.
13	13	VDD	I	Supply input pin to power the driver. The UCD7K devices accept an input range of 4.25 V to 15 V.
14	14, 15, 16	N/C	-	No Connection.

APPLICATION INFORMATION

The UCD7201 is member of the UCD7K family of digital compatible drivers targeting applications utilizing digital control techniques or applications that require local fast peak current limit protection.

Supply

The UCD7K devices accept a supply range of 4.5 V to 15 V. The device has an internal precision linear regulator that produces the 3V3 output from this VDD input. A separate pin, PVDD, not connected internally to the VDD supply rail provides power for the output drivers. In all applications the same bus voltage supplies the two pins. It is recommended that a low value of resistance be placed between the two pins so that the local capacitance on each pin forms low pass filters to attenuate any switching noise that may be on the bus.

Although quiescent VDD current is low, total supply current depends on the gate drive output current required for capacitive load and switching frequency. Total VDD current is the sum of quiescent VDD current and the average OUT current. Knowing the operating frequency and the MOSFET gate charge (Q_G), average OUT current can be calculated from:

$I_{OUT} = Q_G \times f$, where f is frequency.

For the best high-speed circuit performance, two VDD bypass capacitors are recommended to prevent noise problems. A 0.1- μ F ceramic capacitor should be located closest to the VDD to ground connection. In addition, a larger capacitor (such as 4.7 μ F) with relatively low ESR should be connected in parallel, to help deliver the high current peaks to the load. The parallel combination of capacitors should present a low impedance characteristic for the expected current levels in the driver application. The use of surface mount components for the capacitors is highly recommended.

Reference / External Bias Supply

All devices in the UCD7K family are capable of supplying a regulated 3.3-V rail to power various types of external loads such as a microcontroller or an ASIC. The onboard linear voltage regulator is capable of sourcing up to 10 mA of current. For normal operation, place a minimum of 0.22- μ F of ceramic capacitance from the 3V3 pin to ground.

Input Pin

The input pins are high impedance digital inputs capable of accepting 3.3-V logic level signals up to 2 MHz. There is an internal Schmitt Trigger comparator which isolates the internal circuitry from any external noise.

If limiting the rise or fall times to the power device is desired then an external resistance can be added between the output of the driver and the load device, which is generally a power MOSFET gate. The external resistor may also help remove power dissipation from the package.

Current Sensing and Protection

A very fast current limit comparator connected to the CS pin is used to protect the power stage by implementing cycle-by-cycle current limiting.

The current limit threshold is equal to the lesser of the positive inputs at the current limit comparator. The current limit threshold can be set to any value between 0.25 V and 1.0 V by applying the desired threshold voltage to the current limit (ILIM) pin. When the CS level is greater than the I_{LIM} voltage minus 25 mV, the output of the driver is forced low and the current limit flag (CLF) is set high. The CLF signal is latched high until the UCD7K device receives the next rising edge on the IN pin.

When the CS voltage is below I_{LIM} , the driver output follows the PWM input. The CLF digital output flag can be monitored by the host controller to determine when a current limit event occurs and to then apply the appropriate algorithm to obtain the desired current limit profile.

APPLICATION INFORMATION (continued)

One of the main benefits of this local protection feature is that the UCD7K devices can protect the power stage if the software code in the digital controller becomes corrupted and hangs up. If the controller's PWM output stays high, the local current sense circuit turns off the driver output when an over-current condition occurs. The system would likely go into a retry mode because; most DSP and microcontrollers have on-board watchdog, brown-out, and other supervisory peripherals to restart the device in the event that it is not operating properly. But these peripherals typically do not react fast enough to save the power stage. The UCD7K's local current limit comparator provides the required fast protection for the power stage.

The CS threshold is 25 mV below the I_{LIM} voltage. If the user attempts to command zero current ($I_{LIM} < 25$ mV) while the CS pin is at ground, for example at start-up, the CLF flag will latch high until the IN pin receives a pulse. At start-up it is necessary to ensure that the ILIM pin will always be greater than the CS pin for the handshaking to work as described below. If for any reason the CS pin comes to within 25 mV of the ILIM pin during start-up, then the CLF flag will be latched high and the digital controller must poll the UCD7K device, by sending it a narrow IN pulse. If a fault condition is not present the IN pulse will reset the CLF signal to low indicating that the UCD7K device is ready to process power pulses.

Handshaking

The UCD7K family of devices have a built-in handshaking feature to facilitate efficient start-up of the digitally controlled power supply. At start-up the CLF flag is held high until all the internal and external supply voltages of the UCD7K device are within their operating range. Once the supply voltages are within acceptable limits, the CLF goes low and the device will process input drive signals. The micro-controller should monitor the CFL flag at start-up and wait for the CLF flag to go LOW before sending power pulses to the UCD7K device.

Driver Output

The high-current output stage of the UCD7K device family is capable of supplying ± 4 -A peak current pulses and swings to both VDD and GND. The driver outputs follow the state of the IN pin provided that the VDD and 3V3 voltages are above their respective under-voltage lockout threshold..

The drive output utilizes Texas Instruments' TrueDrive™ architecture, which delivers rated current into the gate of a MOSFET when it is most needed, during the Miller plateau region of the switching transition providing efficiency gains.

TrueDrive™ consists of pullup/ pulldown circuits with bipolar and MOSFET transistors in parallel. The peak output current rating is the combined current from the bipolar and MOSFET transistors. The output resistance is the RDS(on) of the MOSFET transistor when the voltage on the driver output is less than the saturation voltage of the bipolar transistor. This hybrid output stage also allows efficient current sourcing at low supply voltages.

Each output stage also provides a very low impedance to overshoot and undershoot due to the body diode of the external MOSFET. This means that in many cases, external-schottky-clamp diodes are not required.

Source/Sink Capabilities During Miller Plateau

Large power MOSFETs present a large load to the control circuitry. Proper drive is required for efficient, reliable operation. The UCD7K drivers have been optimized to provide maximum drive to a power MOSFET during the Miller plateau region of the switching transition. This interval occurs while the drain voltage is swinging between the voltage levels dictated by the power topology, requiring the charging/discharging of the drain-gate capacitance with current supplied or removed by the driver device. See Reference [1]

Drive Current and Power Requirements

The UCD7K family of drivers can delivering high current into a MOSFET gate for a period of several hundred nanoseconds. High peak current is required to turn the device ON quickly. Then, to turn the device OFF, the driver is required to sink a similar amount of current to ground. This repeats at the operating frequency of the power device. A MOSFET is used in this discussion because it is the most common type of switching device used in high frequency power conversion equipment.

Reference [1] discusses the current required to drive a power MOSFET and other capacitive-input switching devices.

APPLICATION INFORMATION (continued)

When a driver device is tested with a discrete, capacitive load it is a fairly simple matter to calculate the power that is required from the bias supply. The energy that must be transferred from the bias supply to charge the capacitor is given by:

$$E = \frac{1}{2} \times CV^2$$

where C is the load capacitor and V is the bias voltage feeding the driver.

There is an equal amount of energy transferred to ground when the capacitor is discharged. This leads to a power loss given by the following:

$$P = \frac{1}{2} \times CV^2 \times f$$

where f is the switching frequency.

This power is dissipated in the resistive elements of the circuit. Thus, with no external resistor between the driver and gate, this power is dissipated inside the driver. Half of the total power is dissipated when the capacitor is charged, and the other half is dissipated when the capacitor is discharged. An actual example using the conditions of the previous gate drive waveform should help clarify this.

With $V_{DD} = 12\text{ V}$, $C_{LOAD} = 10\text{ nF}$, and $f = 300\text{ kHz}$, the power loss can be calculated as:

$$P = 10\text{ nF} \times 12^2 \times 300\text{ kHz} = 0.432\text{ W}$$

With a 12-V supply, this would equate to a current of:

$$I = \frac{P}{V} = \frac{0.432\text{ W}}{12\text{ V}} = 0.036\text{ A}$$

The actual current measured from the supply was 0.037 A, and is very close to the predicted value. But, the I_{DD} current that is due to the device internal consumption should be considered. With no load the device current draw is 0.0027 A. Under this condition the output rise and fall times are faster than with a load. This could lead to an almost insignificant, yet measurable current due to cross-conduction in the output stages of the driver. However, these small current differences are buried in the high frequency switching spikes, and are beyond the measurement capabilities of a basic lab setup. The measured current with 10-nF load is close to the value expected.

The switching load presented by a power MOSFET can be converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain of the device between the ON and OFF states. Most manufacturers provide specifications that provide the typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Q_G , one can determine the power that must be dissipated when charging a capacitor. This is done by using the equivalence $Q_G = C_{EFF} \times V$ to provide the following equation for power:

$$P = C \times V^2 \times f = Q_G \times f$$

This equation allows a power designer to calculate the bias power required to drive a specific MOSFET gate at a specific bias voltage.

APPLICATION INFORMATION (continued)

Thermal Information

The useful range of a driver is greatly affected by the drive power requirements of the load and the thermal characteristics of the device package. In order for a power driver to be useful over a particular temperature range the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The UCD7K family of drivers is available in PowerPAD™ TSSOP and QFN/DFN packages to cover a range of application requirements. Both have an exposed pad to enhance thermal conductivity from the semiconductor junction.

As illustrated in Reference [2], the PowerPAD™ packages offer a leadframe die pad that is exposed at the base of the package. This pad is soldered to the copper on the PC board (PCB) directly underneath the device package, reducing the T_{JC} down to 4.7°C/W. The PC board must be designed with thermal lands and thermal vias to complete the heat removal subsystem, as summarized in Reference [3].

Note that the PowerPAD™ is not directly connected to any leads of the package. However, it is electrically and thermally connected to the substrate which is the ground of the device. The PowerPad™ should be connected to the quiet ground of the circuit.

Circuit Layout Recommendations

In a power driver operating at high frequency, it is a significant challenge to get clean waveforms without much overshoot/undershoot and ringing. The low output impedance of these drivers produces waveforms with high di/dt . This tends to induce ringing in the parasitic inductances. Utmost care must be used in the circuit layout. It is advantageous to connect the driver device as close as possible to the leads. The driver device layout has the analog ground on the opposite side of the output, so the ground should be connected to the bypass capacitors and the load with copper trace as wide as possible. These connections should also be made with a small enclosed loop area to minimize the inductance.

REFERENCES

1. Power Supply Seminar SEM-1400 Topic 2: Design And Application Guide For High Speed MOSFET Gate Drive Circuits, by Laszlo Balogh, Texas Instruments Literature No. SLUP133.
2. Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002
3. Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004

RELATED PRODUCTS

Temperature Range	Current Sense Limit per Channel	110-V HV Startup Circuit
UCD7100	Single Low Side ± 4 -A Driver with Independent CS	3V3, CS ⁽¹⁾⁽²⁾
UCD7200	Dual Low Side ± 4 -A Drivers with Independent CS	3V3, CS ⁽¹⁾⁽²⁾
UCD7230	± 4 -A Synchronous Buck Driver with CS	3V3, CS ⁽¹⁾⁽²⁾
UCD7500	Single Low Side ± 4 -A Driver with CS and 110-V High Voltage Startup	3v3, CS, HVS110 ⁽¹⁾⁽²⁾⁽³⁾
UCD7600	Dual Low Side ± 4 -A Drivers with Independent CS and 110-V High Voltage Startup	3V3, CS, HVS110 ⁽¹⁾⁽²⁾⁽³⁾
UCD7601	Dual Low Side ± 4 -A Drivers with Common CS and 110-V High Voltage Startup	3V3, CCS, HVS110 ⁽¹⁾⁽⁴⁾⁽³⁾
UCD9110	Digital Power Controller for High Performance Single-loop Applications	
UCD9501	Digital Power Controller for High Performance Multi-Loop Applications	

- (1) 3V3 = 3.3-V linear regulator.
 (2) CS = current sense and current limit function.
 (3) HVS110 = 110-V high voltage startup circuit.
 (4) CCS = Common current sense and current limit function.

REVISION HISTORY

DATE	REVISION	CHANGE DESCRIPTION
3/4/05	SLUS645	Initial release

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
UCD7201PWP	PREVIEW	HTSSOP	PWP	14	90	TBD	Call TI	Call TI
UCD7201PWPR	PREVIEW	HTSSOP	PWP	14	2000	TBD	Call TI	Call TI
UCD7201RSAR	PREVIEW	QFN	RSA	16	3000	TBD	Call TI	Call TI
UCD7201RSAT	PREVIEW	QFN	RSA	16	250	TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

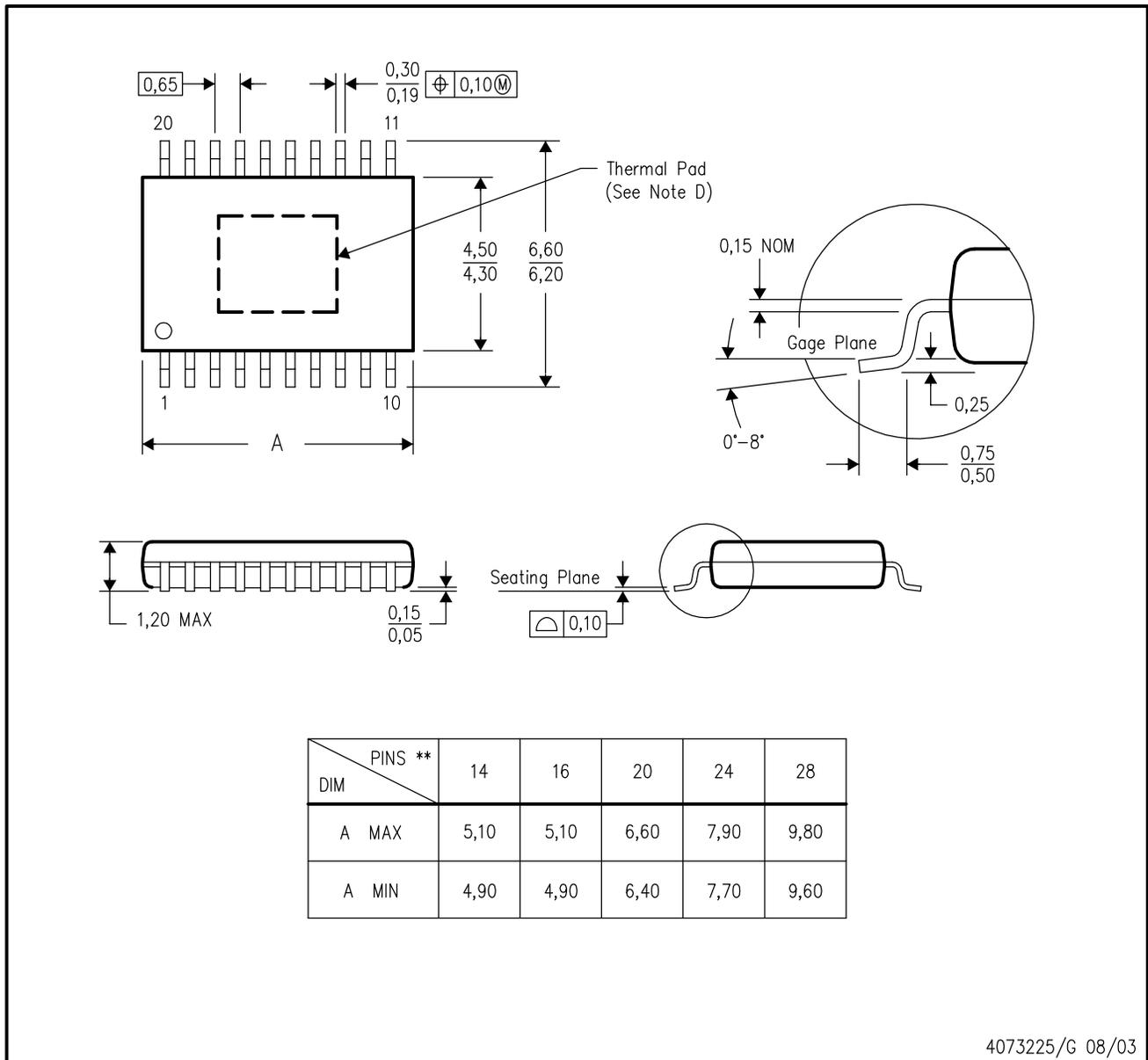
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PWP (R-PDSO-G**) 20 PIN SHOWN

PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE



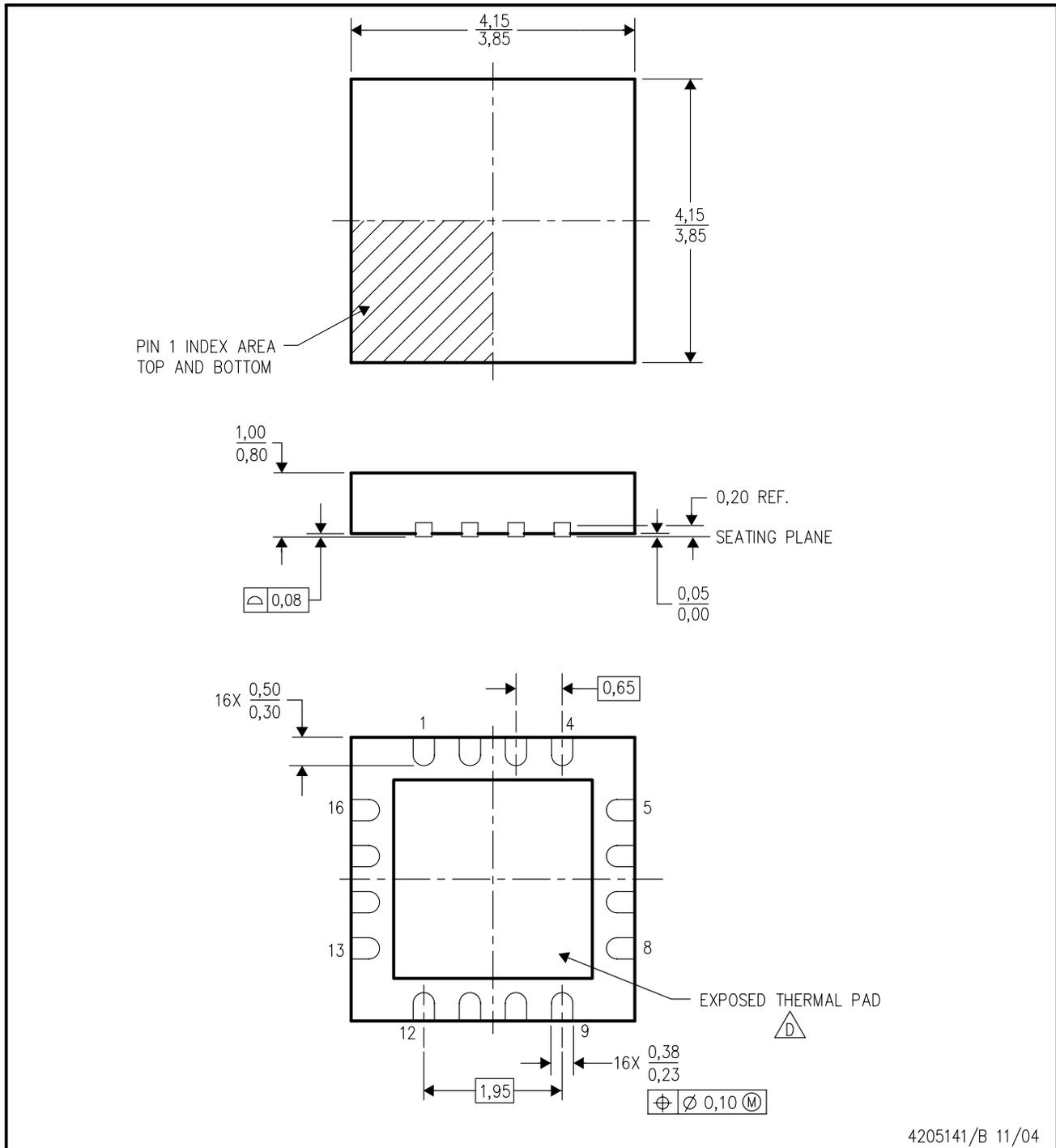
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- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusions.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - E. Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

RSA (S-PQFP-N16)

PLASTIC QUAD FLATPACK



4205141/B 11/04

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Quad Flatpack, No-leads (QFN) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
 - E. Falls within JEDEC MO-220.

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