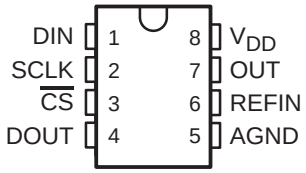
- **10-Bit CMOS Voltage Output DAC in an 8-Terminal Package**
- **5-V Single Supply Operation**
- **3-Wire Serial Interface**
- **High-Impedance Reference Inputs**
- **Voltage Output Range . . . 2 Times the Reference Input Voltage**
- **Internal Power-On Reset**
- **Low Power Consumption . . . 1.75 mW Max**
- **Update Rate of 1.21 MHz**
- **Settling Time to 0.5 LSB . . . 12.5 μs Typ**
- **Monotonic Over Temperature**
- **Pin Compatible With the Maxim MAX515**

applications

- **Battery-Powered Test Instruments**
- **Digital Offset and Gain Adjustment**
- **Battery Operated/Remote Industrial Controls**
- **Machine and Motion Control Devices**
- **Cellular Telephones**

D, P, OR DGK PACKAGE
(TOP VIEW)



description

The TLC5615 is a 10-bit voltage output digital-to-analog converter (DAC) with a buffered reference input (high impedance). The DAC has an output voltage range that is two times the reference voltage, and the DAC is monotonic. The device is simple to use, running from a single supply of 5 V. A power-on-reset function is incorporated to ensure repeatable start-up conditions.

Digital control of the TLC5615 is over a three-wire serial bus that is CMOS compatible and easily interfaced to industry standard microprocessor and microcontroller devices. The device receives a 16-bit data word to produce the analog output. The digital inputs feature Schmitt triggers for high noise immunity. Digital communication protocols include the SPI™, QSPI™, and Microwire™ standards.

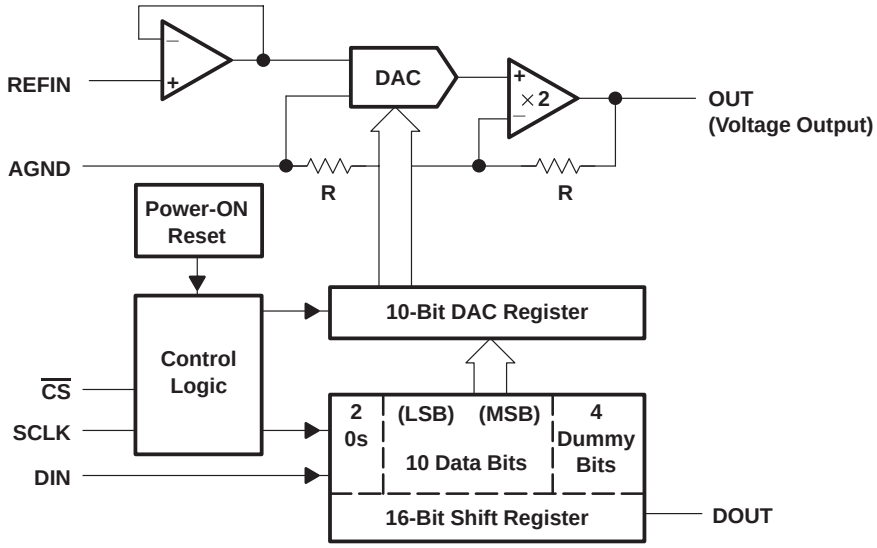
The 8-terminal small-outline D package allows digital control of analog functions in space-critical applications. The TLC5615C is characterized for operation from 0°C to 70°C. The TLC5615I is characterized for operation from –40°C to 85°C.

AVAILABLE OPTIONS

PACKAGE			
T_A	SMALL OUTLINE† (D)	PLASTIC SMALL OUTLINE (DGK)	PLASTIC DIP (P)
0°C to 70°C	TLC5615CD	TLC5615CDGK	TLC5615CP
–40°C to 85°C	TLC5615ID	TLC5615IDGK	TLC5615IP

† Available in tape and reel as the TLC5615CDR and the TLC5615IDR

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
DIN	1	I	Serial data input
SCLK	2	I	Serial clock input
$\overline{CS}$	3	I	Chip select, active low
DOUT	4	O	Serial data output for daisy chaining
AGND	5		Analog ground
REFIN	6	I	Reference input
OUT	7	O	DAC analog voltage output
V_{DD}	8		Positive power supply

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage (V_{DD} to AGND) . . . . . 7 V
Digital input voltage range to AGND . . . . . – 0.3 V to V_{DD} + 0.3 V
Reference input voltage range to AGND . . . . . – 0.3 V to V_{DD} + 0.3 V
Output voltage at OUT from external source . . . . . V_{DD} + 0.3 V
Continuous current at any terminal . . . . . ±20 mA
Operating free-air temperature range, T_A: TLC5615C . . . . . 0°C to 70°C
TLC5615I . . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		4.5	5	5.5	V
High-level digital input voltage, V_{IH}		2.4			V
Low-level digital input voltage, V_{IL}				0.8	V
Reference voltage, V_{ref} to REFIN terminal		2	2.048	$V_{DD}-2$	V
Load resistance, R_L		2			kΩ
Operating free-air temperature, T_A	TLC5615C	0		70	°C
	TLC5615I	–40		85	°C

electrical characteristics over recommended operating free-air temperature range, V_{DD} = 5 V ± 5%, V_{ref} = 2.048 V (unless otherwise noted)

static DAC specifications

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution			10			bits
	Integral nonlinearity, end point adjusted (INL)		V_{ref} = 2.048 V, See Note 1			±1	LSB
	Differential nonlinearity (DNL)		V_{ref} = 2.048 V, See Note 2		±0.1	±0.5	LSB
E_{ZS}	Zero-scale error (offset error at zero scale)		V_{ref} = 2.048 V, See Note 3			±3	LSB
	Zero-scale-error temperature coefficient		V_{ref} = 2.048 V, See Note 4		3		ppm/°C
E_G	Gain error		V_{ref} = 2.048 V, See Note 5			±3	LSB
	Gain-error temperature coefficient		V_{ref} = 2.048 V, See Note 6		1		ppm/°C
PSRR	Power-supply rejection ratio	Zero scale	See Notes 7 and 8	80			dB
		Gain		80			
	Analog full scale output		R_L = 100 kΩ		$2V_{ref}(1023/1024)$		V

NOTES:
1. The relative accuracy or integral nonlinearity (INL), sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale excluding the effects of zero code and full-scale errors (see text).
2. The differential nonlinearity (DNL), sometimes referred to as differential error, is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.
3. Zero-scale error is the deviation from zero-voltage output when the digital input code is zero (see text).
4. Zero-scale-error temperature coefficient is given by: E_{ZS} TC = $[E_{ZS}(T_{max}) - E_{ZS}(T_{min})]/V_{ref} \times 10^6/(T_{max} - T_{min})$.
5. Gain error is the deviation from the ideal output (V_{ref} – 1 LSB) with an output load of 10 kΩ excluding the effects of the zero-scale error.
6. Gain temperature coefficient is given by: E_G TC = $[E_G(T_{max}) - E_G(T_{min})]/V_{ref} \times 10^6/(T_{max} - T_{min})$.
7. Zero-scale-error rejection ratio (EZS-RR) is measured by varying the V_{DD} from 4.5 V to 5.5 V dc and measuring the proportion of this signal imposed on the zero-code output voltage.
8. Gain-error rejection ratio (EG-RR) is measured by varying the V_{DD} from 4.5 V to 5.5 V dc and measuring the proportion of this signal imposed on the full-scale output voltage after subtracting the zero-scale change.

voltage output (OUT)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Voltage output range	R_L = 10 kΩ	0		V_{DD}–0.4	V
	Output load regulation accuracy	$V_{O(OUT)}$ = 2 V, R_L = 2 kΩ			0.5	LSB
I_{OSC}	Output short circuit current	OUT to V_{DD} or AGND		20		mA
$V_{OL(low)}$	Output voltage, low-level	$I_{O(OUT)} \le$ 5 mA			0.25	V
$V_{OH(high)}$	Output voltage, high-level	$I_{O(OUT)} \le$ –5 mA	4.75			V

electrical characteristics over recommended operating free-air temperature range, V_{DD} = 5 V ± 5%, V_{ref} = 2.048 V (unless otherwise noted) (continued)

reference input (REFIN)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_I	Input voltage		0		V_{DD}–2	V
r_i	Input resistance		10			MΩ
C_i	Input capacitance			5		pF

digital inputs (DIN, SCLK, $\overline{CS}$)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level digital input voltage		2.4			V
V_{IL}	Low-level digital input voltage				0.8	V
I_{IH}	High-level digital input current	$V_I = V_{DD}$			±1	µA
I_{IL}	Low-level digital input current	V_I = 0			±1	µA
C_i	Input capacitance			8		pF

digital output (DOUT)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	Output voltage, high-level	I_O = –2 mA	V_{DD}–1			V
V_{OL}	Output voltage, low-level	I_O = 2 mA			0.4	V

power supply

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{DD}	Supply voltage			4.5	5	5.5	V
I_{DD}	Power supply current	V_{DD} = 5.5 V, No load, All inputs = 0 V or V_{DD}	V_{ref} = 0		150	250	µA
		V_{DD} = 5.5 V, No load, All inputs = 0 V or V_{DD}	V_{ref} = 2.048 V		230	350	µA

analog output dynamic performance

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Signal-to-noise + distortion, S/(N+D)	V_{ref} = 1 V_{pp} at 1 kHz + 2.048 Vdc, code = 11 1111 1111, See Note 9	60			dB

NOTE 9: The limiting frequency value at 1 Vpp is determined by the output-amplifier slew rate.

digital input timing requirements (see Figure 1)

PARAMETER		MIN	NOM	MAX	UNIT
$t_{su(DS)}$	Setup time, DIN before SCLK high	45			ns
$t_{h(DH)}$	Hold time, DIN valid after SCLK high	0			ns
$t_{su(CSS)}$	Setup time, $\overline{CS}$ low to SCLK high	1			ns
$t_{su(CS1)}$	Setup time, $\overline{CS}$ high to SCLK high	50			ns
$t_{h(CSH0)}$	Hold time, SCLK low to $\overline{CS}$ low	1			ns
$t_{h(CSH1)}$	Hold time, SCLK low to $\overline{CS}$ high	0			ns
$t_{w(CS)}$	Pulse duration, minimum chip select pulse width high	20			ns
$t_{w(CL)}$	Pulse duration, SCLK low	25			ns
$t_{w(CH)}$	Pulse duration, SCLK high	25			ns

output switching characteristic

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{pd(DOUT)}$	Propagation delay time, DOUT	C_L = 50 pF			50	ns

operating characteristics over recommended operating free-air temperature range, V_{DD} = 5 V ± 5%, V_{ref} = 2.048 V (unless otherwise noted)

analog output dynamic performance

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Output slew rate	C_L = 100 pF, T_A = 25°C	R_L = 10 kΩ,	0.3	0.5		V/μs
t_S	Output settling time	To 0.5 LSB, R_L = 10 kΩ,	C_L = 100 pF, See Note 10		12.5		μs
	Glitch energy	DIN = All 0s to all 1s			5		nV•s

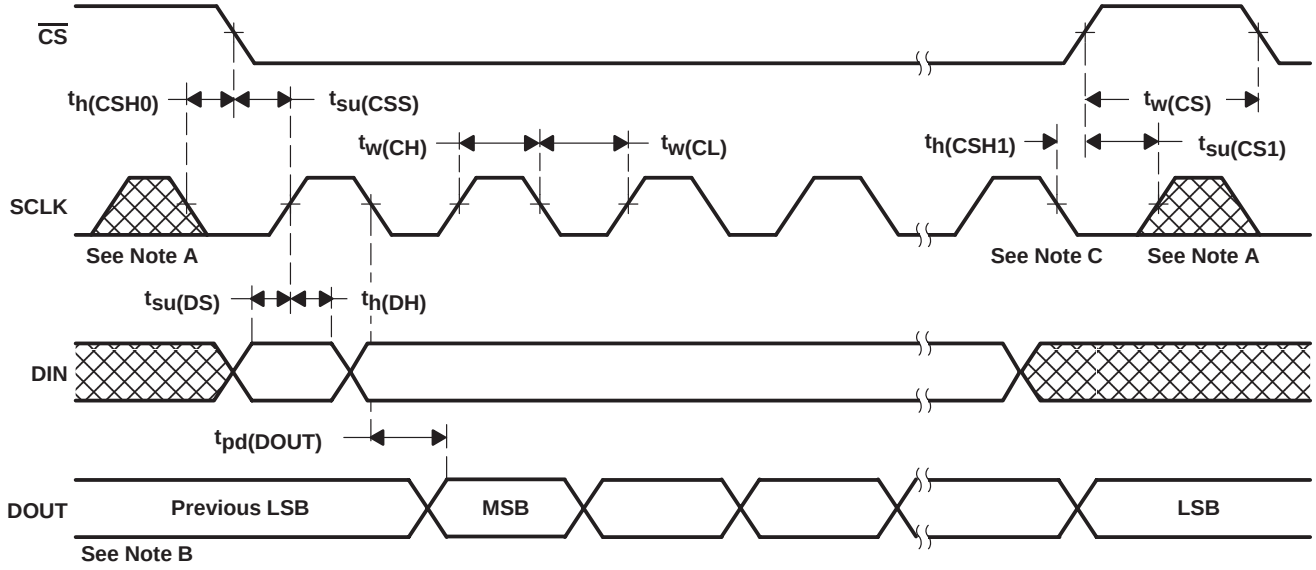
NOTE 10: Settling time is the time for the output signal to remain within ±0.5 LSB of the final measured value for a digital input code change of 000 hex to 3FF hex or 3FF hex to 000 hex.

reference input (REFIN)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Reference feedthrough	REFIN = 1 V_{pp} at 1 kHz + 2.048 Vdc (see Note 11)			–80		dB
	Reference input bandwidth (f–3dB)	REFIN = 0.2 V_{pp} + 2.048 Vdc	REFIN = 0.2 V_{pp} + 2.048 Vdc		30		kHz

NOTE 11: Reference feedthrough is measured at the DAC output with an input code = 000 hex and a V_{ref} input = 2.048 Vdc + 1 V_{pp} at 1 kHz.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The input clock, applied at the SCLK terminal, should be inhibited low when $\overline{CS}$ is high to minimize clock feedthrough.
B. Data input from preceeding conversion cycle.
C. Sixteenth SCLK falling edge

Figure 1. Timing Diagram

TYPICAL CHARACTERISTICS

**OUTPUT SINK CURRENT
vs
OUTPUT PULLDOWN VOLTAGE**

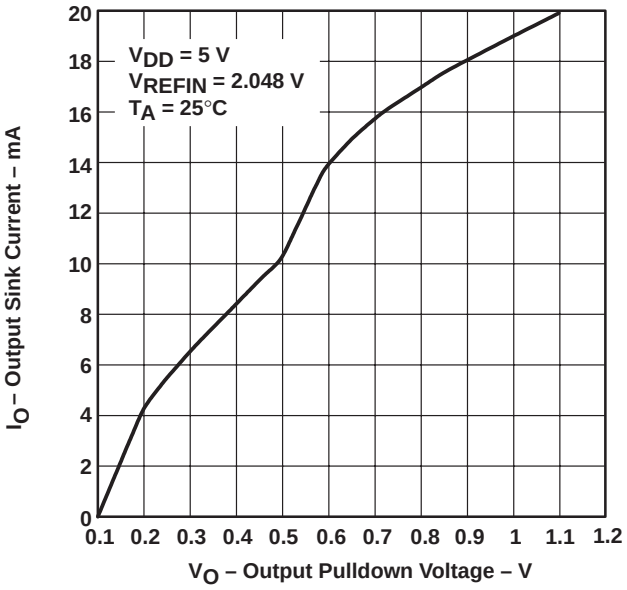


Figure 2

**OUTPUT SOURCE CURRENT
vs
OUTPUT PULLUP VOLTAGE**

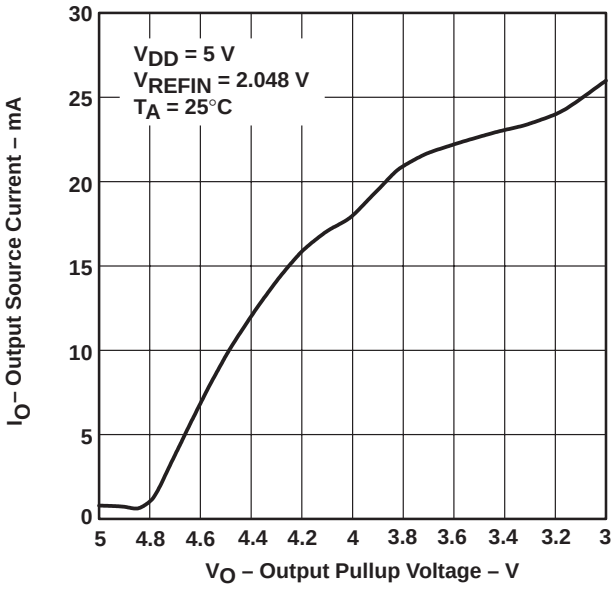


Figure 3

TYPICAL CHARACTERISTICS

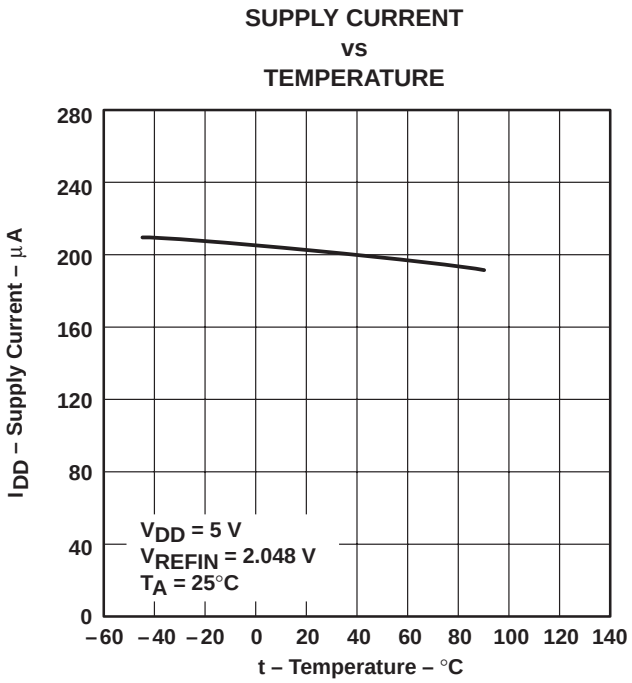


Figure 4

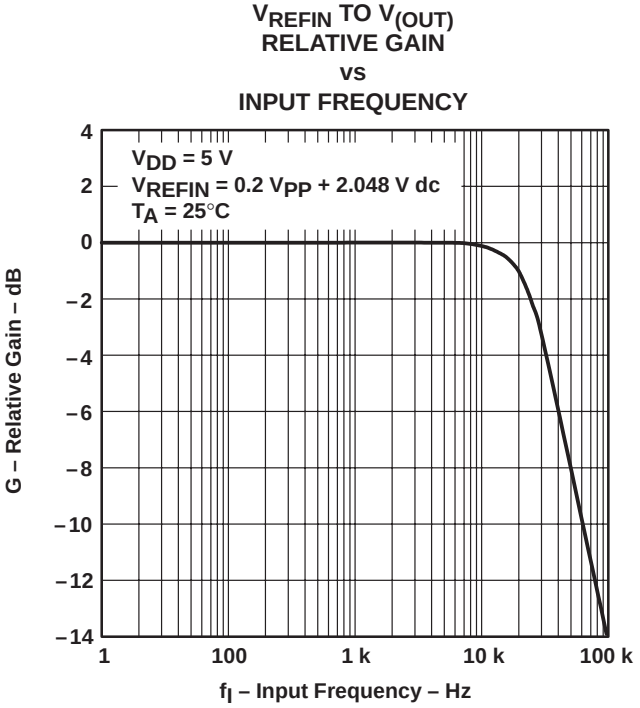


Figure 5

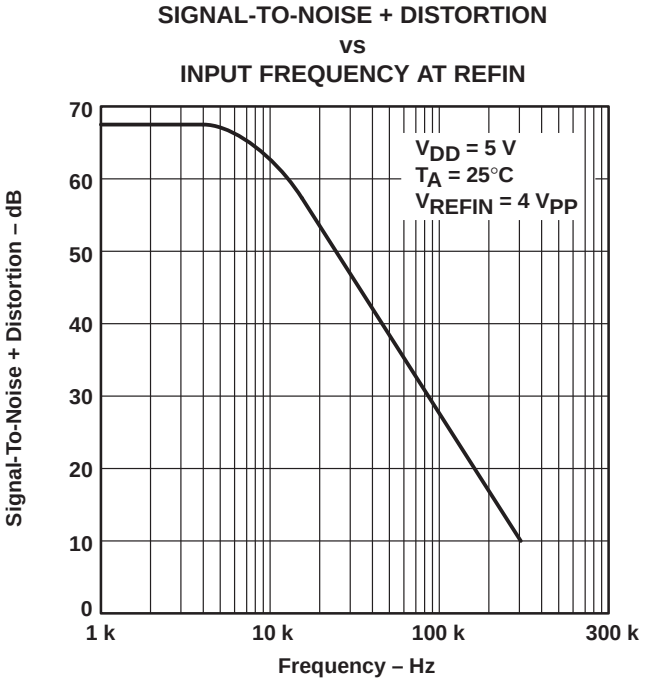


Figure 6

TYPICAL CHARACTERISTICS

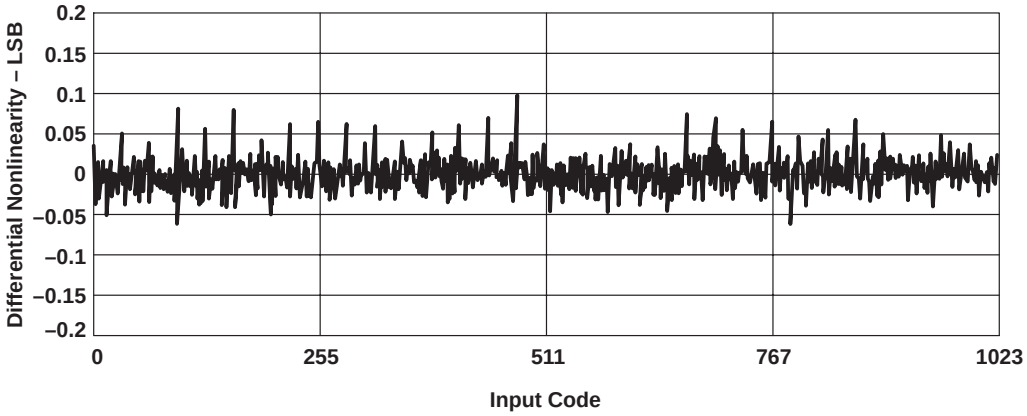


Figure 7. Differential Nonlinearity With Input Code

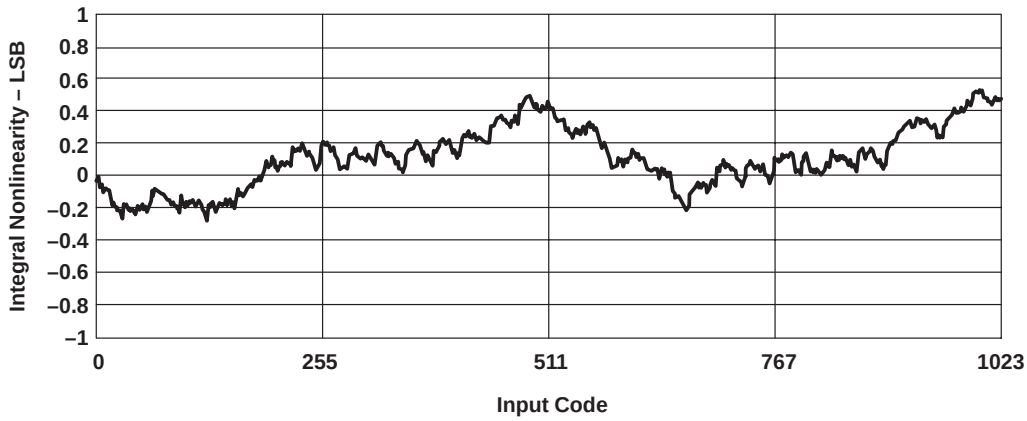


Figure 8. Integral Nonlinearity With Input Code

APPLICATION INFORMATION

general function

The TLC5615 uses a resistor string network buffered with an op amp in a fixed gain of 2 to convert 10-bit digital data to analog voltage levels (see functional block diagram and Figure 9). The output of the TLC5615 is the same polarity as the reference input (see Table 1).

An internal circuit resets the DAC register to all zeros on power up.

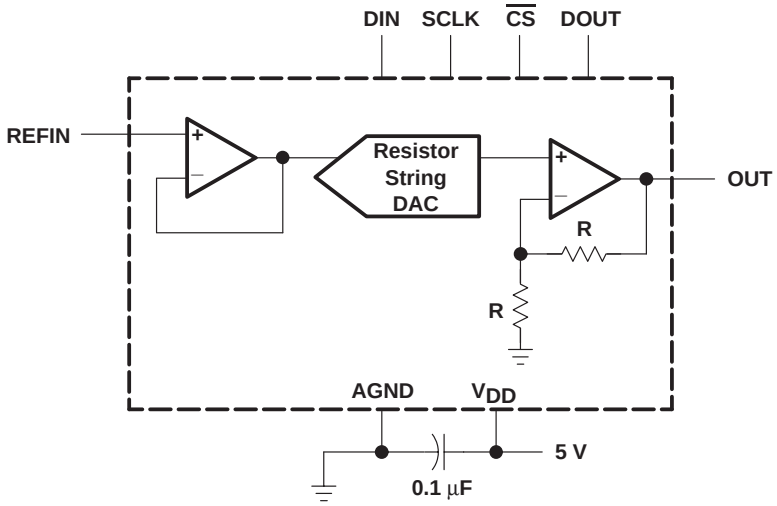


Figure 9. TLC5615 Typical Operating Circuit

Table 1. Binary Code Table (0 V to 2 V_{REFIN} Output), Gain = 2

INPUT†			OUTPUT
1111	1111	11(00)	$2\left(V_{REFIN}\right)\frac{1023}{1024}$
	:		:
1000	0000	01(00)	$2\left(V_{REFIN}\right)\frac{513}{1024}$
1000	0000	00(00)	$2\left(V_{REFIN}\right)\frac{512}{1024} = V_{REFIN}$
0111	1111	11(00)	$2\left(V_{REFIN}\right)\frac{511}{1024}$
	:		:
0000	0000	01(00)	$2\left(V_{REFIN}\right)\frac{1}{1024}$
0000	0000	00(00)	0 V

† A 10-bit data word with two bits below the LSB bit (sub-LSB) with 0 values must be written since the DAC input latch is 12 bits wide.

APPLICATION INFORMATION

buffer amplifier

The output buffer has a rail-to-rail output with short circuit protection and can drive a 2-kΩ load with a 100-pF load capacitance. Settling time is 12.5 μs typical to within 0.5 LSB of final value.

external reference

The reference voltage input is buffered, which makes the DAC input resistance not code dependent. Therefore, the REFIN input resistance is 10 MΩ and the REFIN input capacitance is typically 5 pF independent of input code. The reference voltage determines the DAC full-scale output.

logic interface

The logic inputs function with either TTL or CMOS logic levels. However, using rail-to-rail CMOS logic achieves the lowest power dissipation. The power requirement increases by approximately 2 times when using TTL logic levels.

serial clock and update rate

Figure 1 shows the TLC5615 timing. The maximum serial clock rate is:

$$f_{(SCLK)max} = \frac{1}{t_{w(CH)} + t_{w(CL)}}$$

or approximately 14 MHz. The digital update rate is limited by the chip-select period, which is:

$$t_{p(CS)} = 16 \times \left(t_{w(CH)} + t_{w(CL)} \right) + t_{w(CS)}$$

and is equal to 820 ns which is a 1.21 MHz update rate. However, the DAC settling time to 10 bits of 12.5 μs limits the update rate to 80 kHz for full-scale input step transitions.

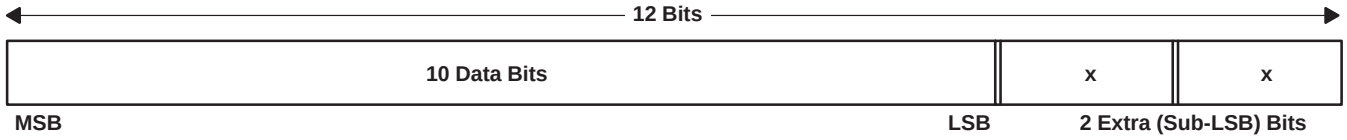
APPLICATION INFORMATION

serial interface

When chip select ($\overline{CS}$) is low, the input data is read into a 16-bit shift register with the input data clocked in most significant bit first. The rising edge of the SLCK input shifts the data into the input register.

The rising edge of $\overline{CS}$ then transfers the data to the DAC register. When $\overline{CS}$ is high, input data cannot be clocked into the input register. All $\overline{CS}$ transitions should occur when the SCLK input is low.

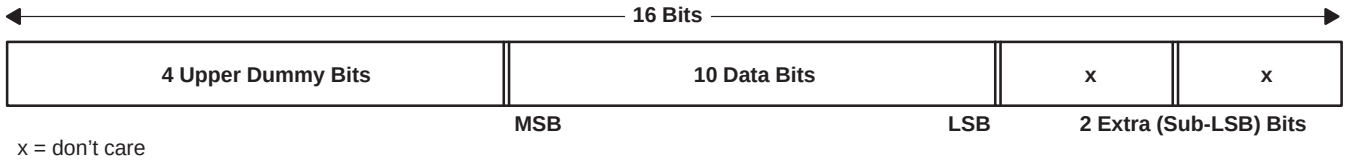
If the daisy chain (cascading) function (see daisy-chaining devices section) is not used, a 12-bit input data sequence with the MSB first can be used as shown in Figure 10:



x = don't care

Figure 10. 12-Bit Input Data Sequence

or 16 bits of data can be transferred as shown in Figure 11 with the 4 upper dummy bits first.



x = don't care

Figure 11. 16-Bit Input Data Sequence

The data from DOUT requires 16 falling edges of the input clock and, therefore, requires an extra clock width. When daisy chaining multiple TLC5615 devices, the data requires 4 upper dummy bits because the data transfer requires 16 input-clock cycles plus one additional input-clock falling edge to clock out the data at the DOUT terminal (see Figure 1).

The two extra (sub-LSB) bits are always required to provide hardware and software compatibility with 12-bit data converter transfers.

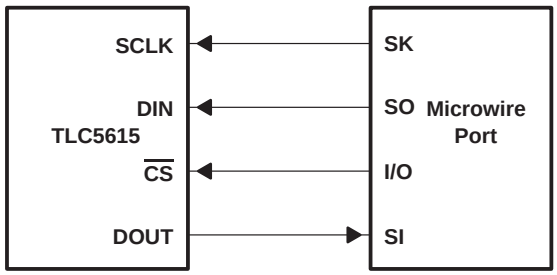
The TLC5615 three-wire interface is compatible with the SPI, QSPI†, and Microwire serial standards. The hardware connections are shown in Figure 12 and Figure 13.

The SPI and Microwire interfaces transfer data in 8-bit bytes, therefore, two write cycles are required to input data to the DAC. The QSPI interface, which has a variable input data length from 8 to 16 bits, can load the DAC input register in one write cycle.

† CPOL = 0, CPHA = 0, QSPI protocol designations

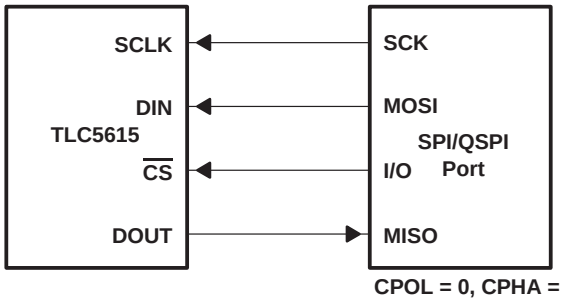
APPLICATION INFORMATION

serial interface (continued)



NOTE A: The DOUT-SI connection is not required for writing to the TLC5615 but may be used for verifying data transfer if desired.

Figure 12. Microwire Connection



NOTE A: The DOUT-MISO connection is not required for writing to the TLC5615 but may be used for verifying data transfer.

Figure 13. SPI/QSPI Connection

daisy-chaining devices

DACs can be daisy-chained by connecting the DOUT terminal of one device to the DIN of the next device in the chain, providing that the setup time, $t_{su(CSS)}$, ($\overline{CS}$ low to SCLK high) is greater than the sum of the setup time, $t_{su(DS)}$, plus the propagation delay time, $t_{pd(DOUT)}$, for proper timing (see digital input timing requirements section). The data at DIN appears at DOUT, delayed by 16 clock cycles plus one clock width. DOUT is a totem-poled output for low power. DOUT changes on the SCLK falling edge when $\overline{CS}$ is low. When $\overline{CS}$ is high, DOUT remains at the value of the last data bit and does not go into a high-impedance state.

linearity, offset, and gain error using single ended supplies

When an amplifier is operated from a single supply, the voltage offset can still be either positive or negative. With a positive offset, the output voltage changes on the first code change. With a negative offset the output voltage may not change with the first code depending on the magnitude of the offset voltage.

The output amplifier attempts to drive the output to a negative voltage. However, because the most negative supply rail is ground, the output cannot drive below ground and clamps the output at 0 V.

The output voltage then remains at zero until the input code value produces a sufficient positive output voltage to overcome the negative offset voltage, resulting in the transfer function shown in Figure 14.

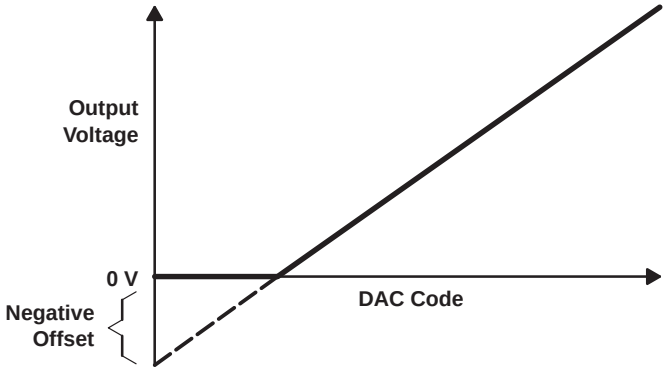


Figure 14. Effect of Negative Offset (Single Supply)

APPLICATION INFORMATION

linearity, offset, and gain error using single ended supplies (continued)

This offset error, not the linearity error, produces this breakpoint. The transfer function would have followed the dotted line if the output buffer could drive below the ground rail.

For a DAC, linearity is measured between zero-input code (all inputs 0) and full-scale code (all inputs 1) after offset and full scale are adjusted out or accounted for in some way. However, single supply operation does not allow for adjustment when the offset is negative due to the breakpoint in the transfer function. So the linearity is measured between full-scale code and the lowest code that produces a positive output voltage. For the TLC5615, the zero-scale (offset) error is plus or minus 3 LSB maximum. The code is calculated from the maximum specification for the negative offset.

power-supply bypassing and ground management

Printed-circuit boards that use separate analog and digital ground planes offer the best system performance. Wire-wrap boards do not perform well and should not be used. The two ground planes should be connected together at the low-impedance power-supply source. The best ground connection may be achieved by connecting the DAC AGND terminal to the system analog ground plane making sure that analog ground currents are well managed and there are negligible voltage drops across the ground plane.

A 0.1-μF ceramic-capacitor bypass should be connected between V_{DD} and AGND and mounted with short leads as close as possible to the device. Use of ferrite beads may further isolate the system analog supply from the digital power supply.

Figure 15 shows the ground plane layout and bypassing technique.

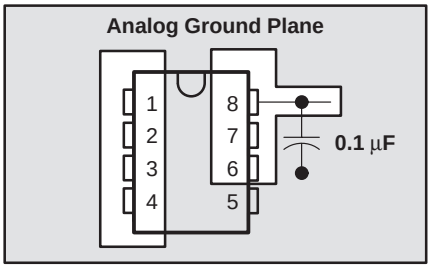


Figure 15. Power-Supply Bypassing

saving power

Setting the DAC register to all 0s minimizes power consumption by the reference resistor array and the output load when the system is not using the DAC.

ac considerations

digital feedthrough

Even with $\overline{CS}$ high, high-speed serial data at any of the digital input or output terminals may couple through the DAC package internal stray capacitance and appear at the DAC analog output as digital feedthrough. Digital feedthrough is tested by holding $\overline{CS}$ high and transmitting 0101010101 from DIN to DOUT.

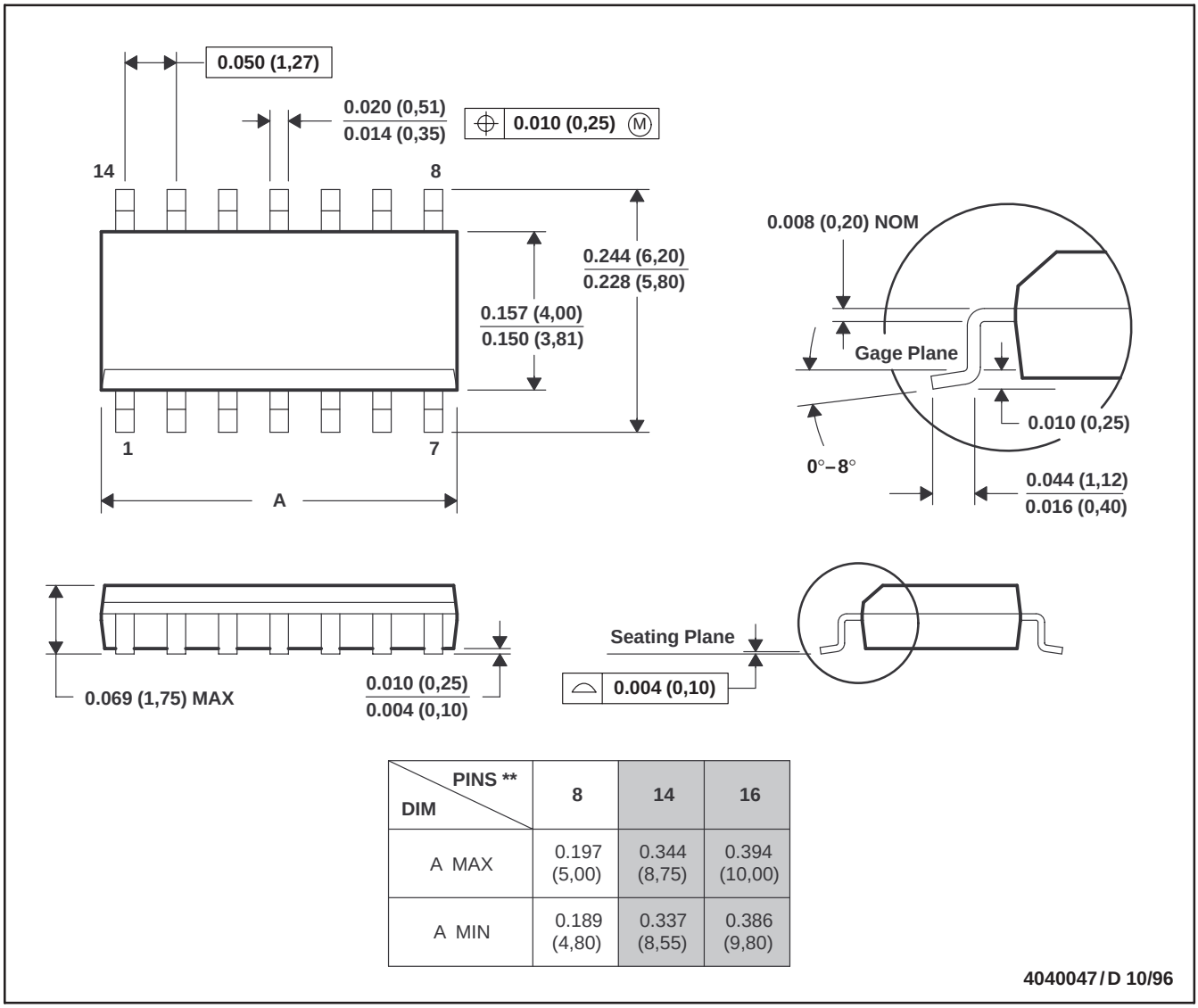
analog feedthrough

Higher frequency analog input signals may couple to the output through internal stray capacitance. Analog feedthrough is tested by holding $\overline{CS}$ high, setting the DAC code to all 0s, sweeping the frequency applied to REFIN, and monitoring the DAC output.

MECHANICAL DATA

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



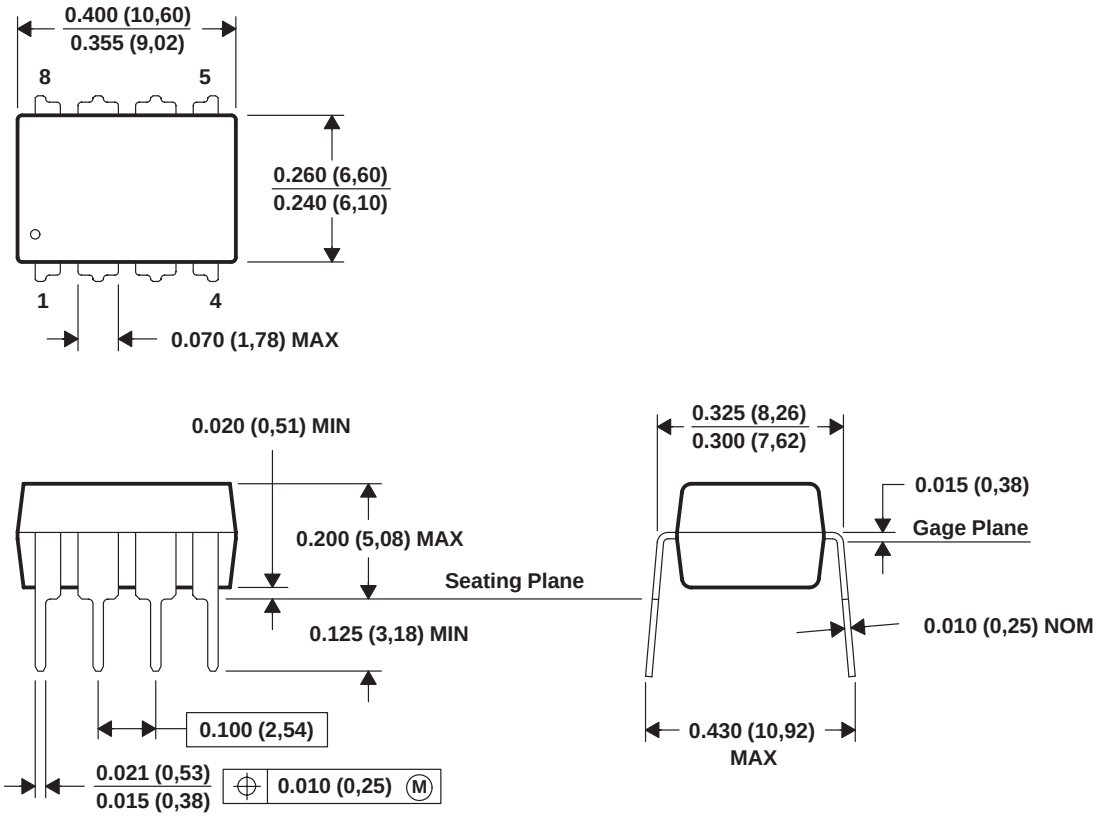
DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047/D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

MECHANICAL DATA

P (R-PDIP-T8) **PLASTIC DUAL-IN-LINE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

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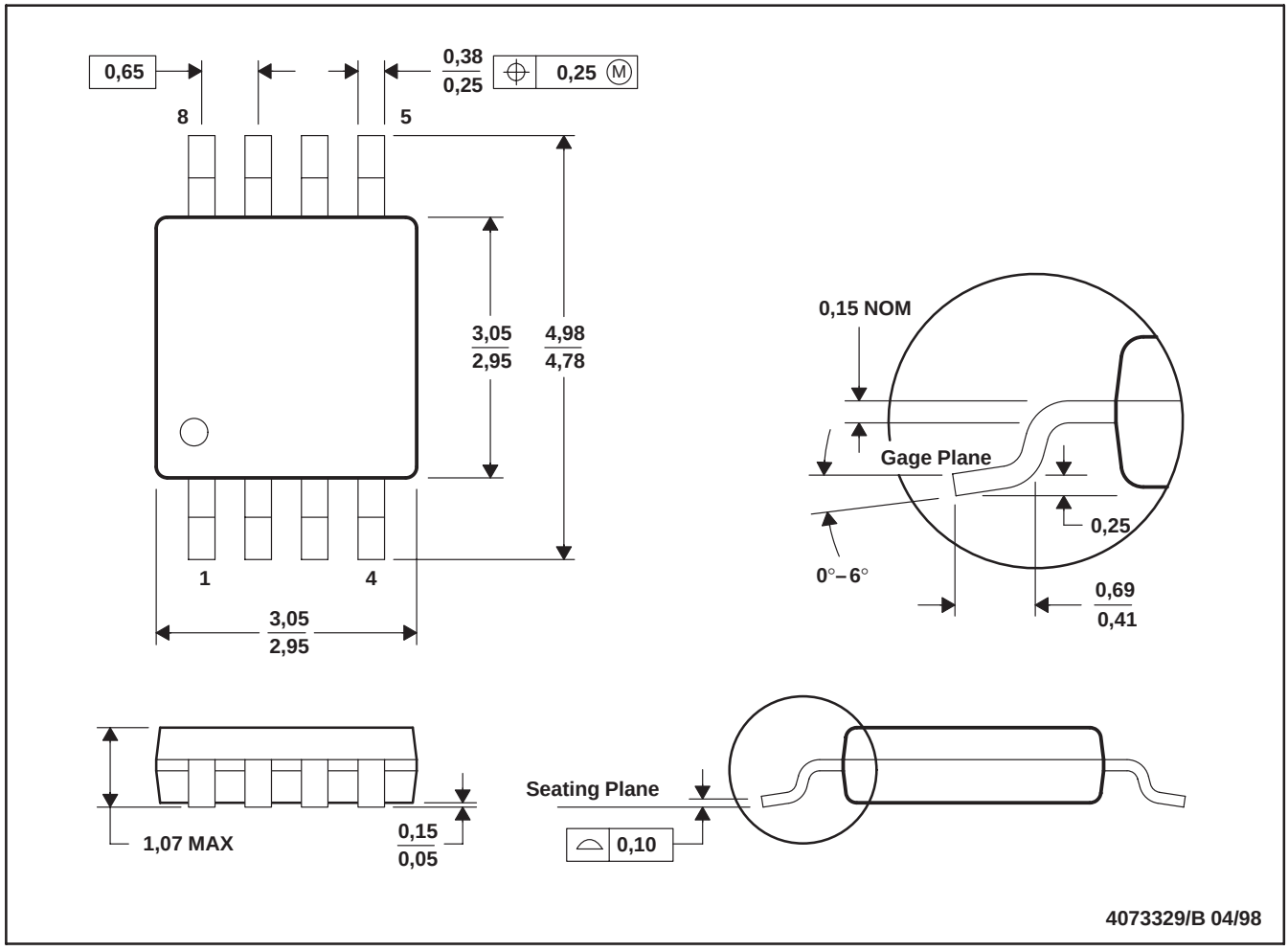
MPDI001A – JANUARY 1995 – REVISED JUNE 1999

MECHANICAL DATA

DGK (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-187

For the latest package information, go to http://www.ti.com/sc/docs/package/pkg_info.htm

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