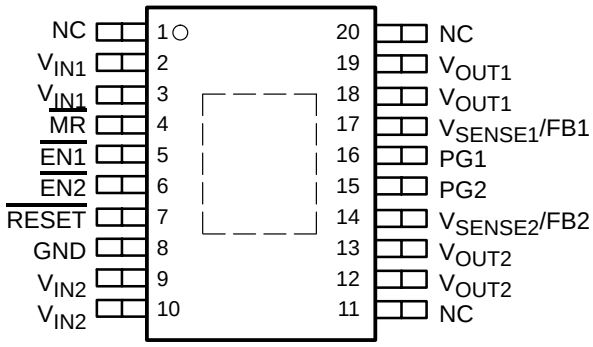
- **Dual Output Voltages for Split-Supply Applications**
- **Independent Enable Functions (See Part Number TPS701xx for Sequenced Outputs)**
- **Output Current Range of 500 mA on Regulator 1 and 250 mA on Regulator 2**
- **Fast Transient Response**
- **Voltage Options Are 3.3-V/2.5-V, 3.3-V/1.8-V, 3.3-V/1.5-V, 3.3-V/1.2-V, and Dual Adjustable Outputs**
- **Open Drain Power-On Reset With 120-ms Delay**
- **Open Drain Power Good for Regulator 1 and Regulator 2**
- **Ultralow 190 μA (typ) Quiescent Current**
- **1 μA Input Current During Standby**
- **Low Noise: 65 $\mu V_{RMS}$ Without Bypass Capacitor**
- **Quick Output Capacitor Discharge Feature**
- **One Manual Reset Input**
- **2% Accuracy Over Load and Temperature**
- **Undervoltage Lockout (UVLO) Feature**
- **20-Pin PowerPAD™ TSSOP Package**
- **Thermal Shutdown Protection**

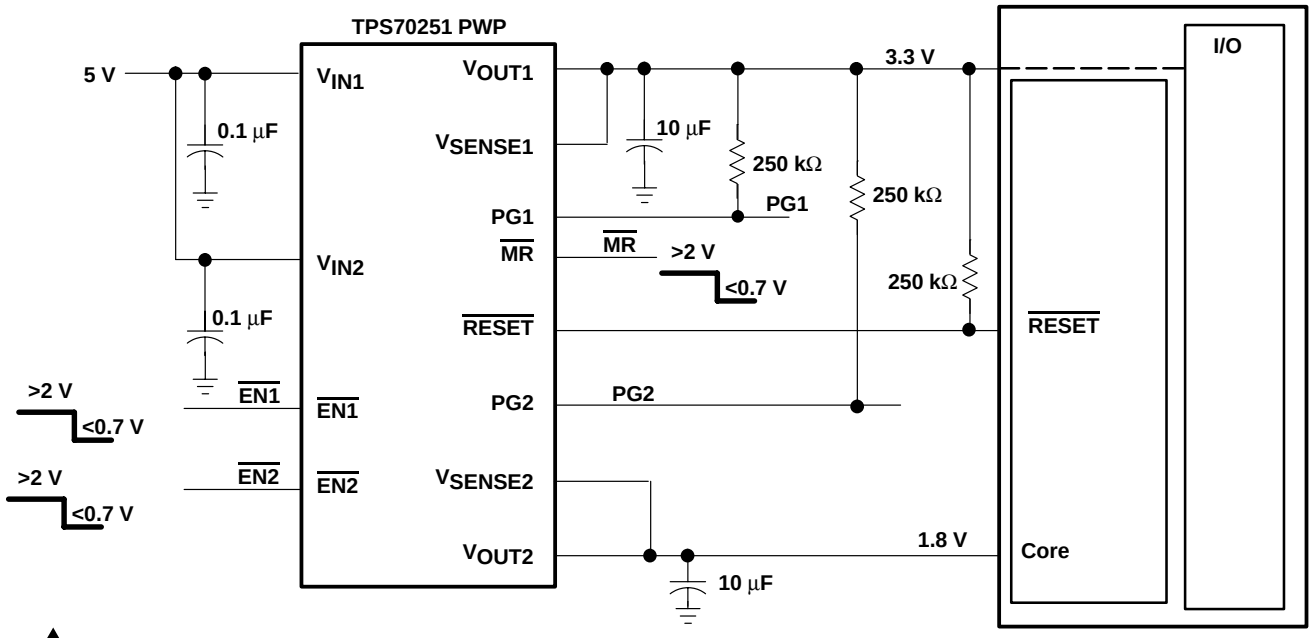
## description

The TPS702xx is a low dropout voltage regulator with integrated SVS ($\overline{\text{RESET}}$, POR, or power on reset) and power good (PG) functions. These devices are capable of supplying 500 mA and 250 mA by regulator 1 and regulator 2 respectively. Quiescent current is typically 190 μA at full load. Differentiated features, such as accuracy, fast transient response, SVS supervisory circuit (power on reset), manual reset input, and independent enable functions provide a complete system solution.

**PWP PACKAGE**
**(TOP VIEW)**




NC – No internal connection

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## description (continued)

The TPS702xx family of voltage regulators offers very low dropout voltage and dual outputs. These devices have extremely low noise output performance without using any added filter bypass capacitors and are designed to have a fast transient response and be stable with 10 μF low ESR capacitors.

These devices have fixed 3.3-V/2.5-V, 3.3-V/1.8-V, 3.3-V/1.5-V, 3.3-V/1.2-V, and adjustable voltage options. Regulator 1 can support up to 500 mA, and regulator 2 can support up to 250 mA. Separate voltage inputs allow the designer to configure the source power.

Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low (typically 170 mV on regulator 1) and is directly proportional to the output current. Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is very low and independent of output loading (maximum of 230 μA over the full range of output current and full range of temperature). This LDO family also features a sleep mode; applying a high signal to $\overline{EN1}$ or $\overline{EN2}$ (enable) shuts down regulator 1 or regulator 2, respectively. When a high signal is applied to both $\overline{EN1}$ and $\overline{EN2}$, both regulators are in sleep mode, thereby reducing the input current to 2 μA at $T_J$ = 25°C.

For each regulator, there is an internal discharge transistor to discharge the output capacitor when the regulator is turned off (disabled).

The PG1 pin reports the voltage condition at $V_{OUT1}$. The PG1 pin can be used to implement a SVS ($\overline{RESET}$, POR, or power on reset) for the circuitry supplied by regulator 1. The PG2 pin reports the voltage conditions at $V_{OUT2}$. The PG2 pin can be used to implement a SVS (power on reset) for the circuitry supplied by regulator 2.

The TPS702xx features a $\overline{RESET}$ (SVS, POR, or power on reset). $\overline{RESET}$ output initiates a reset in the event of an undervoltage condition. $\overline{RESET}$ also indicates the status of the manual reset pin ($\overline{MR}$). When $\overline{MR}$ is in the logic high state, $\overline{RESET}$ goes to a high impedance state after 120 ms delay. To monitor $V_{OUT1}$, the PG1 output pin can be connected to $\overline{MR}$. To monitor $V_{OUT2}$, the PG2 output pin can be connected to $\overline{MR}$.

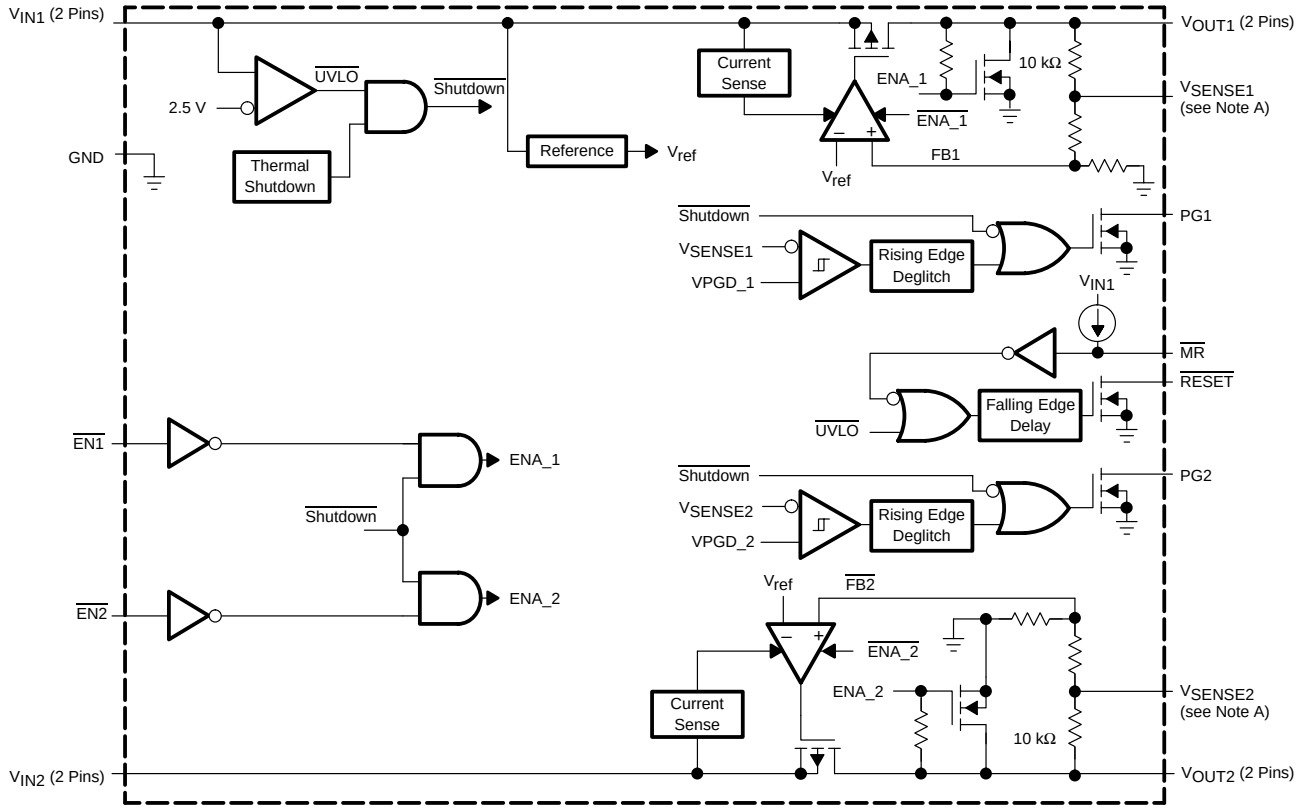
The device has an undervoltage lockout UVLO circuit which prevents the internal regulators from turning on until $V_{IN1}$ reaches 2.5V.

**AVAILABLE OPTIONS**

| $T_J$ | REGULATOR 1 $V_O$ (V) | REGULATOR 2 $V_O$ (V) | TSSOP (PWP) |
|---|---|---|---|
| –40°C to 125°C | 3.3 V | 1.2 V | TPS70245PWP |
| | 3.3 V | 1.5 V | TPS70248PWP |
| | 3.3 V | 1.8 V | TPS70251PWP |
| | 3.3 V | 2.5 V | TPS70258PWP |
| | Adjustable (1.22 V to 5.5 V) | Adjustable (1.22 V to 5.5 V) | TPS70202PWP |

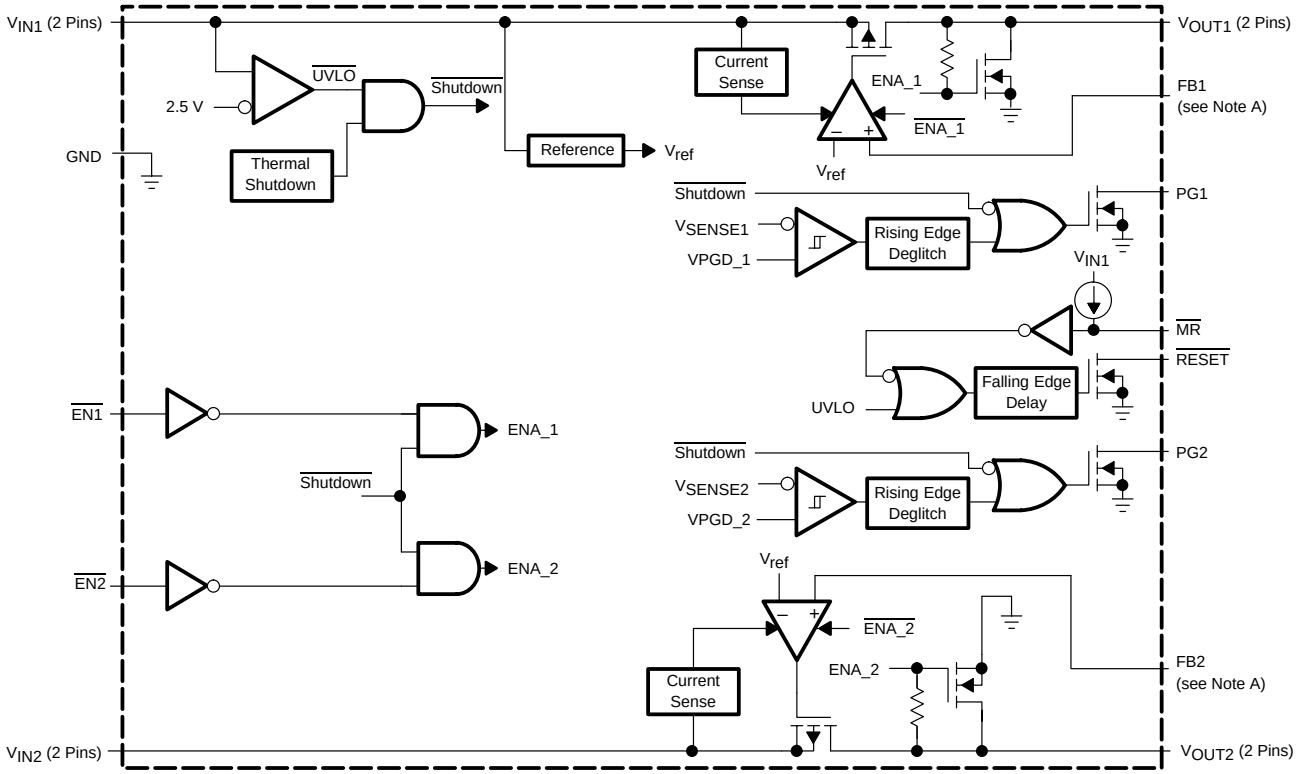
NOTE: The TPS70202 is programmable using external resistor dividers (see application information) The PWP package is available taped and reeled. Add an R suffix to the device type (e.g., TPS70202PWPR).

## detailed block diagram – fixed voltage version



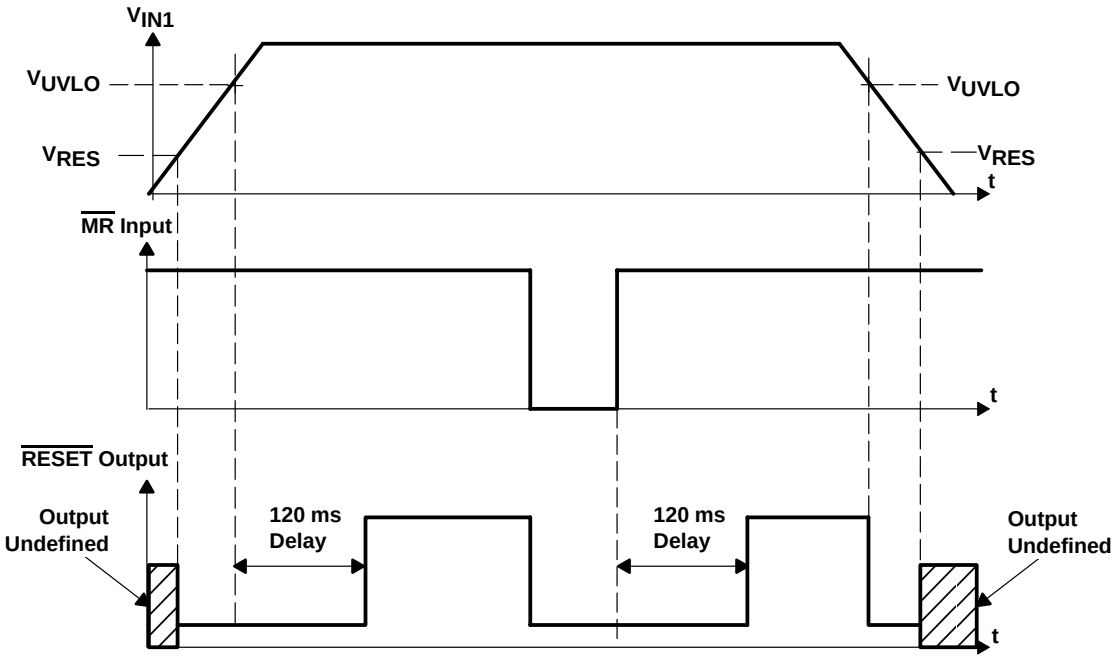

NOTE A: For most applications, $V_{SENSE1}$ and $V_{SENSE2}$ should be externally connected to $V_{OUT1}$ and $V_{OUT2}$ respectively as close as possible to the device. For other implementations, refer to SENSE terminal connection discussion in the application information section.

## detailed block diagram – adjustable voltage version



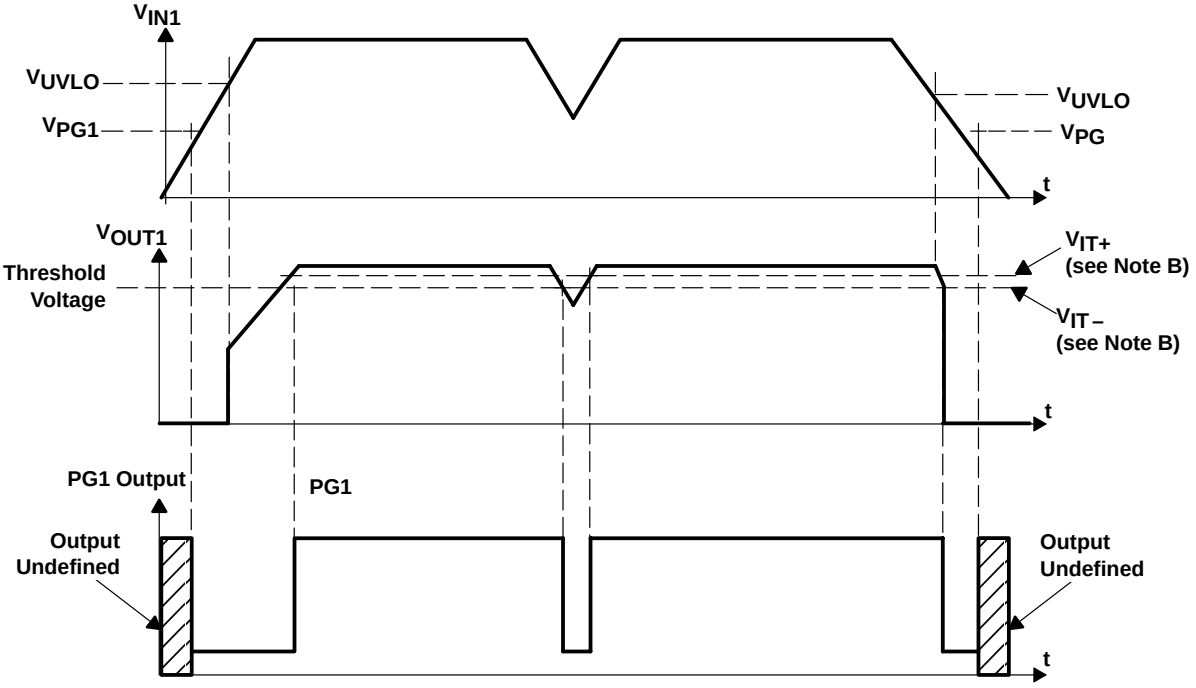

NOTE A: For most applications, FB1 and FB2 should be externally connected to resistor dividers as close as possible to the device. For other implementations, refer to FB terminals connection discussion in the application information section.

## $\overline{\text{RESET}}$ timing diagram




NOTE A: $V_{RES}$ is the minimum input voltage for a valid $\overline{\text{RESET}}$. The symbol $V_{RES}$ is not currently listed within EIA or JEDEC standards for semiconductor symbology.

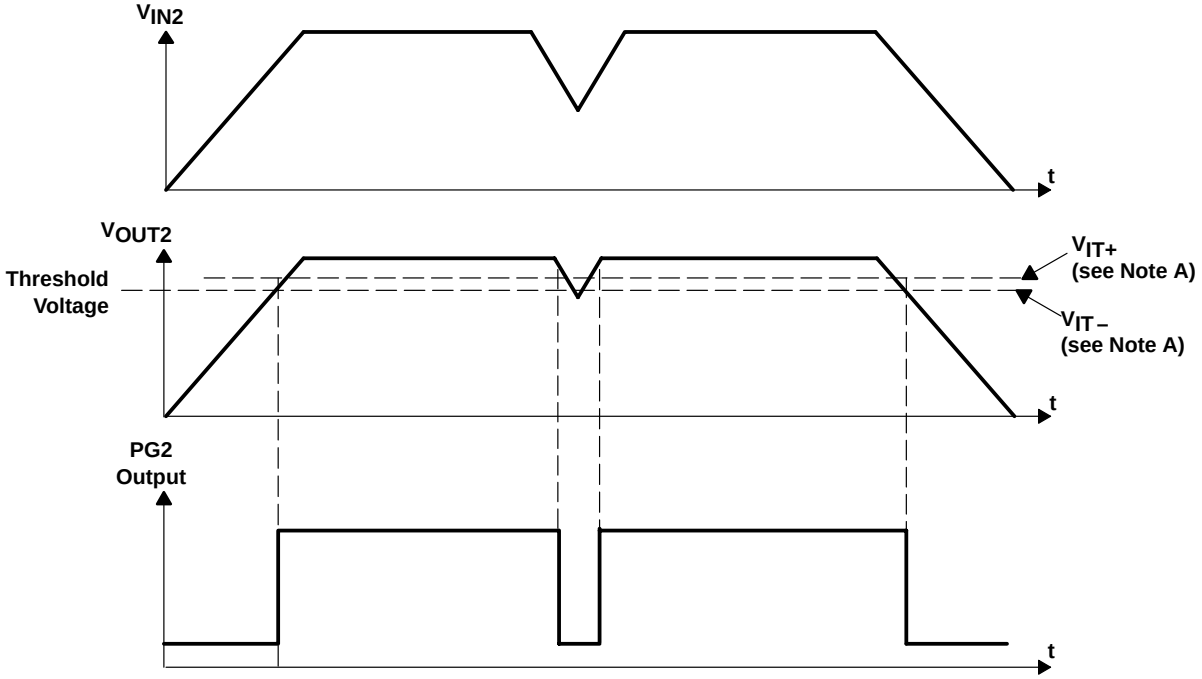
## PG1 timing diagram




NOTES: A. $V_{PG1}$ is the minimum input voltage for a valid PG1. The symbol $V_{PG1}$ is not currently listed within EIA or JEDEC standards for semiconductor symbology.

B. VIT –Trip voltage is typically 5% lower than the output voltage (95%$V_O$) $V_{IT-}$ to $V_{IT+}$ is the hysteresis voltage.

### PG2 timing diagram (assuming $V_{IN1}$ already powered up)




NOTE A: VIT –Trip voltage is typically 5% lower than the output voltage (95%$V_O$) $V_{IT-}$ to $V_{IT+}$ is the hysteresis voltage.

## Terminal Functions

| TERMINAL NAME | TERMINAL NO. | I/O | DESCRIPTION |
|---|---|---|---|
| $\overline{EN1}$ | 5 | I | Active low enable for $V_{OUT1}$ |
| $\overline{EN2}$ | 6 | I | Active low enable for $V_{OUT2}$ |
| GND | 8 | | Ground |
| $\overline{MR}$ | 4 | I | Manual reset input, active low, pulled up internally |
| NC | 1, 11, 20 | | No connection |
| PG1 | 16 | O | Open drain output, low when $V_{OUT1}$ voltage is less than 95% of the nominal regulated voltage |
| PG2 | 15 | O | Open drain output, low when $V_{OUT2}$ voltage is less than 95% of the nominal regulated voltage |
| $\overline{RESET}$ | 7 | I | Open drain output, SVS (power on reset) signal, active low |
| $V_{IN1}$ | 2, 3 | I | Input voltage of regulator 1 |
| $V_{IN2}$ | 9, 10 | I | Input voltage of regulator 2 |
| $V_{OUT1}$ | 18, 19 | O | Output voltage of regulator 1 |
| $V_{OUT2}$ | 12, 13 | O | Output voltage of regulator 2 |
| $V_{SENSE2}$/FB2 | 14 | I | Regulator 2 output voltage sense/ regulator 2 feedback for adjustable |
| $V_{SENSE1}$/FB1 | 17 | I | Regulator 1 output voltage sense/ regulator 1 feedback for adjustable |

## detailed description

The TPS702xx low dropout regulator family provides dual regulated output voltages with independent enable functions. These devices provide fast transient response and high accuracy with small output capacitors, while drawing low quiescent current. Other features are integrated SVS (power-on reset, $\overline{\text{RESET}}$) and power good (PG1, PG2) that monitor output voltages and provide logic output to the system. These differentiated features provide a complete power solution.

The TPS702xx, unlike many other LDOs, features very low quiescent current which remains virtually constant even with varying loads. Conventional LDO regulators use a pnp pass element, the base current of which is directly proportional to the load current through the regulator ($I_B = I_C/\beta$). The TPS702xx uses a PMOS transistor to pass current; because the gate of the PMOS is voltage driven, operating current is low and stable over the full load range.

## pin functions

### enable ($\overline{\text{EN1}}$ and $\overline{\text{EN2}}$)

The $\overline{\text{EN}}$ terminals are inputs which enable or shut down each respective regulator. If $\overline{\text{EN}}$ is at a voltage high signal the respective regulator is in shutdown mode. When $\overline{\text{EN}}$ goes to voltage low, then the respective regulator is enabled.

### power good (PG1 and PG2)

The PG terminals are open drain, active high outputs which indicate the status of each respective regulator. When the $V_{OUT1}$ reaches 95% of its regulated voltage, PG1 will go to a high impedance state. When the $V_{OUT2}$ reaches 95% of its regulated voltage, PG2 will go to a high impedance state. Each PG will go to a low impedance state when its respective output voltage is pulled below 95% (i.e., over load condition) of its regulated voltage. The open drain outputs of the PG terminals require a pullup resistor.

### manual reset pin ($\overline{\text{MR}}$)

$\overline{\text{MR}}$ is an active low input terminal used to trigger a reset condition. When $\overline{\text{MR}}$ is pulled to logic low, a POR ($\overline{\text{RESET}}$) occurs. The terminal has a 6-μA pullup current to $V_{IN1}$.

### sense ($V_{SENSE1}$, $V_{SENSE2}$)

The sense terminals of fixed-output options must be connected to the regulator outputs, and the connection should be as short as possible. Internally, the sense terminal connects to high-impedance wide-bandwidth amplifiers through a resistor-divider network and noise pickup feeds through to the regulator output. It is essential to route the sense connection in such a way as to minimize/avoid noise pickup. Adding RC networks between sense terminals and $V_{OUTS}$ to filter noise is not recommended because it can cause the regulators to oscillate.

### FB1 and FB2

FB1 and FB2 are input terminals used for adjustable-output devices and must be connected to the external feedback resistor divider. FB1 and FB2 connections should be as short as possible. It is essential to route them in such a way as to minimize/avoid noise pickup. Adding RC networks between FB terminals and $V_{OUTS}$ to filter noise is not recommended because it can cause the regulators to oscillate.

### $\overline{\text{RESET}}$ indicator

The TPS702xx features a $\overline{\text{RESET}}$ (SVS, POR, or power on reset). $\overline{\text{RESET}}$ can be used to drive power on reset circuitry or a low-battery indicator. $\overline{\text{RESET}}$ is an active low, open drain output which indicates the status of the manual reset pin ($\overline{\text{MR}}$). When $\overline{\text{MR}}$ is in high impedance state, $\overline{\text{RESET}}$ goes to a high impedance state after a 120 ms delay. To monitor $V_{OUT1}$, the PG1 output pin can be connected to $\overline{\text{MR}}$. To monitor $V_{OUT2}$, the PG2 output pin can be connected to $\overline{\text{MR}}$. The open drain output of the $\overline{\text{RESET}}$ terminal requires a pullup resistor. If $\overline{\text{RESET}}$ is not used, it can be left floating.

## detailed description (continued)

### $V_{IN1}$ and $V_{IN2}$

$V_{IN1}$ and $V_{IN2}$ are inputs to each regulator. Internal bias voltages are powered by $V_{IN1}$.

### $V_{OUT1}$ and $V_{OUT2}$

$V_{OUT1}$ and $V_{OUT2}$ are output terminals of each regulator.

## absolute maximum ratings over operating junction temperature (unless otherwise noted)†

Input voltage range‡: $V_{IN1}$ . . . . . –0.3 V to 7 V
$V_{IN2}$ . . . . . –0.3 V to 7 V
Voltage range at $\overline{EN1}$, $\overline{EN2}$ . . . . . –0.3 V to 7 V
Output voltage range ($V_{OUT1}$, $V_{SENSE1}$) . . . . . 5.5 V
Output voltage range ($V_{OUT2}$, $V_{SENSE2}$) . . . . . 5.5 V
Maximum $\overline{RESET}$, PG1, PG2 voltage . . . . . 7 V
Maximum $\overline{MR}$ voltage . . . . . $V_{IN1}$
Peak output current . . . . . Internally limited
Continuous total power dissipation . . . . . See Dissipation Rating Tables
Operating virtual junction temperature range, $T_J$ . . . . . –40°C to 150°C
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C
ESD rating, HBM . . . . . 2 kV

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ All voltages are tied to network ground.

**DISSIPATION RATING TABLE**

| PACKAGE | AIR FLOW (CFM) | $T_A \le 25°C$ | DERATING FACTOR | $T_A = 70°C$ | $T_A = 85°C$ |
|---|---|---|---|---|---|
| PWP§ | 0 | 3.067 W | 30.67 mW/°C | 1.687 W | 1.227 W |
| | 250 | 4.115 W | 41.15 mW/°C | 2.265 W | 1.646 W |

§ This parameter is measured with the recommended copper heat sink pattern on a 4-layer PCB, 1 oz. copper on 4-in × 4-in ground layer. For more information, refer to TI technical brief SLMA002.

## recommended operating conditions

| | MIN | MAX | UNIT |
|---|---|---|---|
| Input voltage, $V_I$¶ | 2.7 | 6 | V |
| Output current, $I_O$ (regulator 1) | 0 | 500 | mA |
| Output current, $I_O$ (regulator 2) | 0 | 250 | mA |
| Output voltage range (for adjustable option) | 1.22 | 5.5 | V |
| Operating virtual junction temperature, $T_J$ | –40 | 125 | °C |

¶ To calculate the minimum input voltage for maximum output current, use the following equation: $V_{I(min)} = V_{O(max)} + V_{DO(max\ load)}$.

## electrical characteristics over recommended operating junction temperature ($T_J$ = –40°C to 125°C) $V_{IN1}$ or $V_{IN2}$= $V_{O(nom)}$ + 1 V, $I_O$ = 1 mA, $\overline{EN1}$ = 0, $\overline{EN2}$ = 0, $C_O$ = 33 μF(unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_O$ Output voltage (see Notes 1 and 3) | Reference voltage | 2.7 V < $V_{IN}$ < 6 V, $T_J$ = 25°C | FB connected to $V_O$ | | 1.22 | | V |
| | | 2.7 V < $V_{IN}$ < 6 V, | FB connected to $V_O$ | 1.196 | | 1.244 | |
| | 1.2 V output | 2.7 V < $V_I$ < 6 V, | $T_J$ = 25°C | | 1.2 | | |
| | | 2.7 V < $V_I$ < 6 V | | 1.176 | | 1.224 | |
| | 1.5 V output | 2.7 V < $V_I$ < 6 V, | $T_J$ = 25°C | | 1.5 | | |
| | | 2.7 V < $V_I$ < 6 V | | 1.47 | | 1.53 | |
| | 1.8 V output | 2.8 V < $V_I$ < 6 V, | $T_J$ = 25°C | | 1.8 | | |
| | | 2.8 V < $V_I$ < 6 V | | 1.764 | | 1.836 | |
| | 2.5 V output | 3.5 V < $V_I$ < 6 V, | $T_J$ = 25°C | | 2.5 | | |
| | | 3.5 V < $V_I$ < 6 V | | 2.45 | | 2.55 | |
| | 3.3 V output | 4.3 V < $V_I$ < 6 V, | $T_J$ = 25°C | | 3.3 | | V |
| | | 4.3 V < $V_I$ < 6 V | | 3.234 | | 3.366 | |
| Quiescent current (GND current) for regulator 1 and regulator 2, $\overline{EN1}$ = $\overline{EN2}$ = 0 V, (see Note 1) | | See Note 3, | $T_J$ = 25°C | | 190 | | μA |
| | | See Note 3 | | | | 230 | |
| Output voltage line regulation ($\Delta V_O/V_O$) for regulator 1 and regulator 2 (see Note 2) | | $V_O$ + 1 V < $V_I$ ≤ 6 V, | $T_J$ = 25°C, See Note 1 | | 0.01% | | V |
| | | $V_O$ + 1 V < $V_I$ ≤ 6 V, | See Note 1 | | | 0.1% | |
| Load regulation for $V_{OUT1}$ and $V_{OUT2}$ | | $T_J$ = 25°C | | | 1 | | mV |
| $V_n$ Output noise voltage | Regulator 1 | BW = 300 Hz to 50 kHz, $C_O$ = 33 μF, $T_J$ = 25°C | | | 65 | | μVrms |
| | Regulator 2 | | | | 65 | | |
| Output current limit | Regulator 1 | $V_O$ = 0 V | | | 1.6 | 1.9 | A |
| | Regulator 2 | | | | 0.750 | 1 | |
| Thermal shutdown junction temperature | | | | | 150 | | °C |
| $I_{I(standby)}$ Standby current | Regulator 1 and Regulator 2 | $\overline{EN1}$ = $V_I$, $\overline{EN2}$ = $V_I$, | $T_J$ = 25°C | | | 2 | μA |
| | | $\overline{EN1}$ = $V_I$, $\overline{EN2}$ = $V_I$ | | | | 6 | |
| PSRR Power supply ripple rejection | Regulator 1 | f = 1 kHz, $C_O$ = 33 μF, $I_{OUT1}$ = 500 mA | $T_J$ = 25°C, See Note 1 | | 60 | | dB |
| | Regulator 2 | f = 1 kHz, $C_O$ = 33 μF, $I_{OUT2}$ = 250 mA | $T_J$ = 25°C, See Note 1 | | 50 | | |
| UVLO threshold | | | | 2.4 | | 2.65 | V |

NOTES: 1. Minimum input operating voltage is 2.7 V or $V_{O(typ)}$ + 1 V, whichever is greater. Maximum input voltage = 6 V, minimum output current 1 mA.

2. If $V_O$ < 1.8 V then $V_{Imax}$ = 6 V, $V_{Imin}$ = 2.7 V:

$$\text{Line regulation (mV)} = (\%/V) \times \frac{V_O\left(V_{Imax} - 2.7\ V\right)}{100} \times 1000$$

If $V_O$ > 2.5 V then $V_{Imax}$ = 6 V, $V_{Imin}$ = Vo + 1 V:

$$\text{Line regulation (mV)} = (\%/V) \times \frac{V_O\left(V_{Imax} - \left(V_O + 1\right)\right)}{100} \times 1000$$

3. $I_O$ = 1 mA to 500 mA for regulator 1 and 1 mA to 250 mA for regulator 2.

## electrical characteristics over recommended operating junction temperature ($T_J$ = –40°C to 125°C) $V_{IN1}$ or $V_{IN2}$= $V_{O(nom)}$ + 1 V, $I_O$ = 1 mA, $\overline{EN1}$ = 0, $\overline{EN2}$ = 0, $C_O$ = 33 μF(unless otherwise noted) (continued)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **RESET terminal** | | | | | |
| Minimum input voltage for valid $\overline{RESET}$ | $I_{(RESET)}$ = 300 μA, $V_{(RESET)} \le$ 0.8 V | | 1.0 | 1.3 | V |
| $t_{(RESET)}$ | $\overline{RESET}$ pulse duration | 80 | 120 | 160 | ms |
| Output low voltage | $V_I$ = 3.5 V, $I_{(RESET)}$ = 1 mA | | 0.15 | 0.4 | V |
| Leakage current | $V_{(RESET)}$ = 6 V | | | 1 | μA |
| **PG1/PG2 terminal** | | | | | |
| Minimum input voltage for valid PGx | $I_{(PGx)}$ = 300 μA, $V_{(PGx)} \le$ 0.8 V | | 1.0 | 1.3 | V |
| Trip threshold voltage | $V_O$ decreasing | 92% | 95% | 98% | $V_O$ |
| Hysteresis voltage | Measured at $V_O$ | | 0.5% | | $V_O$ |
| $t_{r(PGx)}$ | Rising edge deglitch | | 30 | | μs |
| Output low voltage | $V_I$ = 2.7 V, $I_{(PGx)}$ = 1 mA | | 0.15 | 0.4 | V |
| Leakage current | $V_{(PGx)}$ = 6 V | | | 1 | μA |
| **EN1/EN2 terminal** | | | | | |
| High-level $\overline{ENx}$ input voltage | | 2 | | | V |
| Low-level $\overline{ENx}$ input voltage | | | | 0.7 | V |
| Input current ($\overline{ENx}$) | | –1 | | 1 | μA |
| **MR terminal** | | | | | |
| High-level input voltage | | 2 | | | V |
| Low-level input voltage | | | | 0.7 | V |
| Pullup current source | | | 6 | | μA |
| **$V_{OUT1}$ terminal** | | | | | |
| Dropout voltage (see Note 4) | $I_O$ = 500 mA, $V_{IN1}$ = 3.2 V, $T_J$ = 25°C | | 170 | | mV |
| | $I_O$ = 500 mA, $V_{IN1}$ = 3.2 V | | | 275 | |
| Peak output current | 2 ms pulse width | | 750 | | mA |
| Discharge transistor current | $V_{OUT1}$ = 1.5 V | | 7.5 | | mA |
| **$V_{OUT2}$ terminal** | | | | | |
| Peak output current | 2 ms pulse width | | 375 | | mA |
| Discharge transistor current | $V_{OUT2}$ = 1.5 V | | 7.5 | | mA |
| **FB terminal** | | | | | |
| Input current – TPS70202 | FB = 1.8 V | | 1 | | μA |

NOTE 4: Input voltage($V_{IN1}$ or $V_{IN2}$) = $V_O$(Typ) – 100 mV. For the 1.5-V, 1.8-V and 2.5-V regulators, the dropout voltage is limited by input voltage range. The 3.3 V regulator input voltage is set to 3.2 V to perform this test.

## TYPICAL CHARACTERISTICS

### Table of Graphs

| | | | FIGURE |
|---|---|---|---|
| $V_O$ | Output voltage | vs Output current | 1 – 3 |
| | | vs Junction temperature | 4 – 5 |
| | Ground current | vs Junction temperature | 6 |
| PSRR | Power supply rejection ratio | vs Frequency | 7 – 10 |
| | Output spectral noise density | vs Frequency | 11 – 14 |
| $Z_O$ | Output impedance | vs Frequency | 15 – 18 |
| | Dropout voltage | vs Temperature | 19, 20 |
| | | vs Input voltage | 21, 22 |
| | Load transient response | | 23, 24 |
| | Line transient response ($V_{OUT1}$) | | 25 |
| | Line transient response ($V_{OUT2}$) | | 26 |
| $V_O$ | Output voltage | vs Time (start-up) | 27, 28 |
| | Equivalent series resistance (ESR) | vs Output current | 30 – 33 |

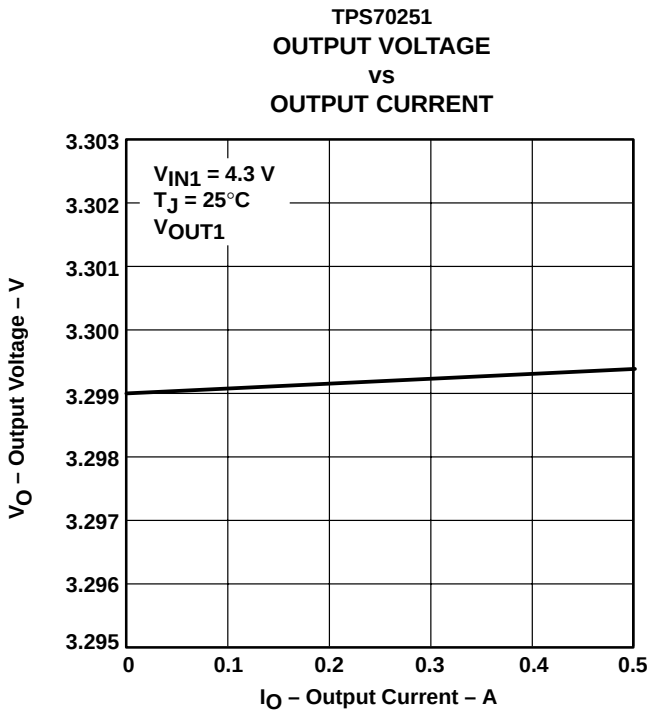



Figure 1

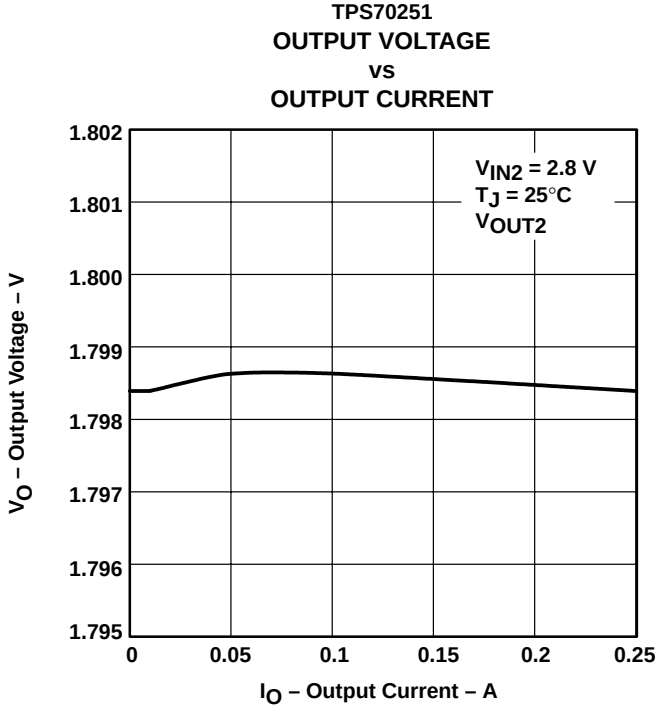



Figure 2

## TYPICAL CHARACTERISTICS

**TPS70245**
**OUTPUT VOLTAGE**
**vs**
**OUTPUT CURRENT**

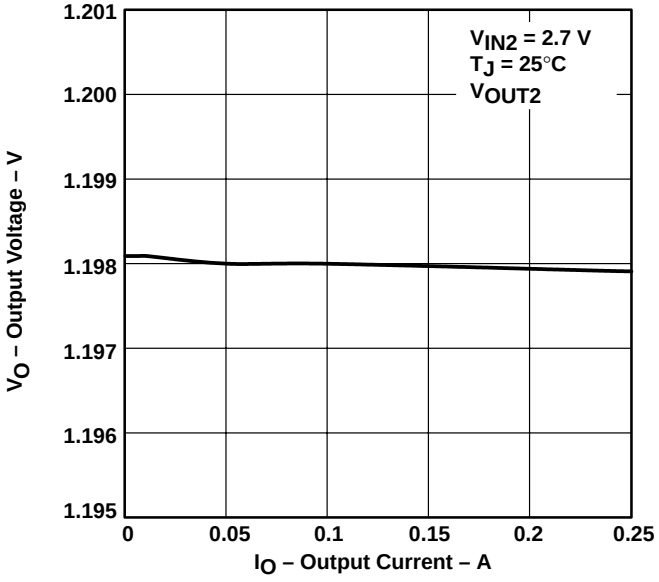



**Figure 3**

**TPS70251**
**OUTPUT VOLTAGE**
**vs**
**JUNCTION TEMPERATURE**

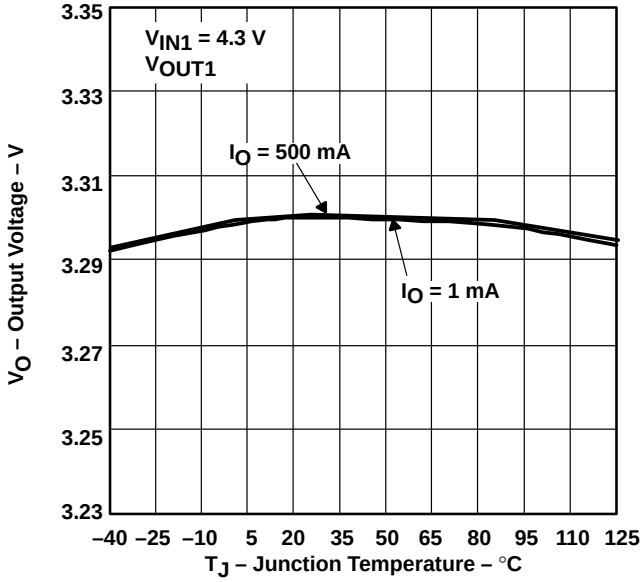



**Figure 4**

**TPS70251**
**OUTPUT VOLTAGE**
**vs**
**JUNCTION TEMPERATURE**

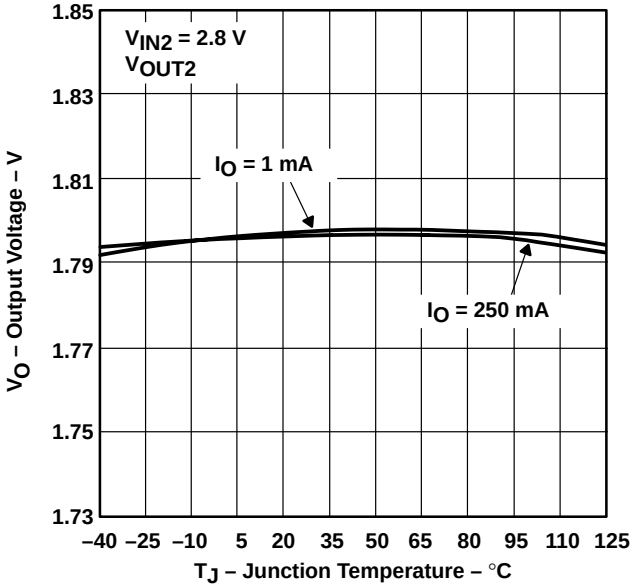



**Figure 5**

**GROUND CURRENT**
**vs**
**JUNCTION TEMPERATURE**

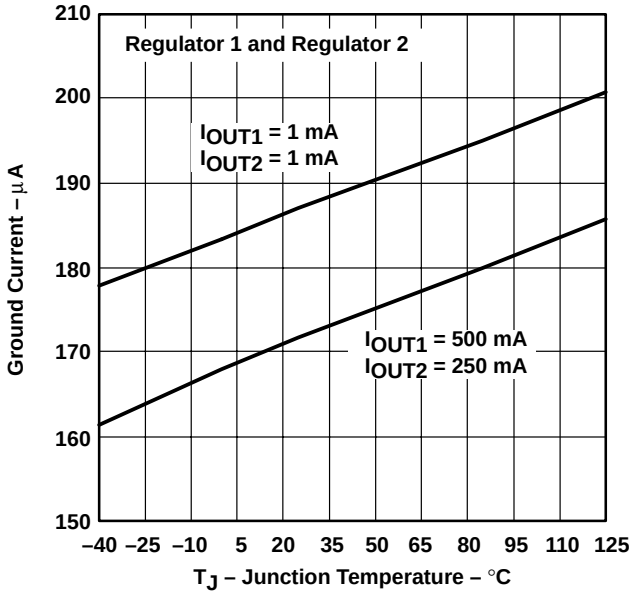



**Figure 6**

## TYPICAL CHARACTERISTICS

TPS70251
POWER SUPPLY REJECTION RATIO
vs
FREQUENCY

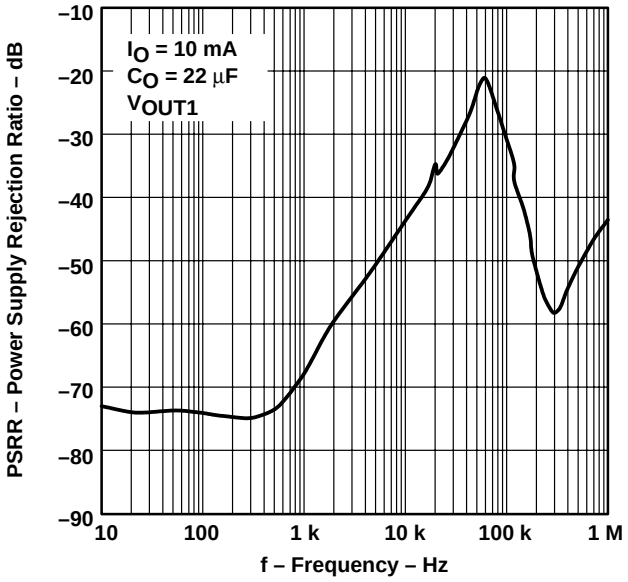



Figure 7

TPS70251
POWER SUPPLY REJECTION RATIO
vs
FREQUENCY

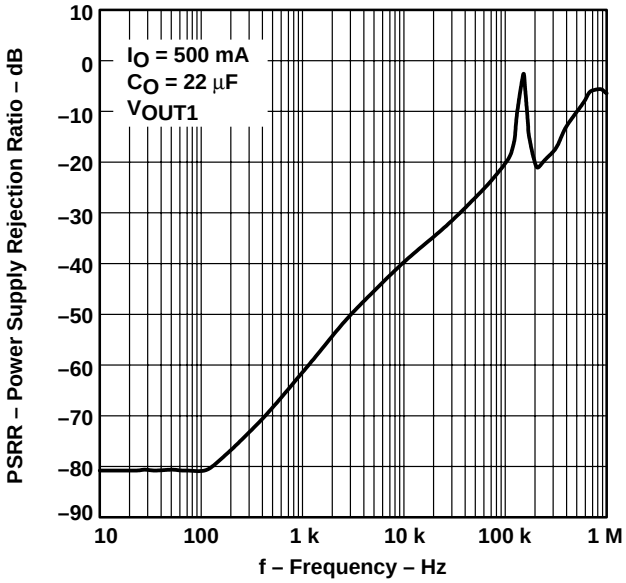



Figure 8

TPS70251
POWER SUPPLY REJECTION RATIO
vs
FREQUENCY

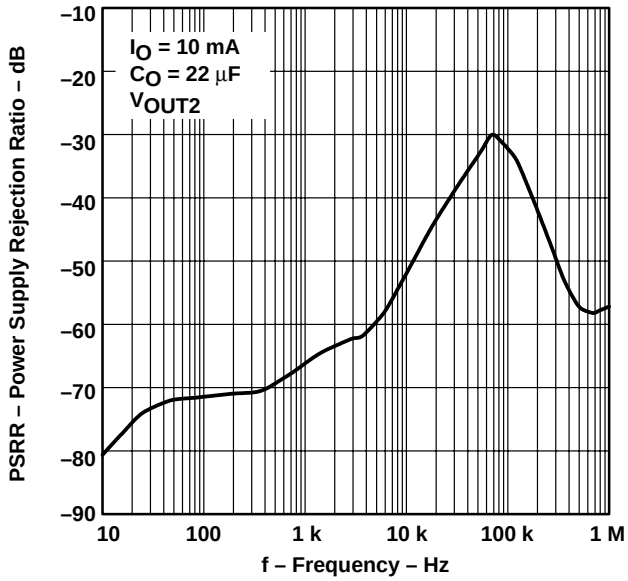



Figure 9

TPS70251
POWER SUPPLY REJECTION RATIO
vs
FREQUENCY

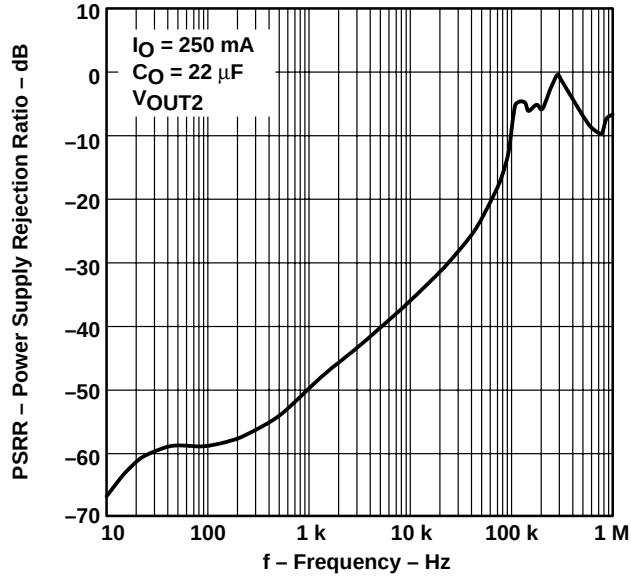



Figure 10

## TYPICAL CHARACTERISTICS

**OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY**

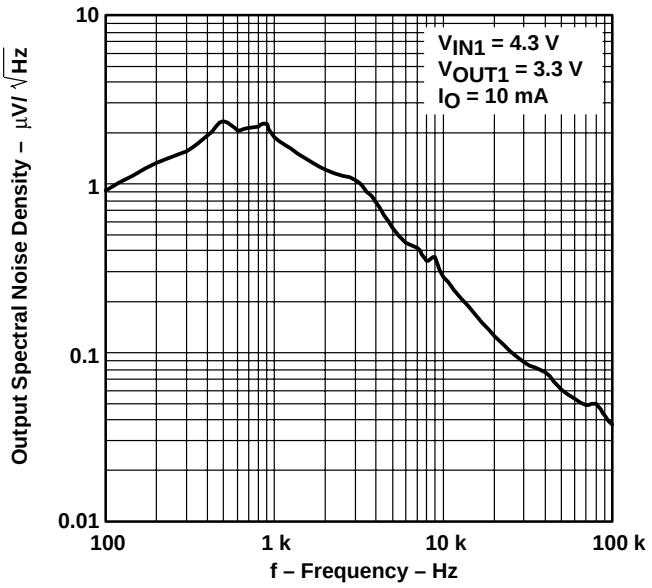



Figure 11

**OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY**

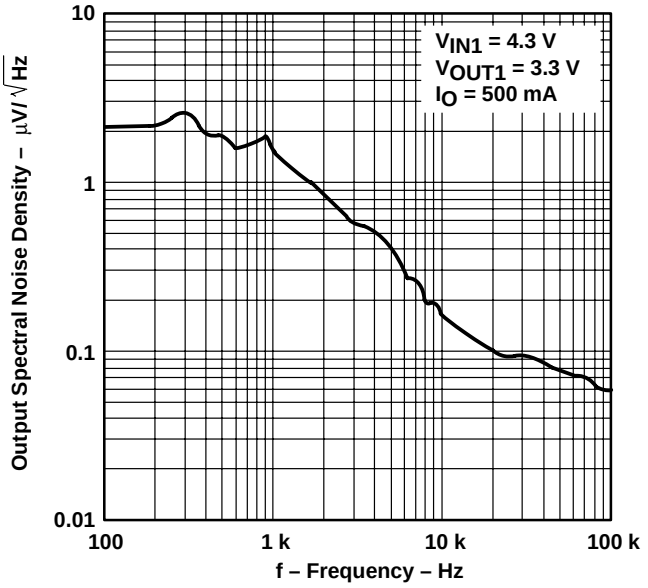



Figure 12

**OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY**

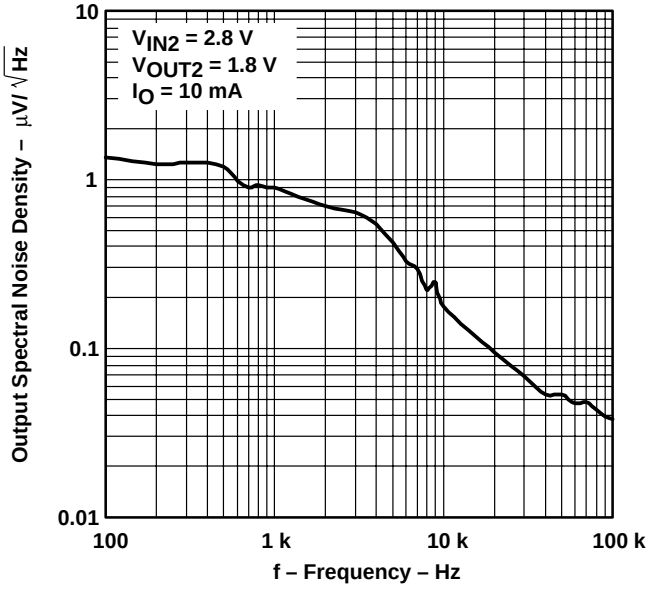



Figure 13

**OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY**

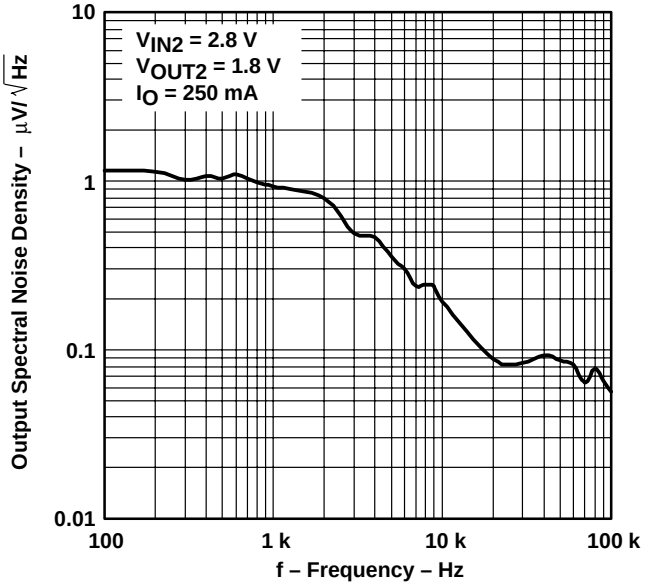



Figure 14

## TYPICAL CHARACTERISTICS

**OUTPUT IMPEDANCE vs FREQUENCY**

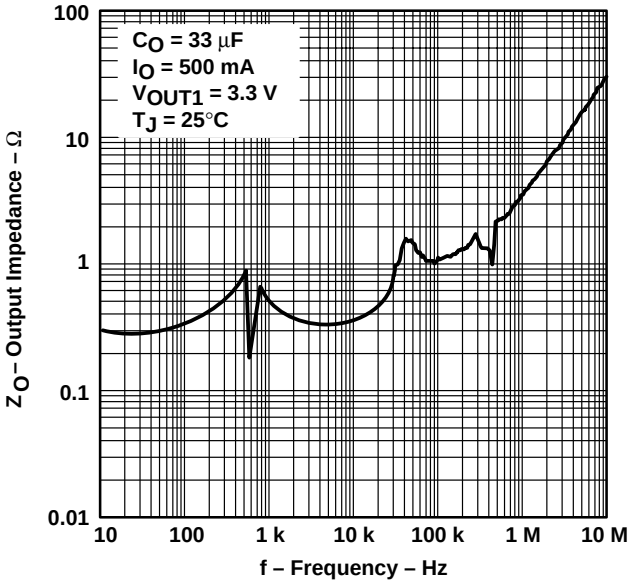



**Figure 15**

**OUTPUT IMPEDANCE vs FREQUENCY**

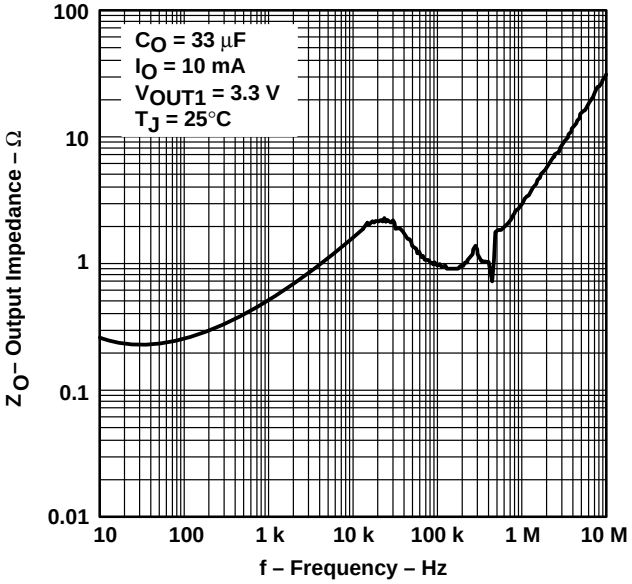



**Figure 16**

**OUTPUT IMPEDANCE vs FREQUENCY**

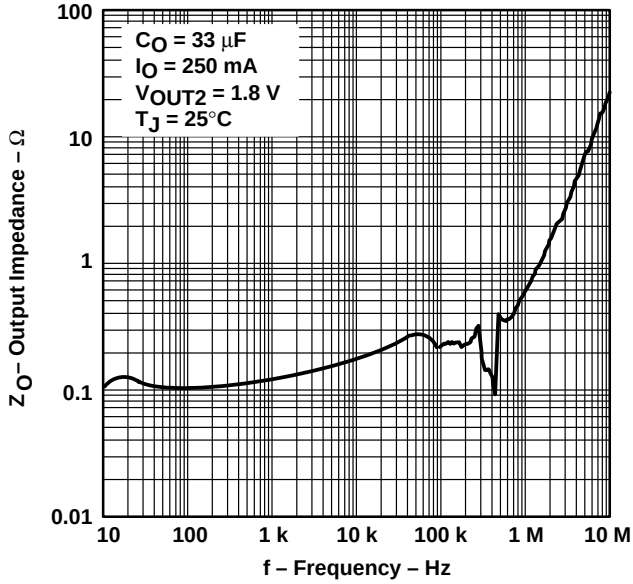



**Figure 17**

**OUTPUT IMPEDANCE vs FREQUENCY**

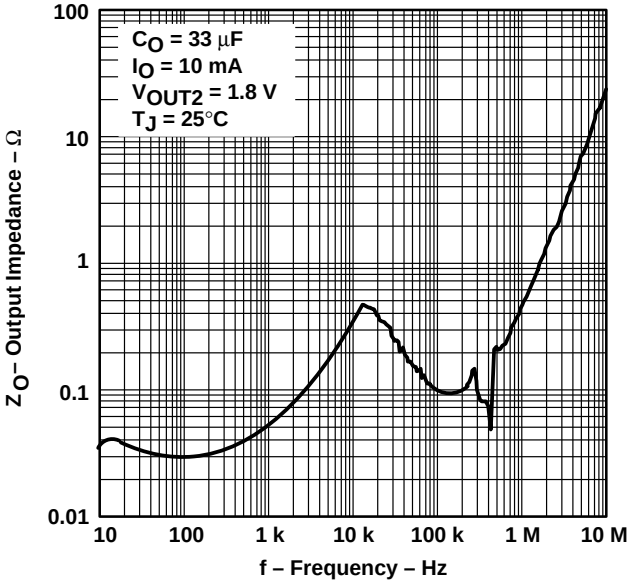



**Figure 18**

## TYPICAL CHARACTERISTICS

**DROPOUT VOLTAGE vs TEMPERATURE**

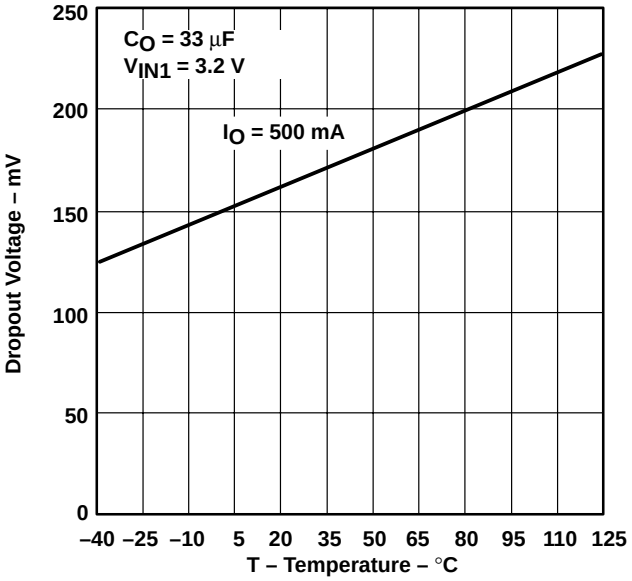



Figure 19

**DROPOUT VOLTAGE vs TEMPERATURE**

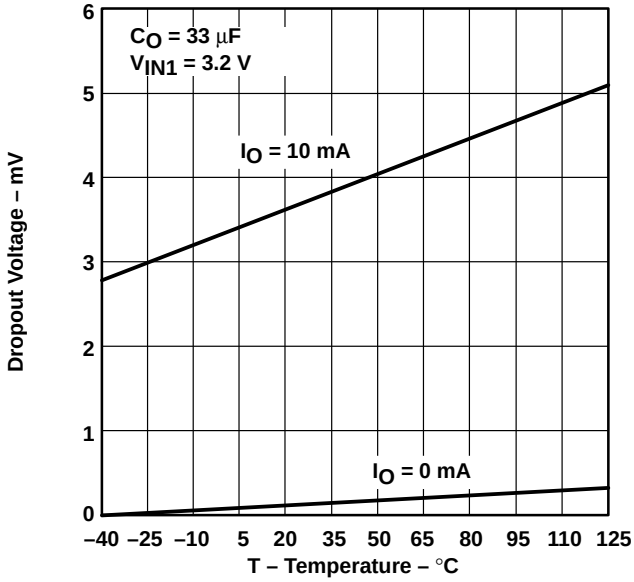



Figure 20

**TPS70202 DROPOUT VOLTAGE vs INPUT VOLTAGE**

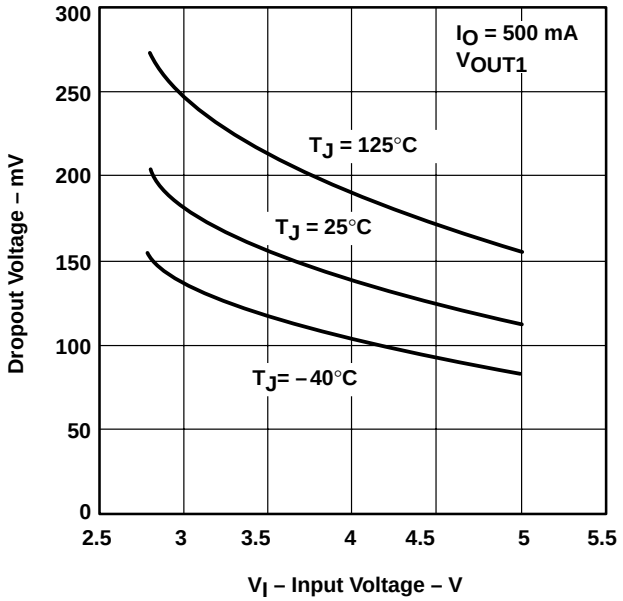



Figure 21

**TPS70202 DROPOUT VOLTAGE vs INPUT VOLTAGE**

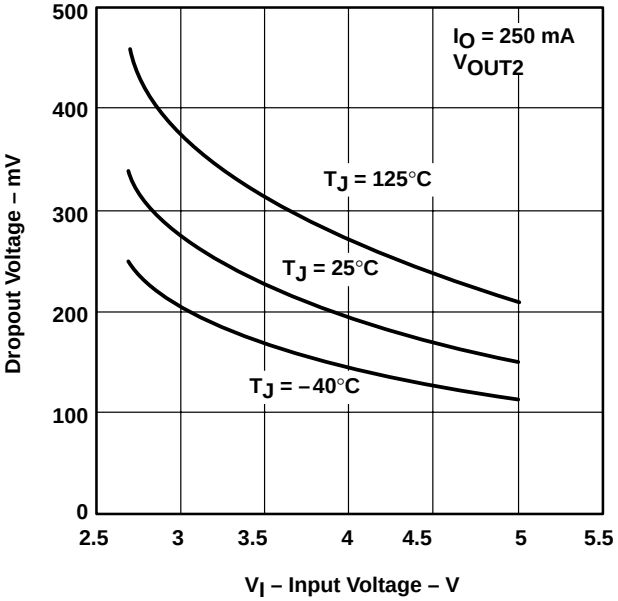



Figure 22

## TYPICAL CHARACTERISTICS

**LOAD TRANSIENT RESPONSE**

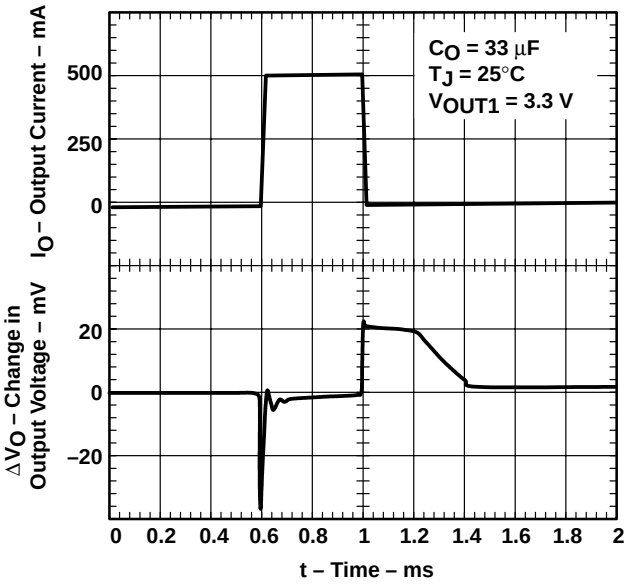



**Figure 23**

**LOAD TRANSIENT RESPONSE**

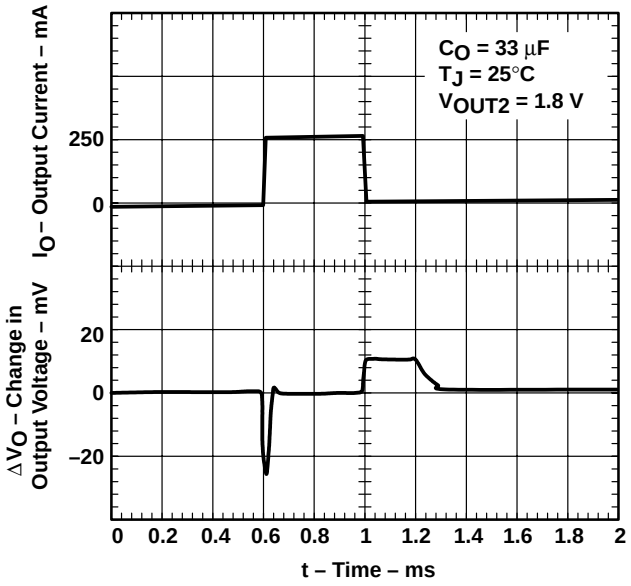



**Figure 24**

**LINE TRANSIENT RESPONSE**

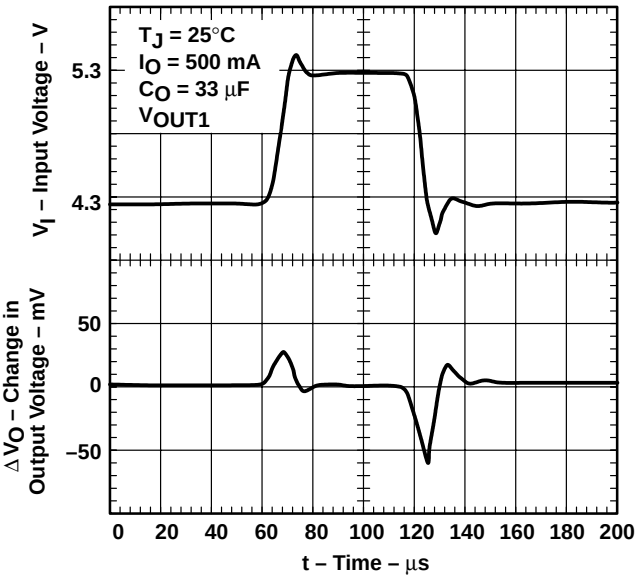



**Figure 25**

**LINE TRANSIENT RESPONSE**

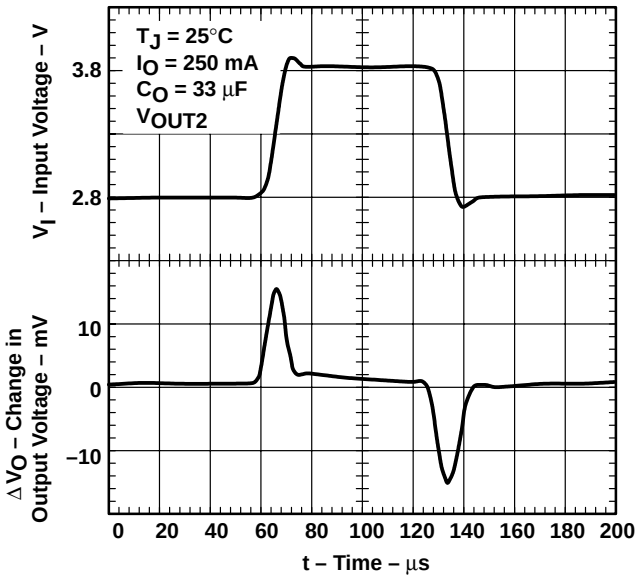



**Figure 26**

## TYPICAL CHARACTERISTICS

**OUTPUT VOLTAGE vs TIME (START-UP)**

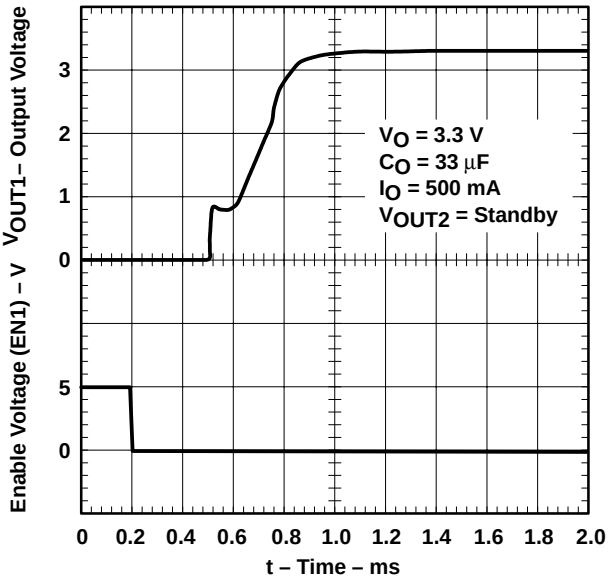



Figure 27

**OUTPUT VOLTAGE vs TIME (START-UP)**

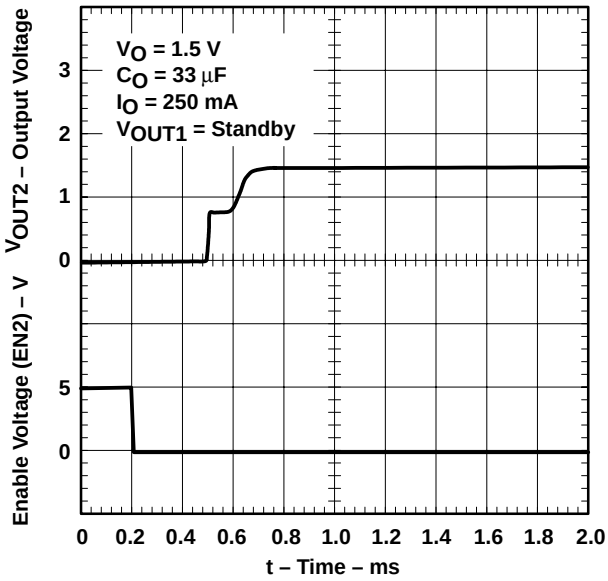



Figure 28

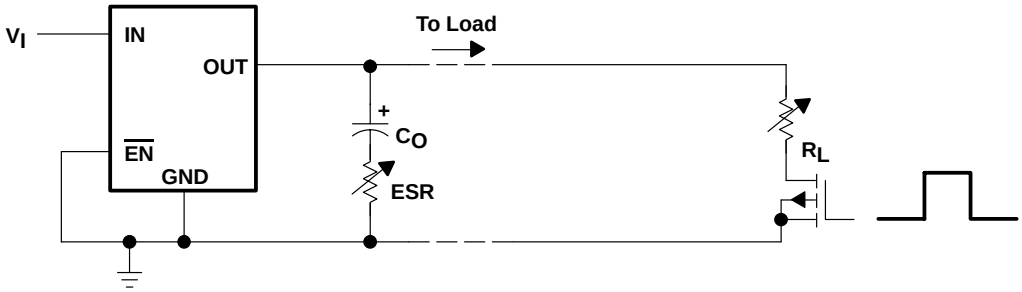



**Figure 29. Test Circuit for Typical Regions of Stability**

† Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to $C_O$.

## TYPICAL CHARACTERISTICS

**TYPICAL REGION OF STABILITY**
**EQUIVALENT SERIES RESISTANCE†**
**vs**
**OUTPUT CURRENT**

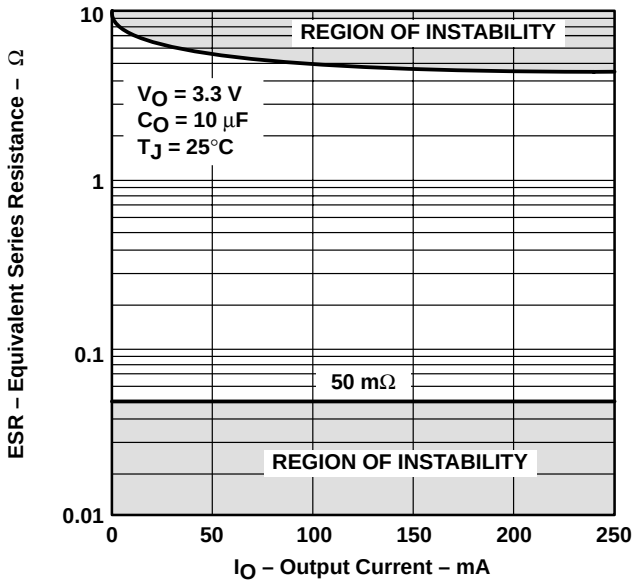



**Figure 30**

**TYPICAL REGION OF STABILITY**
**EQUIVALENT SERIES RESISTANCE†**
**vs**
**OUTPUT CURRENT**

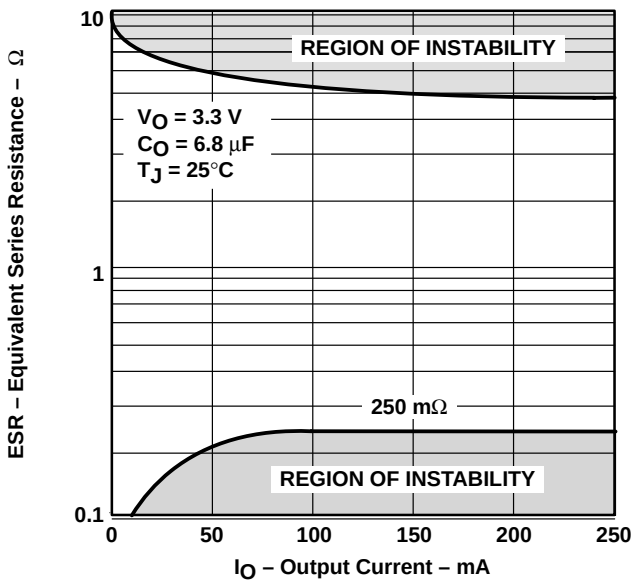



**Figure 31**

**TYPICAL REGION OF STABILITY**
**EQUIVALENT SERIES RESISTANCE†**
**vs**
**OUTPUT CURRENT**

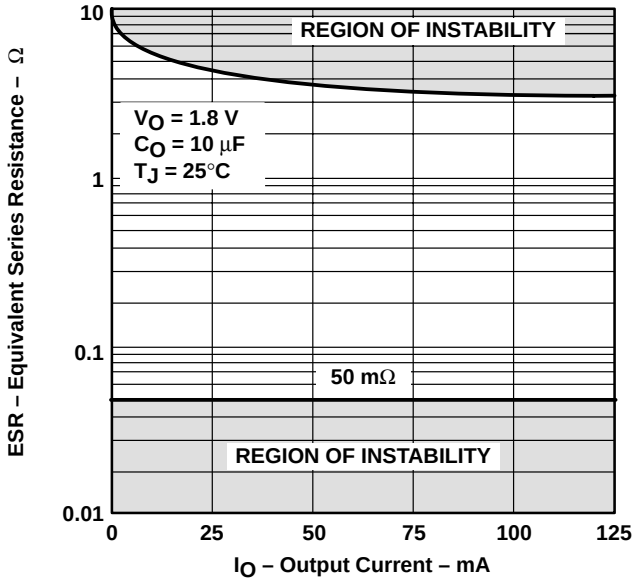



**Figure 32**

**TYPICAL REGION OF STABILITY**
**EQUIVALENT SERIES RESISTANCE†**
**vs**
**OUTPUT CURRENT**

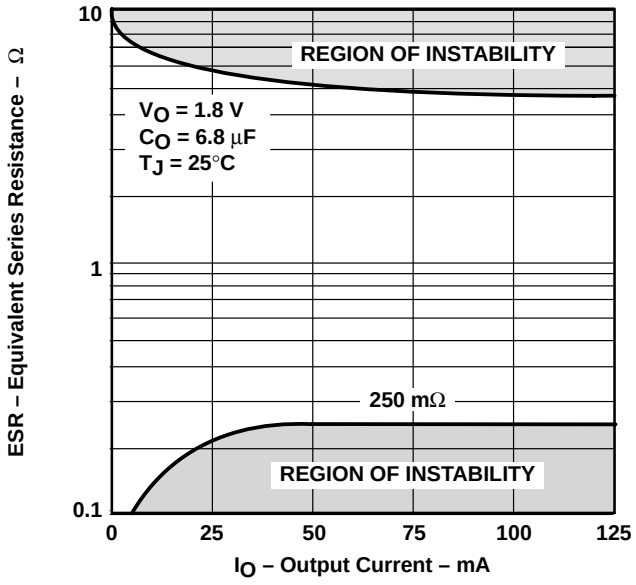



**Figure 33**

† Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to $C_O$.

## APPLICATION INFORMATION

### timing diagrams

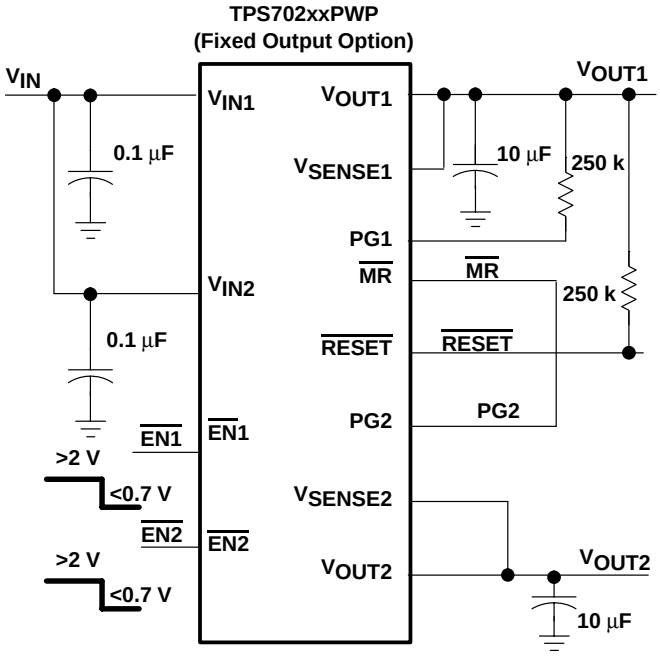
The following figures provide a timing diagram of how this device functions in different configurations.

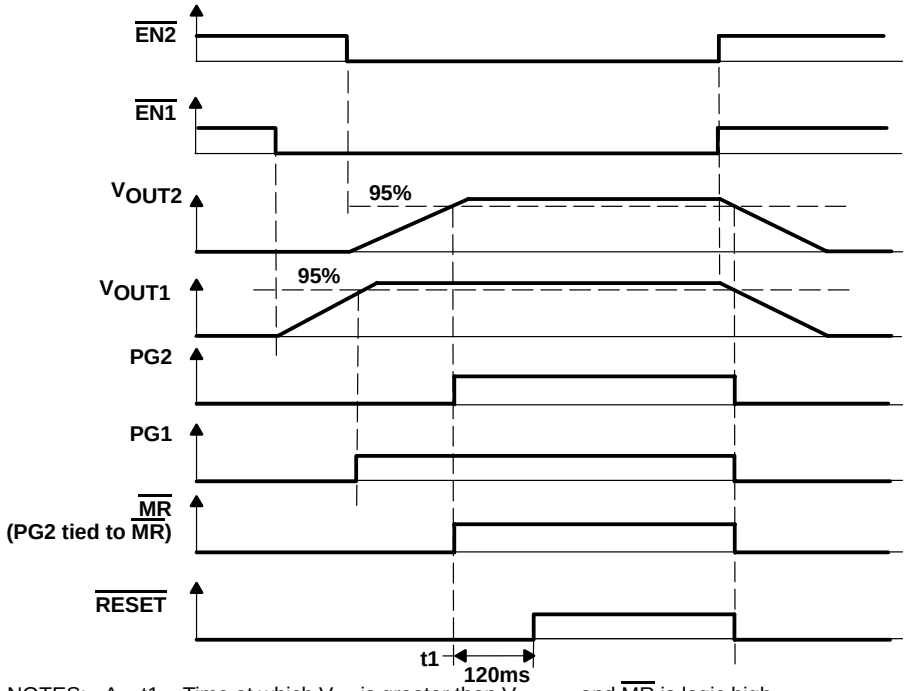
**application conditions not shown in block diagram**:

$V_{IN1}$ and $V_{IN2}$ are tied to the same fixed input voltage greater than the $V_{UVLO}$. PG2 is tied to $\overline{MR}$.

**explanation of timing diagrams:**

$\overline{EN1}$ and $\overline{EN2}$ are initially high; therefore, both regulators are off, and PG1 and PG2 (tied to $\overline{MR}$) are at logic low. Since $\overline{MR}$ is at logic low, $\overline{RESET}$ is also at logic low. When $\overline{EN1}$ is taken to logic low, $V_{OUT1}$ turns on. Later, when $\overline{EN2}$ is taken to logic low, $V_{OUT2}$ turns on. When $V_{OUT1}$ reaches 95% of its regulated output voltage, PG1 goes to logic high. When $V_{OUT2}$ reaches 95% of its regulated output voltage, PG2 (tied to $\overline{MR}$) goes to logic high. When $V_{IN1}$ is greater than $V_{UVLO}$ and $\overline{MR}$ (tied to PG2) is at logic high, $\overline{RESET}$ is pulled to logic high after a 120 ms delay. When $\overline{EN1}$ and $\overline{EN2}$ are returned to logic high, both devices power down and both PG1, PG2 (tied to $\overline{MR2}$), and $\overline{RESET}$ return to logic low.




NOTES: A. t1 – Time at which $V_{IN}$ is greater than $V_{UVLO}$ and $\overline{MR}$ is logic high.
B. The timing diagrams are not drawn to scale.

**Figure 34. Timing When $V_{OUT1}$ Is Enabled Before $V_{OUT2}$**

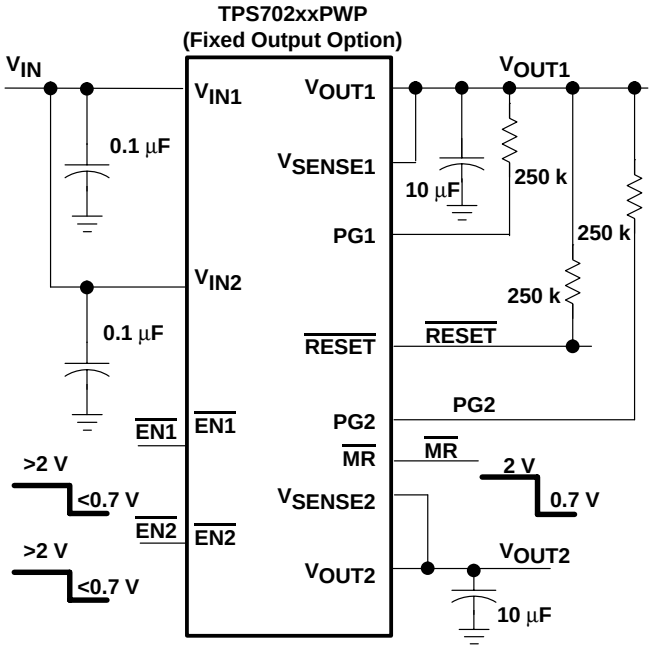
## APPLICATION INFORMATION

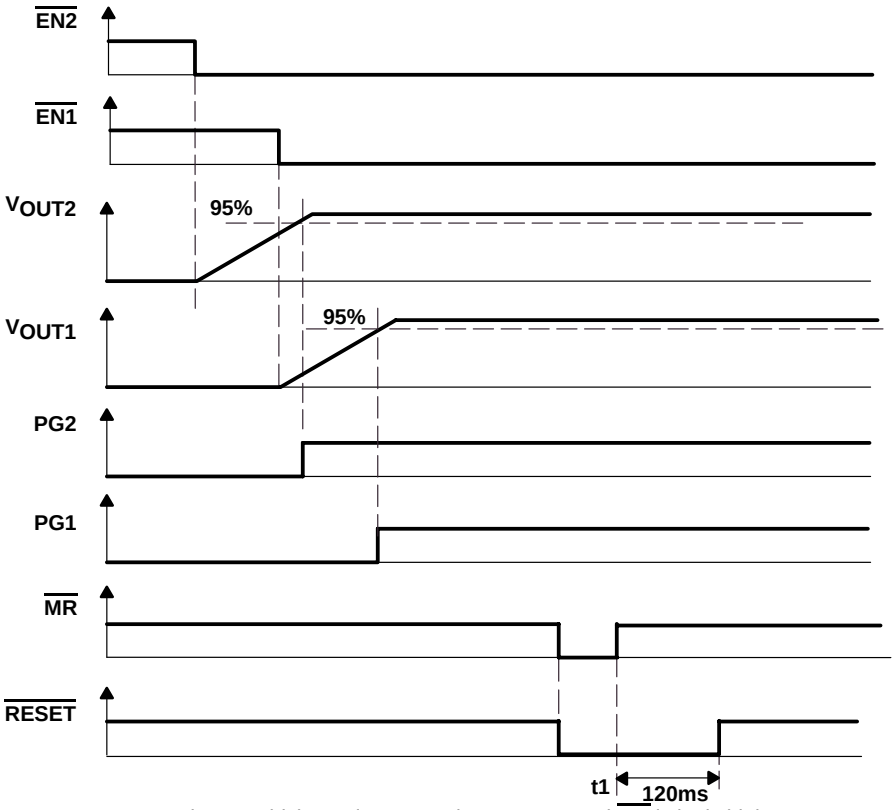
**application conditions not shown in block diagram**:

$V_{IN1}$ and $V_{IN2}$ are tied to the same fixed input voltage greater than $V_{UVLO}$. $\overline{MR}$ is initially logic high but is eventually toggled.

**explanation of timing diagrams:**

$\overline{EN1}$ and $\overline{EN2}$ are initially high; therefore, both regulators are off, and PG1 and PG2 are at logic low. Since $V_{IN1}$ is greater than $V_{UVLO}$ and $\overline{MR}$ is at logic high, $\overline{RESET}$ is also at logic high. When $\overline{EN2}$ is taken to logic low, $V_{OUT2}$ turns on. Later, when $\overline{EN1}$ is taken to logic low, $V_{OUT1}$ turns on. When $V_{OUT2}$ reaches 95% of its regulated output voltage, PG2 goes to logic high. When $V_{OUT1}$ reaches 95% of its regulated output voltage, PG1 goes to logic high. When $\overline{MR}$ is taken to logic low, $\overline{RESET}$ is taken low. When $\overline{MR}$ returns to logic high, $\overline{RESET}$ returns to logic high after a 120 ms delay.




NOTES: A. t1 – Time at which $V_{IN}$ is greater than $V_{UVLO}$ and $\overline{MR}$ is logic high.
B. The timing diagram is not drawn to scale.

**Figure 35. Timing When $\overline{MR}$ Is Toggled**

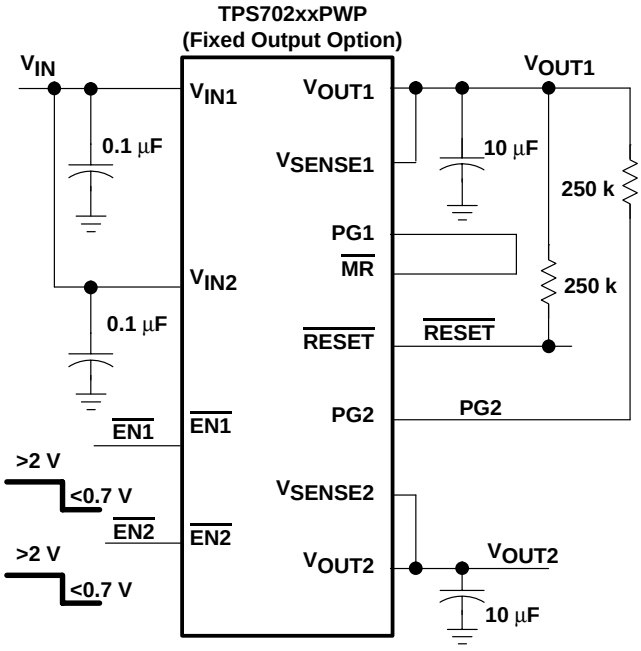
## APPLICATION INFORMATION

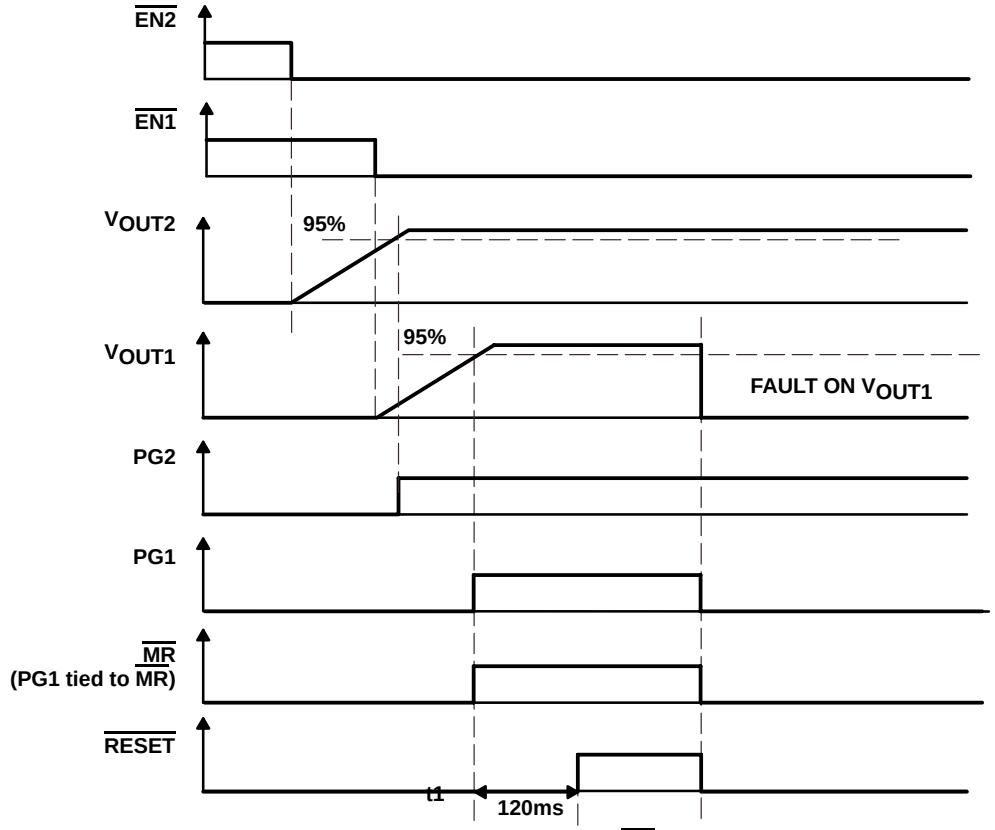
**application conditions not shown in block diagram**:

$V_{IN1}$ and $V_{IN2}$ are tied to same fixed input voltage greater than $V_{UVLO}$. PG1 is tied to $\overline{MR}$.

**explanation of timing diagrams:**

$\overline{EN1}$ and $\overline{EN2}$ are initially high; therefore, both regulators are off, and PG1 (tied to $\overline{MR}$) and PG2 are at logic low. Since $\overline{MR}$ is at logic low, $\overline{RESET}$ is also at logic low. When $\overline{EN2}$ is taken to logic low, $V_{OUT2}$ turns on. Later, when $\overline{EN1}$ is taken to logic low, $V_{OUT1}$ turns on. When $V_{OUT2}$ reaches 95% of its regulated output voltage, PG2 goes to logic high. When $V_{OUT1}$ reaches 95% of its regulated output voltage, PG1 goes to logic high. When $V_{IN1}$ is greater than $V_{UVLO}$ and $\overline{MR}$ (tied to PG2) is at logic high, $\overline{RESET}$ is pulled to logic high after a 120 ms delay. When a fault on $V_{OUT1}$ causes it to fall below 95% of its regulated output voltage, PG1 (tied to $\overline{MR}$) goes to logic low. Since $\overline{MR}$ is logic low, $\overline{RESET}$ goes to logic low. $V_{OUT2}$ is unaffected.




NOTES: A. t1 – Time at which $V_{IN}$ is greater than $V_{UVLO}$ and $\overline{MR}$ is logic high.
B. The timing diagram is not drawn to scale.

**Figure 36. Timing When There Is a Fault on $V_{OUT1}$**

## APPLICATION INFORMATION

### input capacitor

For a typical application, an input bypass capacitor (0.1 μF – 1 μF) is recommended. This capacitor will filter any high frequency noise generated in the line. For fast transient condition where droop at the input of the LDO may occur due to high inrush current, it is recommended to place a larger capacitor at the input as well. The size of this capacitor is dependant on the output current and response time of the main power supply, as well as the distance to the $V_I$ pins of the LDO.

### output capacitor

As with most LDO regulators, the TPS702xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance values are 10 μF ceramic capacitors with an ESR (equivalent series resistance) between 50-mΩ and 2.5-Ω or 6.8-μF tantalum capacitors with ESR between 250 mΩ and 4 Ω. Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors with capacitance values greater than 10 μF are all suitable, provided they meet the requirements described above. Larger capacitors provide a wider range of stability and better load transient response. Below is a partial listing of surface-mount capacitors usable with the TPS702xx. for fast transient response application.

This information, along with the ESR graphs, is included to assist in selection of suitable capacitance for the user's application. When necessary to achieve low height requirements along with high output current and/or high load capacitance, several higher ESR capacitors can be used in parallel to meet the guidelines above.

| VALUE | MFR. | MAX ESR† | PART NO. |
|---|---|---|---|
| 22 μF | Kemet | 345 mΩ | 7495C226K0010AS |
| 33 μF | Sanyo | 100 mΩ | 10TPA33M |
| 47 μF | Sanyo | 100 mΩ | 6TPA47M |
| 68 μF | Sanyo | 45 mΩ | 10TPC68M |

### ESR and transient response

LDOs typically require an external output capacitor for stability. In fast transient response applications, capacitors are used to support the load current while LDO amplifier is responding. In most applications, one capacitor is used to support both functions.

Besides its capacitance, every capacitor also contains parasitic impedances. These parasitic impedances are resistive as well as inductive. The resistive impedance is called equivalent series resistance (ESR), and the inductive impedance is called equivalent series inductance (ESL). The equivalent schematic diagram of any capacitor can therefore be drawn as shown in Figure 37.


**Figure 37. ESR and ESL**

In most cases one can neglect the effect of inductive impedance ESL. Therefore, the following application focuses mainly on the parasitic resistance ESR.

## APPLICATION INFORMATION

Figure 38 shows the output capacitor and its parasitic impedances in a typical LDO output stage.

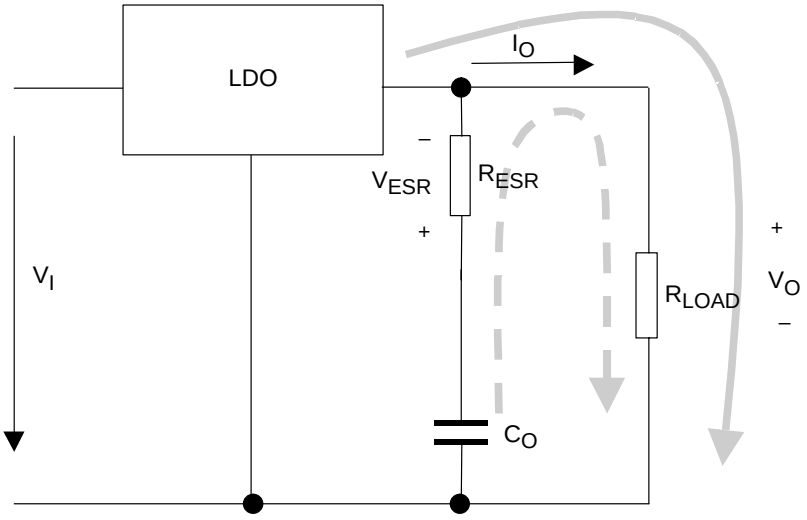



**Figure 38. LDO Output Stage With Parasitic Resistances ESR**

In steady state (dc state condition), the load current is supplied by the LDO (solid arrow) and the voltage across the capacitor is the same as the output voltage ($V(C_O) = V_O$). This means no current is flowing into the $C_O$ branch. If $I_O$ suddenly increases (transient condition), the following occurs:

- The LDO is not able to supply the sudden current need due to its response time ($t_1$ in Figure 39). Therefore, capacitor $C_O$ provides the current for the new load condition (dashed arrow). $C_O$ now acts like a battery with an internal resistance, ESR. Depending on the current demand at the output, a voltage drop occurs at $R_{ESR}$. This voltage is shown as $V_{ESR}$ in Figure 38.
- When $C_O$ is conducting current to the load, initial voltage at the load will be $V_O = V(C_O) – V_{ESR}$. Due to the discharge of $C_O$, the output voltage $V_O$ will drop continuously until the response time $t_1$ of the LDO is reached and the LDO resumes supplying the load. From this point, the output voltage starts rising again until it reaches the regulated voltage. This period is shown as $t_2$ in Figure 39.

The figure also shows the impact of different ESRs on the output voltage. The left brackets show different levels of ESRs where number 1 displays the lowest and number 3 displays the highest ESR.

From above, the following conclusions can be drawn:

- The higher the ESR, the larger the droop at the beginning of load transient.
- The smaller the output capacitor, the faster the discharge time and the bigger the voltage droop during the LDO response period.

## APPLICATION INFORMATION

### conclusion

To minimize the transient output droop, capacitors must have a low ESR and be large enough to support the minimum output voltage requirement.

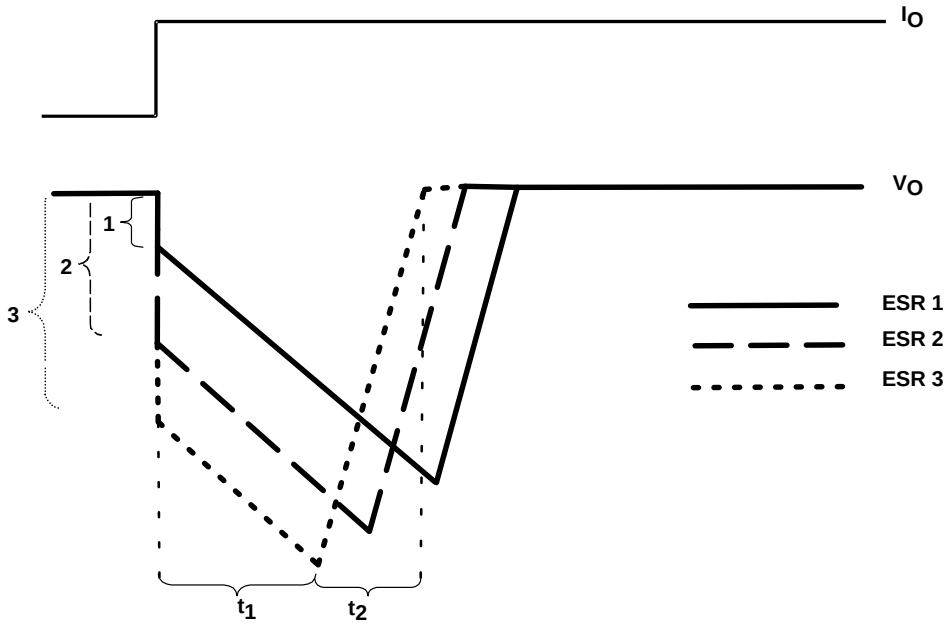



**Figure 39. Correlation of Different ESRs and Their Influence to the Regulation of $V_O$ at a Load Step From Low-to-High Output Current**

## APPLICATION INFORMATION

### programming the TPS70202 adjustable LDO regulator

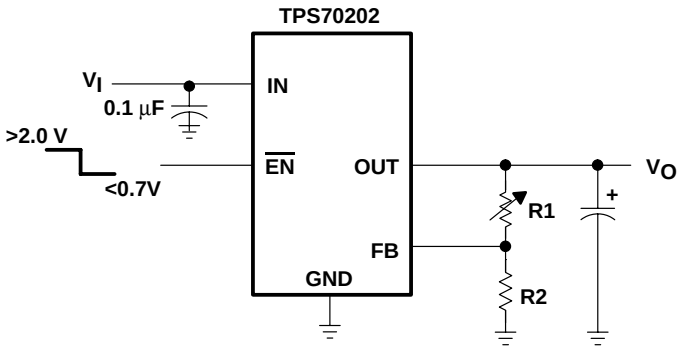
The output voltage of the TPS70202 adjustable regulators is programmed using an external resistor divider as shown in Figure 40.

Resistors R1 and R2 should be chosen for approximately 50-μA divider current. Lower value resistors can be used, but offer no inherent advantage and waste more power. Higher values should be avoided as leakage currents at the sense terminal increase the output voltage error. The recommended design procedure is to choose R2 = 30.1 kΩ to set the divider current at approximately 50 μA and then calculate R1 using:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \times R2$$

where

$V_{ref}$ = 1.224 V typ (the internal reference voltage)




**OUTPUT VOLTAGE PROGRAMMING GUIDE**

| OUTPUT VOLTAGE | R1 | R2 | UNIT |
|---|---|---|---|
| 2.5 V | 31.6 | 30.1 | kΩ |
| 3.3 V | 51.1 | 30.1 | kΩ |
| 3.6 V | 59.0 | 30.1 | kΩ |

**Figure 40. TPS70202 Adjustable LDO Regulator Programming**

### regulator protection

Both TPS702xx PMOS-pass transistors have built-in back diodes that conduct reverse currents when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. When extended reverse voltage is anticipated, external limiting may be appropriate.

The TPS702xx also features internal current limiting and thermal protection. During normal operation, the TPS702xx regulator 1 limits output current to approximately 1.6 A (typ) and regulator 2 limits output current to approximately 750 mA (typ). When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 150°C(typ), thermal-protection circuitry shuts it down. Once the device has cooled below 130°C(typ), regulator operation resumes.

## APPLICATION INFORMATION

### power dissipation and junction temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, $P_D$, which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}}$$

where

$T_J max$ is the maximum allowable junction temperature.

$R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package, i.e., 32.6°C/W for the 20-terminal PWP with no airflow.

$T_A$ is the ambient temperature.

The regulator dissipation is calculated using:

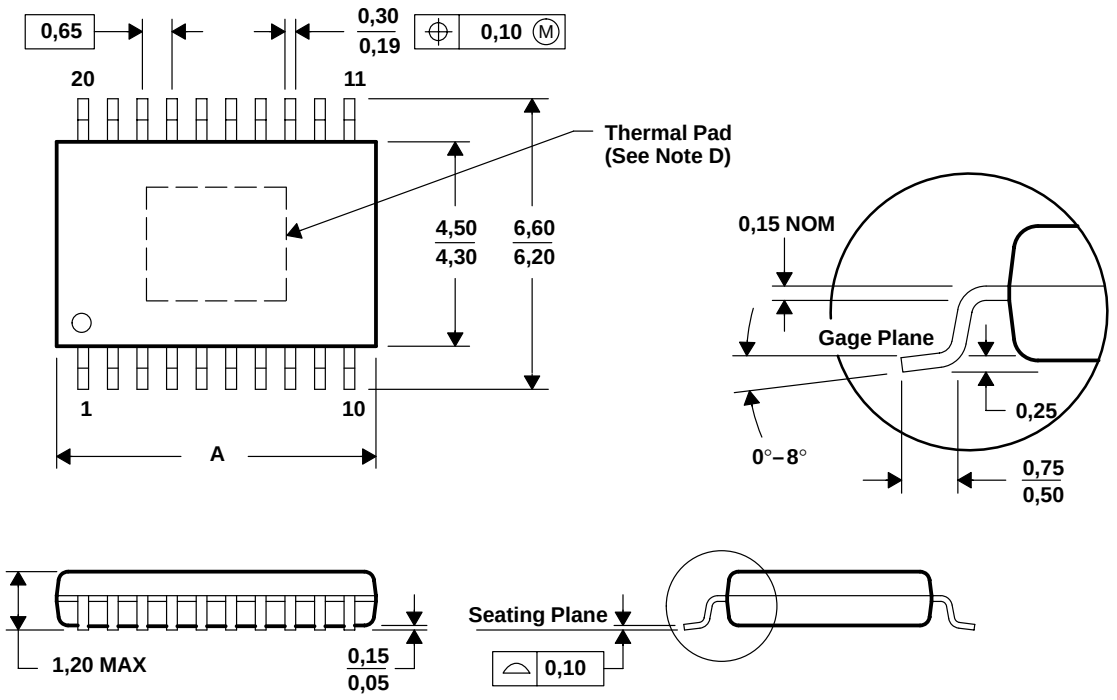
$$P_D = \left(V_I - V_O\right) \times I_O$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation triggers the thermal protection circuit.

## MECHANICAL DATA

**PWP (R-PDSO-G**)** **PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE**

**20-PIN SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 | 28 |
|---|---|---|---|---|---|
| A MAX | 5,10 | 5,10 | 6,60 | 7,90 | 9,80 |
| A MIN | 4,90 | 4,90 | 6,40 | 7,70 | 9,60 |

**4073225/E 03/97**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MO-153

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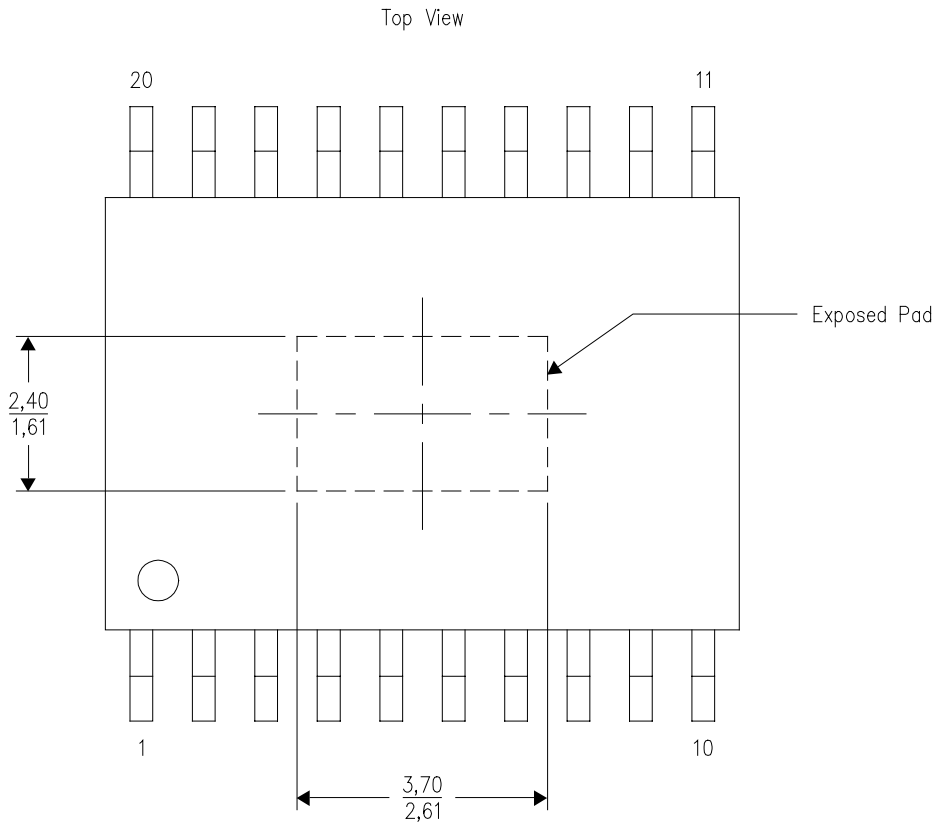
**PWP (R-PDSO-G20)** **PowerPAD™ PLASTIC SMALL-OUTLINE**




06/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. For additional information on the PowerPAD™ package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, ***PowerPAD Thermally Enhanced Package***, Texas Instruments Literature No. SLMA002 and Application Brief, ***PowerPAD Made Easy***, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

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