MCP3202

2.7V Dual Channel 12-Bit A/D Converter with SPI® Serial Interface

FEATURES

- 12-bit resolution
- ±1 LSB max DNL
- ±1 LSB max INL (MCP3202-B)
- ±2 LSB max INL (MCP3202-C)
- Analog inputs programmable as single-ended or pseudo-differential pairs
- On-chip sample and hold
- SPI® serial interface (modes 0,0 and 1,1)
- Single supply operation: 2.7V - 5.5V
- 100ksps max. sampling rate at V_{DD} = 5V
- 50ksps max. sampling rate at V_{DD} = 2.7V
- Low power CMOS technology
  - 500nA typical standby current, 5µA max.
  - 550µA max. active current at 5V
- Industrial temp range: -40°C to +85°C
- 8-pin PDIP SOIC and TSSOP packages

APPLICATIONS

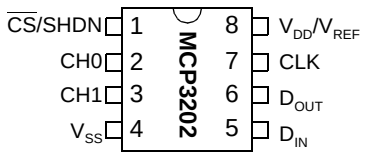
- Sensor Interface
- Process Control
- Data Acquisition
- Battery Operated Systems

DESCRIPTION

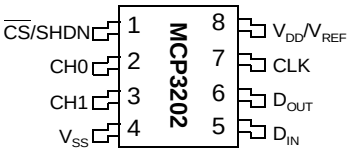
The Microchip Technology Inc. MCP3202 is a successive approximation 12-bit Analog-to-Digital (A/D) Converter with on-board sample and hold circuitry. The MCP3202 is programmable to provide a single pseudo-differential input pair or dual single-ended inputs. Differential Nonlinearity (DNL) is specified at ±1 LSB, and Integral Nonlinearity (INL) is offered in ±1 LSB (MCP3202-B) and ±2 LSB (MCP3202-C) versions. Communication with the device is done using a simple serial interface compatible with the SPI protocol. The device is capable of conversion rates of up to 100ksps at 5V and 50ksps at 2.7V. The MCP3202 device operates over a broad voltage range (2.7V - 5.5V). Low current design permits operation with typical standby and active currents of only 500nA and 375µA, respectively. The MCP3202 is offered in 8-pin PDIP, TSSOP and 150mil SOIC packages.

PACKAGE TYPES

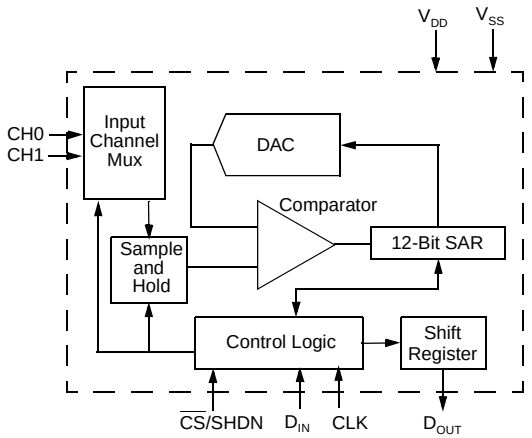
PDIP



SOIC, TSSOP



FUNCTIONAL BLOCK DIAGRAM



1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

V_{DD}.....7.0V
All inputs and outputs w.r.t. V_{SS} ..... -0.6V to V_{DD} +0.6V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied.....-65°C to +125°C
Soldering temperature of leads (10 seconds) ..+300°C
ESD protection on all pins.....> 4kV

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

NAME	FUNCTION
V_{DD}/V_{REF}	+2.7V to 5.5V Power Supply and Reference Voltage Input
CH0	Channel 0 Analog Input
CH1	Channel 1 Analog Input
CLK	Serial Clock
D_{IN}	Serial Data In
D_{OUT}	Serial Data Out
$\overline{CS}$/SHDN	Chip Select/Shutdown Input

ELECTRICAL CHARACTERISTICS

All parameters apply at V_{DD} = 5.5V, V_{SS} = 0V, T_{AMB} = -40°C to +85°C, f_{SAMPLE} = 100ksps and f_{CLK} = 18*f_{SAMPLE} unless otherwise noted.

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Conversion Rate						
Conversion Time	t_{CONV}			12	clock cycles	
Analog Input Sample Time	t_{SAMPLE}		1.5		clock cycles	
Throughput Rate	f_{SAMPLE}			100 50	ksps ksps	$V_{DD} = V_{REF}$ = 5V $V_{DD} = V_{REF}$ = 2.7V
DC Accuracy						
Resolution			12		bits	
Integral Nonlinearity	INL		±0.75 ±1	±1 ±2	LSB LSB	MCP3202-B MCP3202-C
Differential Nonlinearity	DNL		±0.5	±1	LSB	No missing codes over temperature
Offset Error			±1.25	±3	LSB	
Gain Error			±1.25	±5	LSB	
Dynamic Performance						
Total Harmonic Distortion			-82		dB	V_{IN} = 0.1V to 4.9V@1kHz
Signal to Noise and Distortion (SINAD)			72		dB	V_{IN} = 0.1V to 4.9V@1kHz
Spurious Free Dynamic Range			86		dB	V_{IN} = 0.1V to 4.9V@1kHz
Analog Inputs						
Input Voltage Range for CH0 or CH1 in Single-Ended Mode		V_{SS}		V_{REF}	V	
Input Voltage Range for IN+ in Pseudo-Differential Mode		IN-		V_{REF}+IN-		See Sections 3.1 and 4.1
Input Voltage Range for IN- in Pseudo-Differential Mode		V_{SS}-100		V_{SS}+100	mV	See Sections 3.1 and 4.1
Leakage Current			.001	±1	µA	
Switch Resistance	R_{SS}		1K		Ω	See Figure 4-1
Sample Capacitor	C_{SAMPLE}		20		pF	See Figure 4-1

ELECTRICAL CHARACTERISTICS (CONTINUED)

All parameters apply at V_{DD} = 5.5V, V_{SS} = 0V, T_{AMB} = -40°C to +85°C, f_{SAMPLE} = 100ksps and f_{CLK} = 18*f_{SAMPLE} unless otherwise noted.

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Digital Input/Output						
Data Coding Format		Straight Binary				
High Level Input Voltage	V_{IH}	0.7 V_{DD}			V	
Low Level Input Voltage	V_{IL}			0.3 V_{DD}	V	
High Level Output Voltage	V_{OH}	4.1			V	I_{OH} = -1mA, V_{DD} = 4.5V
Low Level Output Voltage	V_{OL}			0.4	V	I_{OL} = 1mA, V_{DD} = 4.5V
Input Leakage Current	I_{LI}	-10		10	µA	V_{IN} = V_{SS} or V_{DD}
Output Leakage Current	I_{LO}	-10		10	µA	V_{OUT} = V_{SS} or V_{DD}
Pin Capacitance (All Inputs/Outputs)	C_{IN}, C_{OUT}			10	pF	V_{DD} = 5.0V (Note 1) T_{AMB} = 25°C, f = 1 MHz
Timing Parameters						
Clock Frequency	f_{CLK}			1.8 0.9	MHz MHz	V_{DD} = 5V (Note 2) V_{DD} = 2.7V (Note 2)
Clock High Time	t_{HI}	250			ns	
Clock Low Time	t_{LO}	250			ns	
$\overline{CS}$ Fall To First Rising CLK Edge	t_{SUCS}	100			ns	
Data Input Setup Time	t_{SU}			50	ns	
Data Input Hold Time	t_{HD}			50	ns	
CLK Fall To Output Data Valid	t_{DO}			200	ns	See Test Circuits, Figure 1-2
CLK Fall To Output Enable	t_{EN}			200	ns	See Test Circuits, Figure 1-2
$\overline{CS}$ Rise To Output Disable	t_{DIS}			100	ns	See Test Circuits, Figure 1-2 Note 1
$\overline{CS}$ Disable Time	t_{CSH}	500			ns	
D_{OUT} Rise Time	t_R			100	ns	See Test Circuits, Figure 1-2 Note 1
D_{OUT} Fall Time	t_F			100	ns	See Test Circuits, Figure 1-2 Note 1
Power Requirements						
Operating Voltage	V_{DD}	2.7		5.5	V	
Operating Current	I_{DD}		375	550	µA	V_{DD} = 5.0V, D_{OUT} unloaded
Standby Current	I_{DDS}		0.5	5	µA	$\overline{CS}$ = V_{DD} = 5.0V

Note 1: This parameter is guaranteed by characterization and not 100% tested.

Note 2: Because the sample cap will eventually lose charge, effective clock rates below 10kHz can affect linearity performance, especially at elevated temperatures. See Section 6.2 for more information.

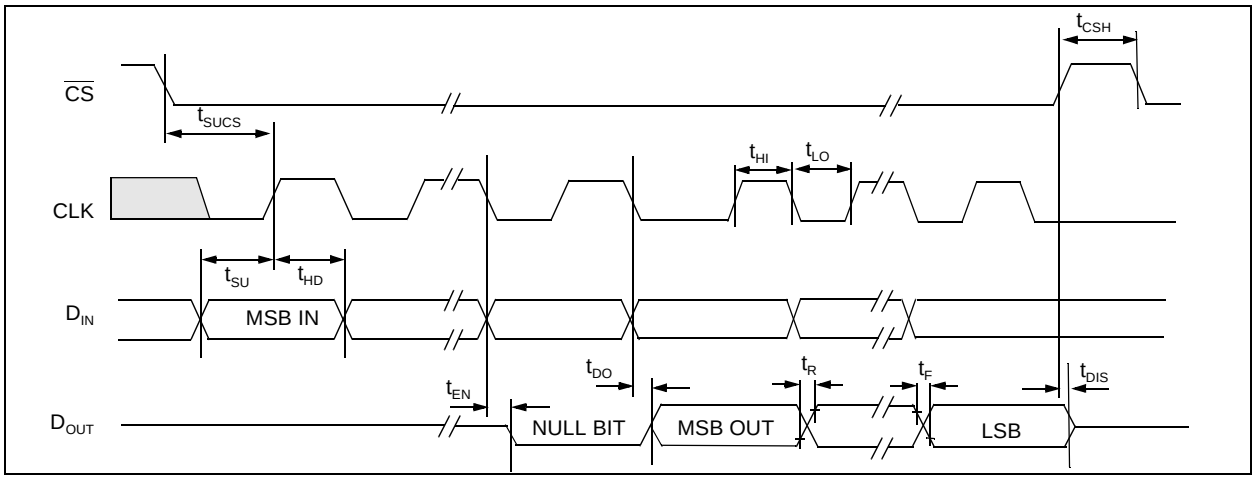
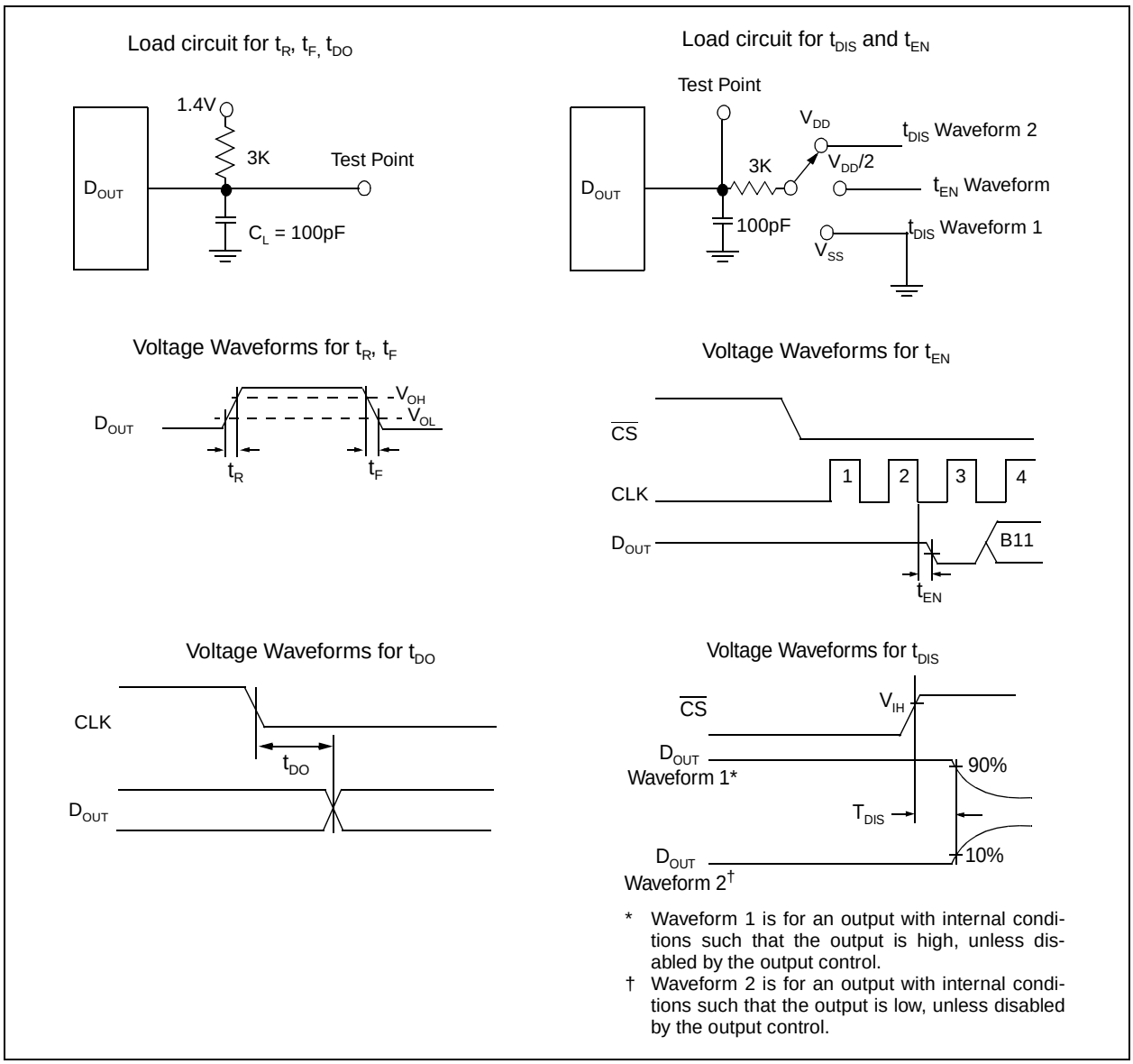


FIGURE 1-1: *Serial Timing.*



* Waveform 1 is for an output with internal conditions such that the output is high, unless disabled by the output control.

† Waveform 2 is for an output with internal conditions such that the output is low, unless disabled by the output control.

FIGURE 1-2: *Test Circuits.*

2.0 TYPICAL PERFORMANCE CHARACTERISTICS

Note: Unless otherwise indicated, V_{DD} = 5V, V_{SS} = 0V, f_{SAMPLE} = 100ksps, f_{CLK} = 18* f_{SAMPLE}, T_A = 25°C

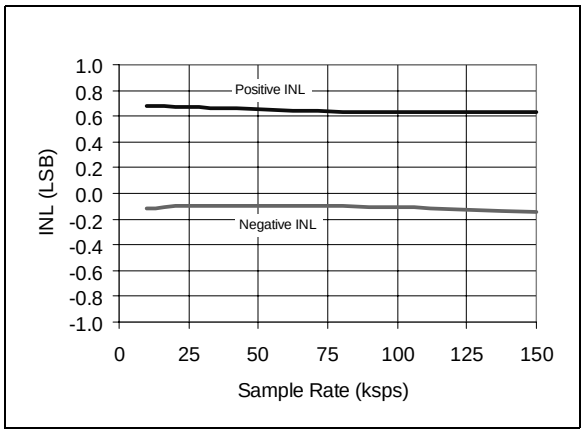


FIGURE 2-1: *Integral Nonlinearity (INL) vs. Sample Rate.*

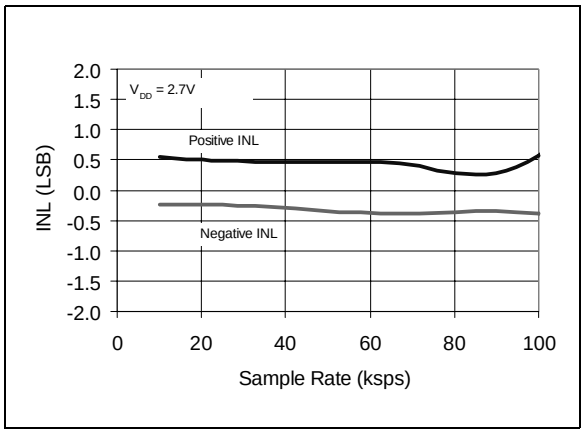


FIGURE 2-4: *Integral Nonlinearity (INL) vs. Sample Rate (V_{DD} = 2.7V).*

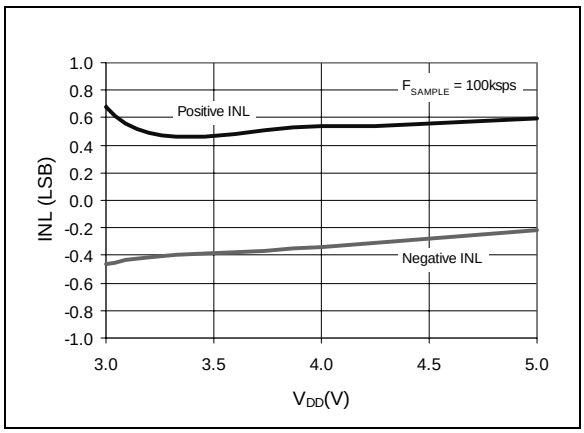


FIGURE 2-2: *Integral Nonlinearity (INL) vs. V_{DD}.*

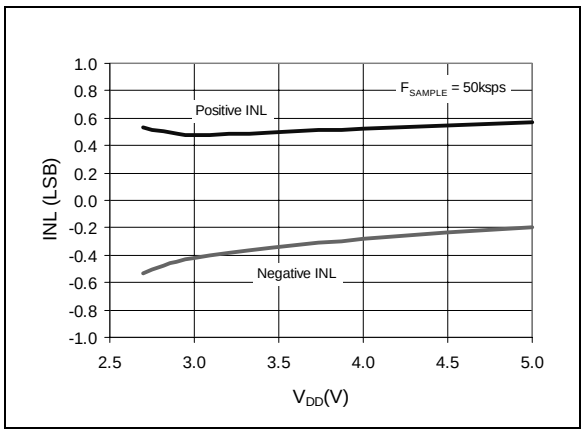


FIGURE 2-5: *Integral Nonlinearity (INL) vs. V_{DD}.*

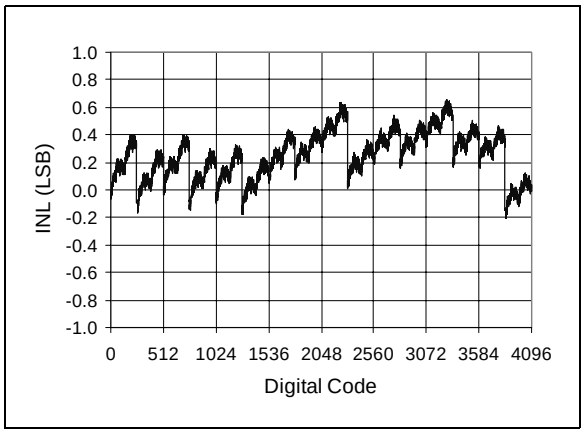


FIGURE 2-3: *Integral Nonlinearity (INL) vs. Code (Representative Part).*

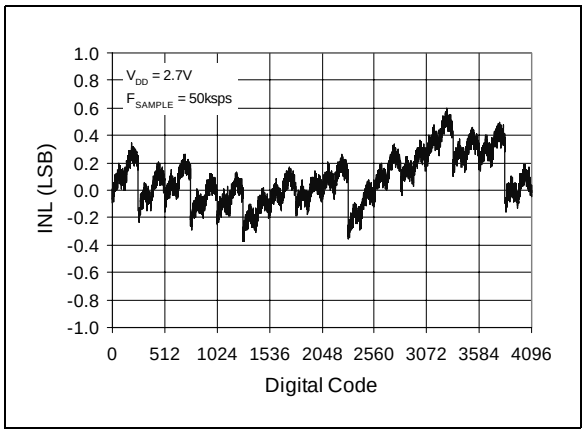


FIGURE 2-6: *Integral Nonlinearity (INL) vs. Code (Representative Part, V_{DD} = 2.7V).*

Note: Unless otherwise indicated, V_{DD} = 5V, V_{SS} = 0V, f_{SAMPLE} = 100ksps, f_{CLK} = 18* f_{SAMPLE}, T_A = 25°C

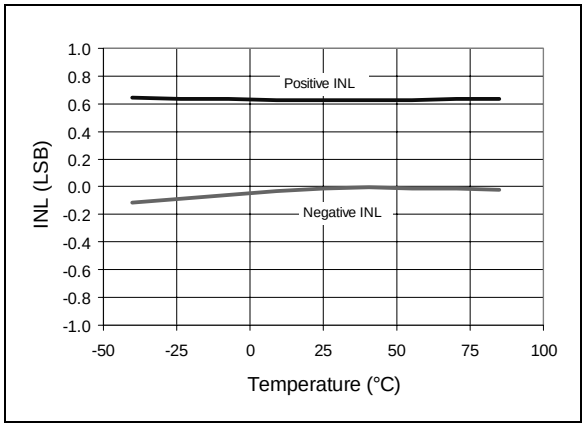


FIGURE 2-7: *Integral Nonlinearity (INL) vs. Temperature.*

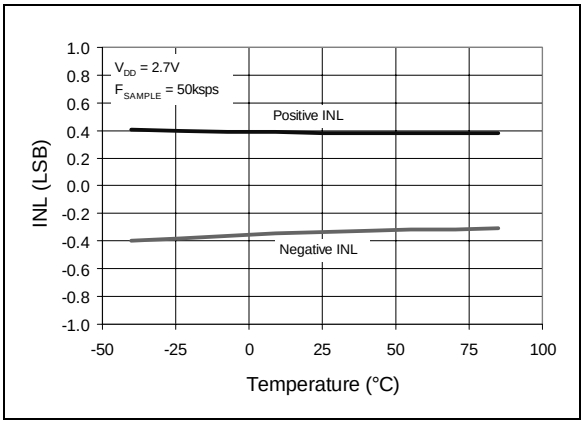


FIGURE 2-10: *Integral Nonlinearity (INL) vs. Temperature (V_{DD} = 2.7V).*

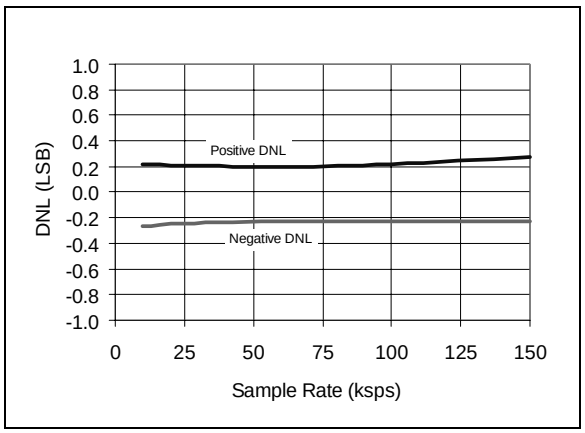


FIGURE 2-8: *Differential Nonlinearity (DNL) vs. Sample Rate.*

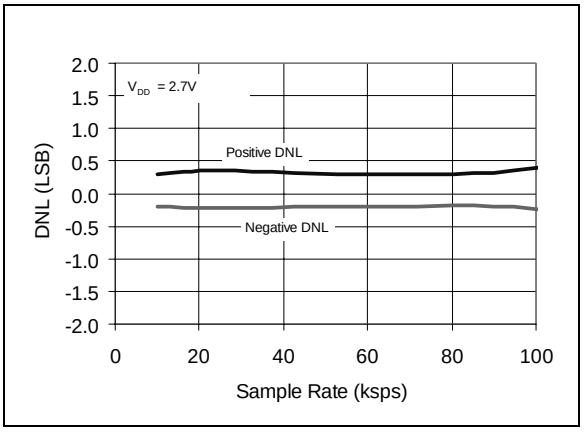


FIGURE 2-11: *Differential Nonlinearity (DNL) vs. Sample Rate (V_{DD} = 2.7V).*

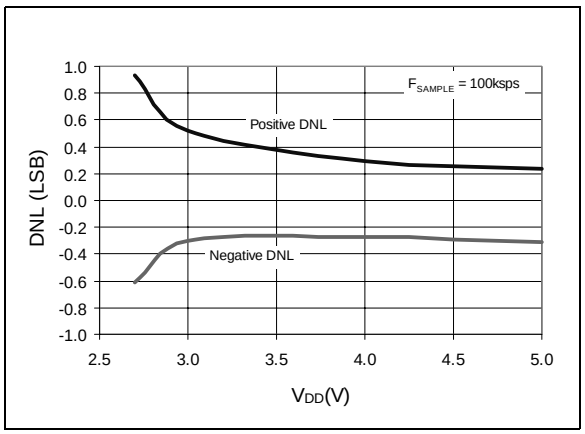


FIGURE 2-9: *Differential Nonlinearity (DNL) vs. V_{DD}.*

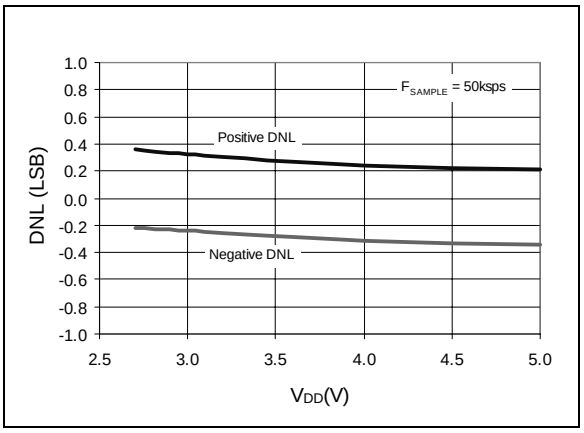


FIGURE 2-12: *Differential Nonlinearity (DNL) vs. V_{DD}.*

Note: Unless otherwise indicated, V_{DD} = 5V, V_{SS} = 0V, f_{SAMPLE} = 100ksps, f_{CLK} = 18* f_{SAMPLE}, T_A = 25°C

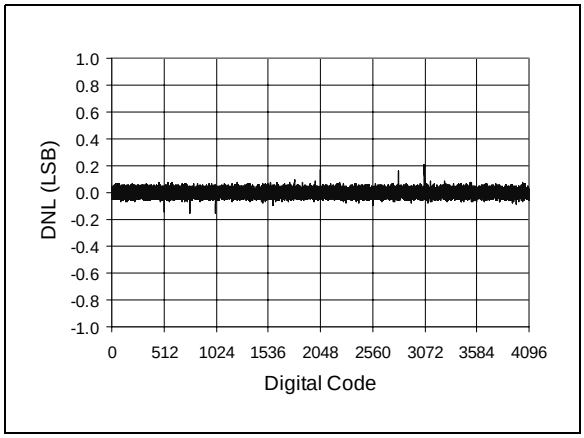


FIGURE 2-13: *Differential Nonlinearity (DNL) vs. Code (Representative Part).*

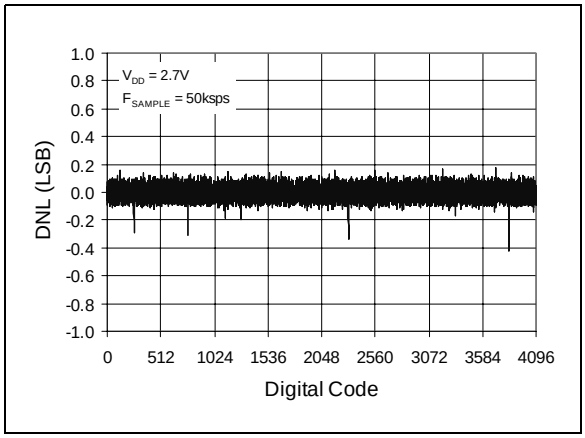


FIGURE 2-16: *Differential Nonlinearity (DNL) vs. Code (Representative Part, V_{DD} = 2.7V).*

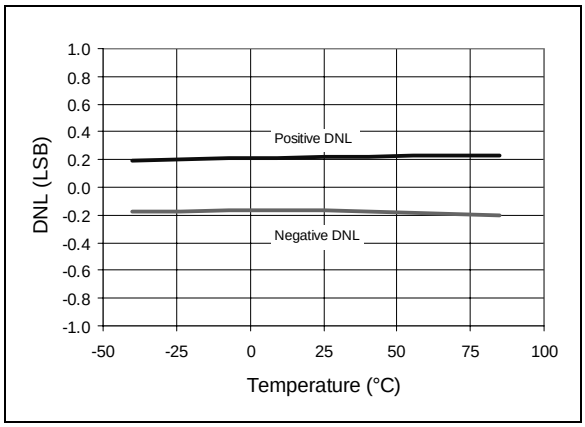


FIGURE 2-14: *Differential Nonlinearity (DNL) vs. Temperature.*

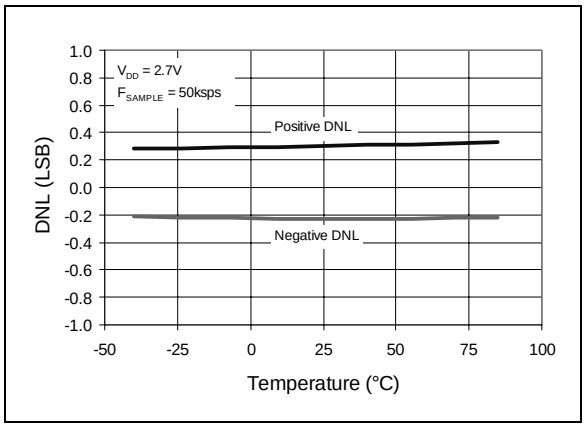


FIGURE 2-17: *Differential Nonlinearity (DNL) vs. Temperature (V_{DD} = 2.7V).*

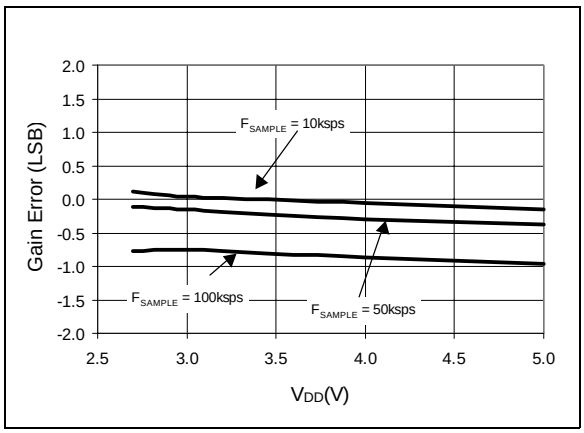


FIGURE 2-15: *Gain Error vs. V_{DD}.*

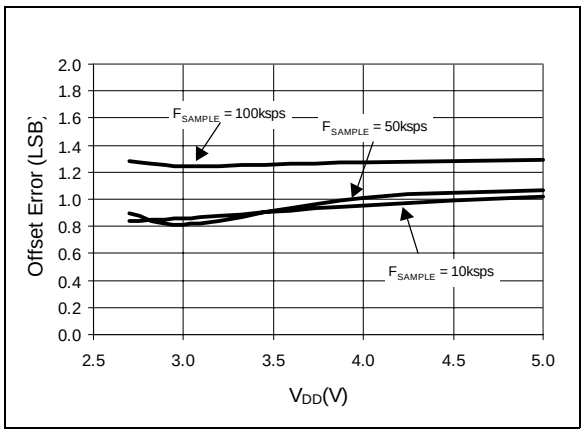


FIGURE 2-18: *Offset Error vs. V_{DD}.*

Note: Unless otherwise indicated, V_{DD} = 5V, V_{SS} = 0V, f_{SAMPLE} = 100ksps, f_{CLK} = 18* f_{SAMPLE}, T_A = 25°C

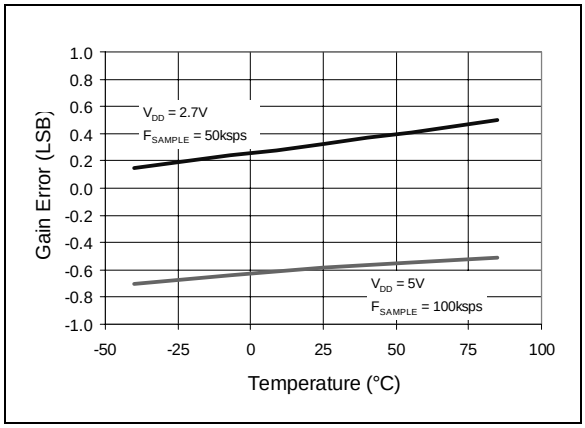


FIGURE 2-19: *Gain Error vs. Temperature.*

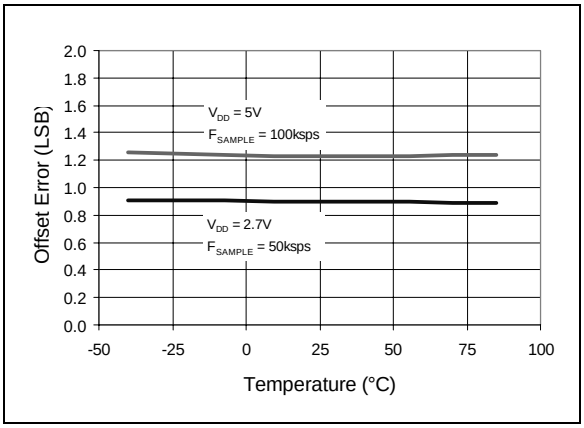


FIGURE 2-22: *Offset Error vs. Temperature.*

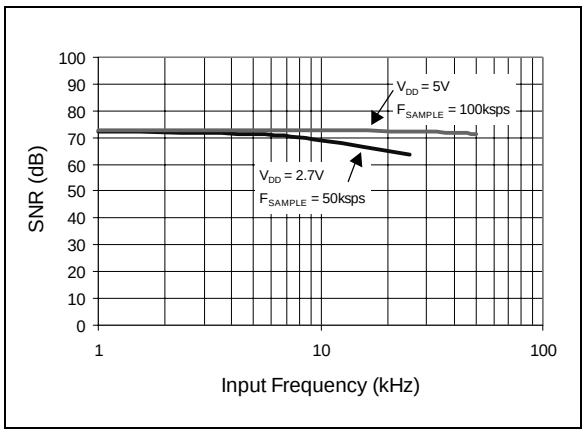


FIGURE 2-20: *Signal to Noise Ratio (SNR) vs. Input Frequency.*

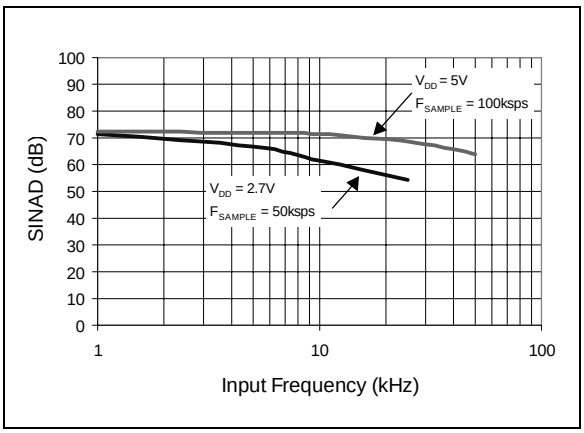


FIGURE 2-23: *Signal to Noise and Distortion (SINAD) vs. Input Frequency.*

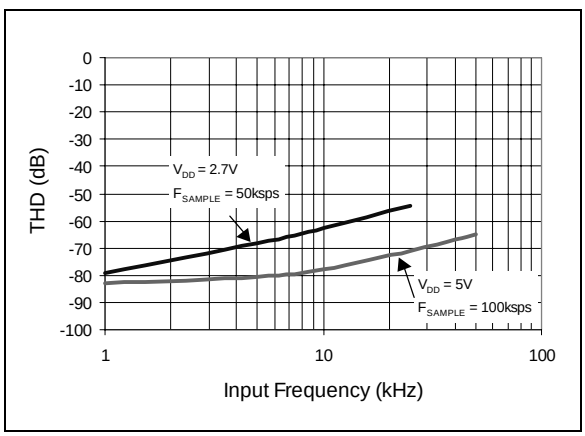


FIGURE 2-21: *Total Harmonic Distortion (THD) vs. Input Frequency.*

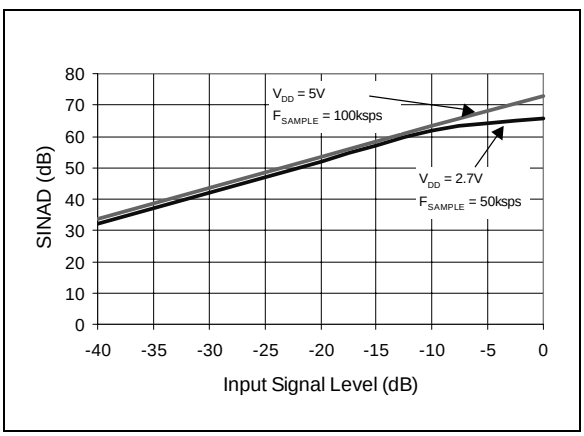


FIGURE 2-24: *Signal to Noise and Distortion (SINAD) vs. Signal Level.*

Note: Unless otherwise indicated, V_{DD} = 5V, V_{SS} = 0V, f_{SAMPLE} = 100ksps, f_{CLK} = 18* f_{SAMPLE}, T_A = 25°C

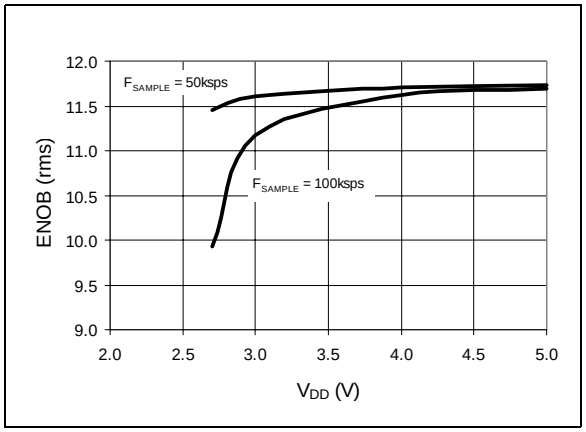


FIGURE 2-25: *Effective number of bits (ENOB) vs. V_{DD}.*

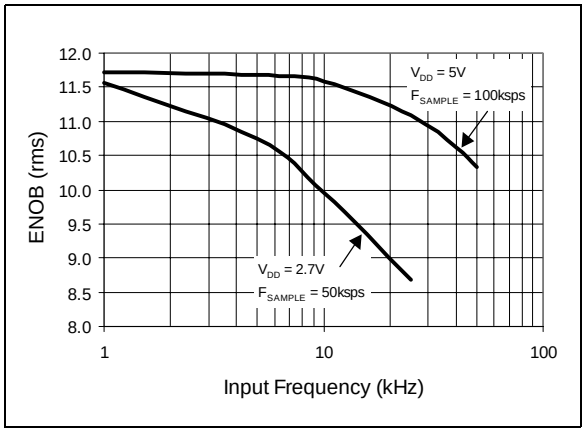


FIGURE 2-28: *Effective Number of Bits (ENOB) vs. Input Frequency.*

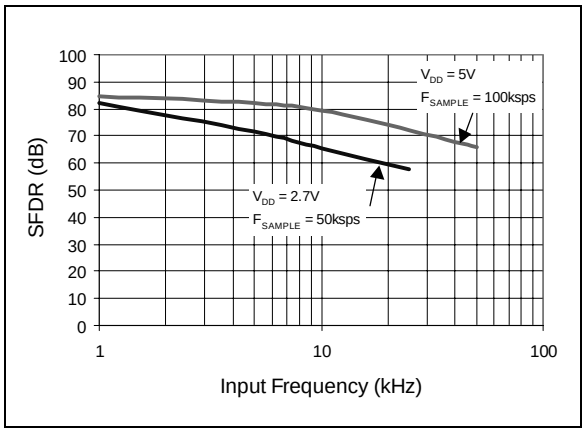


FIGURE 2-26: *Spurious Free Dynamic Range (SFDR) vs. Input Frequency.*

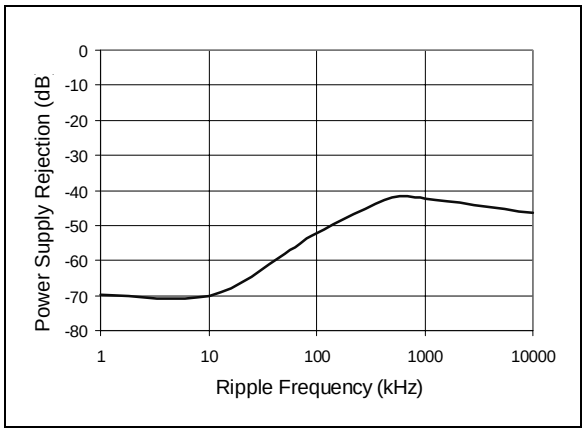


FIGURE 2-29: *Power Supply Rejection (PSR) vs. Ripple Frequency.*

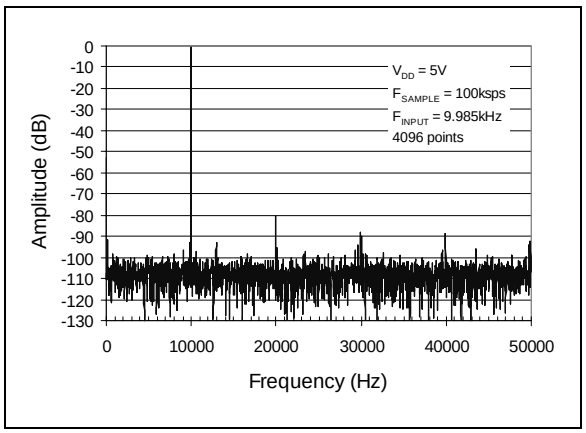


FIGURE 2-27: *Frequency Spectrum of 10kHz input (Representative Part).*

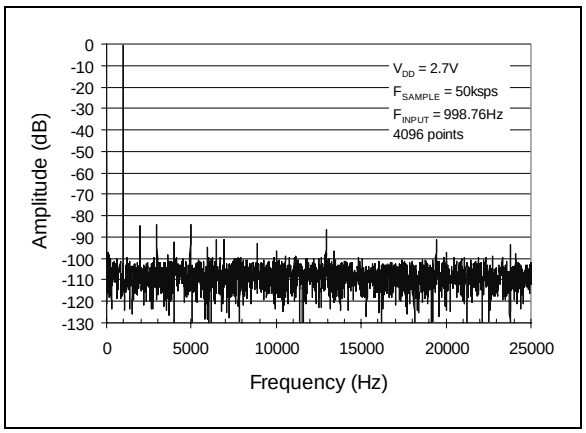


FIGURE 2-30: *Frequency Spectrum of 1kHz input (Representative Part, V_{DD} = 2.7V).*

Note: Unless otherwise indicated, V_{DD} = 5V, V_{SS} = 0V, f_{SAMPLE} = 100ksps, f_{CLK} = 18* f_{SAMPLE}, T_A = 25°C

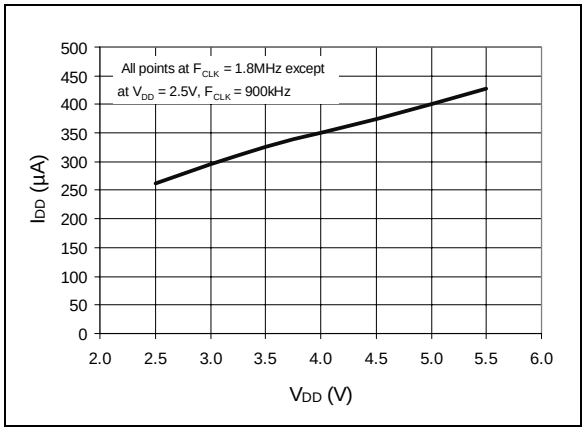


FIGURE 2-31: *I_{DD} vs. V_{DD}.*

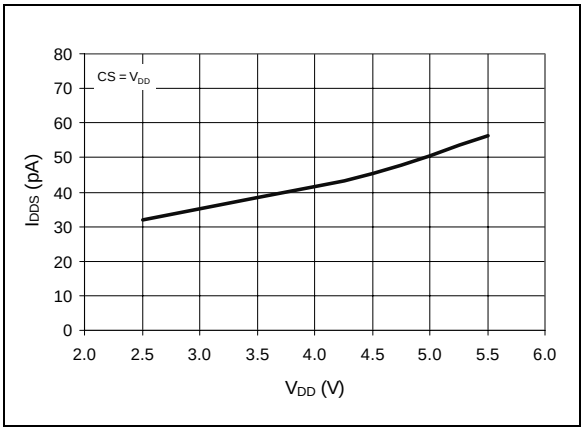


FIGURE 2-34: *I_{DDS} vs. V_{DD}.*

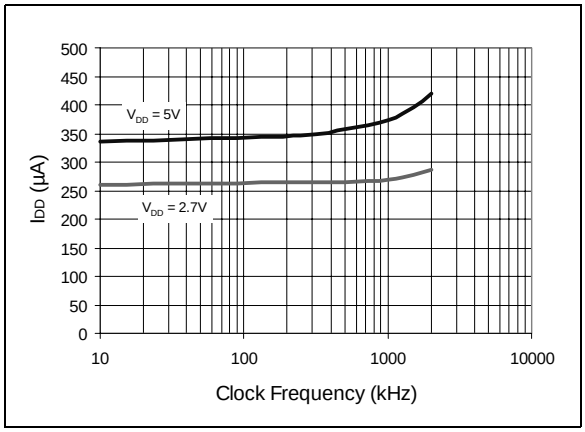


FIGURE 2-32: *I_{DD} vs. Clock Frequency.*

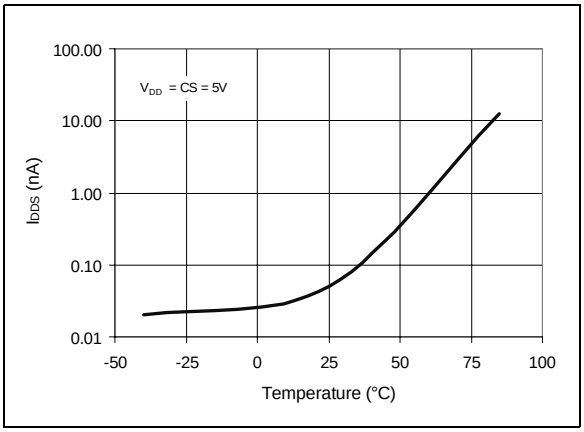


FIGURE 2-35: *I_{DDS} vs. Temperature.*

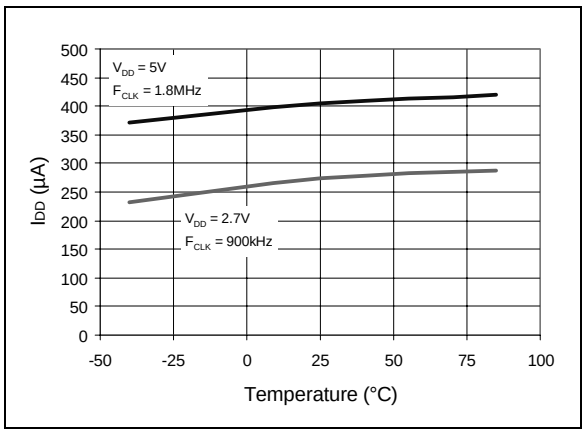


FIGURE 2-33: *I_{DD} vs. Temperature.*

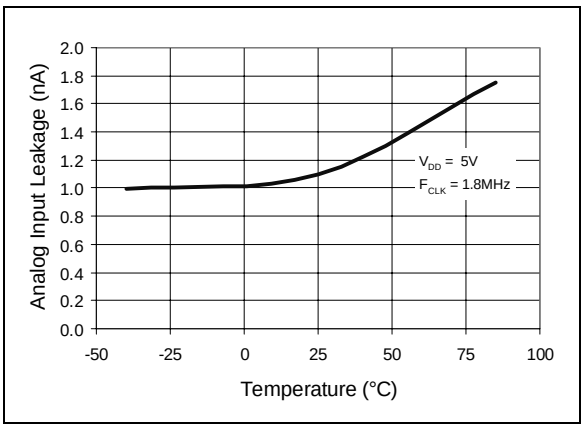


FIGURE 2-36: *Analog Input leakage current vs. Temperature.*

3.0 PIN DESCRIPTIONS

3.1 CH0/CH1

Analog inputs for channels 0 and 1 respectively. These channels can programmed to be used as two independent channels in single ended-mode or as a single pseudo-differential input where one channel is IN+ and one channel is IN-. See Section 5.0 for information on programming the channel configuration.

3.2 $\overline{CS}$/SHDN($\overline{Chip\ Select}$/Shutdown)

The $\overline{CS}$/SHDN pin is used to initiate communication with the device when pulled low and will end a conversion and put the device in low power standby when pulled high. The $\overline{CS}$/SHDN pin must be pulled high between conversions.

3.3 CLK (Serial Clock)

The SPI clock pin is used to initiate a conversion and to clock out each bit of the conversion as it takes place. See Section 6.2 for constraints on clock speed.

3.4 DIN (Serial Data Input)

The SPI port serial data input pin is used to clock in input channel configuration data.

3.5 DOUT (Serial Data output)

The SPI serial data output pin is used to shift out the results of the A/D conversion. Data will always change on the falling edge of each clock as the conversion takes place.

4.0 DEVICE OPERATION

The MCP3202 A/D Converter employs a conventional SAR architecture. With this architecture, a sample is acquired on an internal sample/hold capacitor for 1.5 clock cycles starting on the second rising edge of the serial clock after the start bit has been received. Following this sample time, the input switch of the converter opens and the device uses the collected charge on the internal sample and hold capacitor to produce a serial 12-bit digital output code. Conversion rates of 100ksps are possible on the MCP3202. See Section 6.2 for information on minimum clock rates. Communication with the device is done using a 3-wire SPI-compatible interface.

4.1 Analog Inputs

The MCP3202 device offers the choice of using the analog input channels configured as two single-ended inputs or a single pseudo-differential input. Configuration is done as part of the serial command before each conversion begins. When used in the psuedo-differential mode, CH0 and CH1 are programmed as the IN+ and IN- inputs as part of the command string transmitted to the device. The IN+ input can range from IN- to V_{REF} (V_{REF} + IN-). The IN- input is limited to ±100mV from the V_{SS} rail. The IN- input can be used to cancel small signal common-mode noise which is present on both the IN+ and IN- inputs.

For the A/D Converter to meet specification, the charge holding capacitor (C_{SAMPLE}) must be given enough time to acquire a 12-bit accurate voltage level during the 1.5 clock cycle sampling period. The analog input model is shown in Figure 4-1.

In this diagram, it is shown that the source impedance (R_S) adds to the internal sampling switch (R_{SS}) impedance, directly affecting the time that is required to charge the capacitor, C_{SAMPLE}. Consequently, larger source impedances increase the offset, gain, and integral linearity errors of the conversion.

Ideally, the impedance of the signal source should be near zero. This is achievable with an operational amplifier such as the MCP601 which has a closed loop output impedance of tens of ohms. The adverse affects of higher source impedances are shown in Figure 4-2.

When operating in the pseudo-differential mode, if the voltage level of IN+ is equal to or less than IN-, the resultant code will be 000h. If the voltage at IN+ is equal to or greater than {[V_{REF} + (IN-)] - 1 LSB}, then the output code will be FFFh. If the voltage level at IN- is more than 1 LSB below V_{SS}, then the voltage level at the IN+ input will have to go below V_{SS} to see the 000h output code. Conversely, if IN- is more than 1 LSB above V_{SS}, then the FFFh code will not be seen unless the IN+ input level goes above V_{REF} level.

4.2 Digital Output Code

The digital output code produced by an A/D Converter is a function of the input signal and the reference voltage. For the MCP3202, V_{DD} is used as the reference voltage. As the V_{DD} level is reduced, the LSB size is reduced accordingly. The theoretical digital output code produced by the A/D Converter is shown below.

$$Digital\ Output\ Code = \frac{4096 * V_{IN}}{V_{DD}}$$

where:

V_{IN} = *analog input voltage*

V_{DD} = *supply voltage*

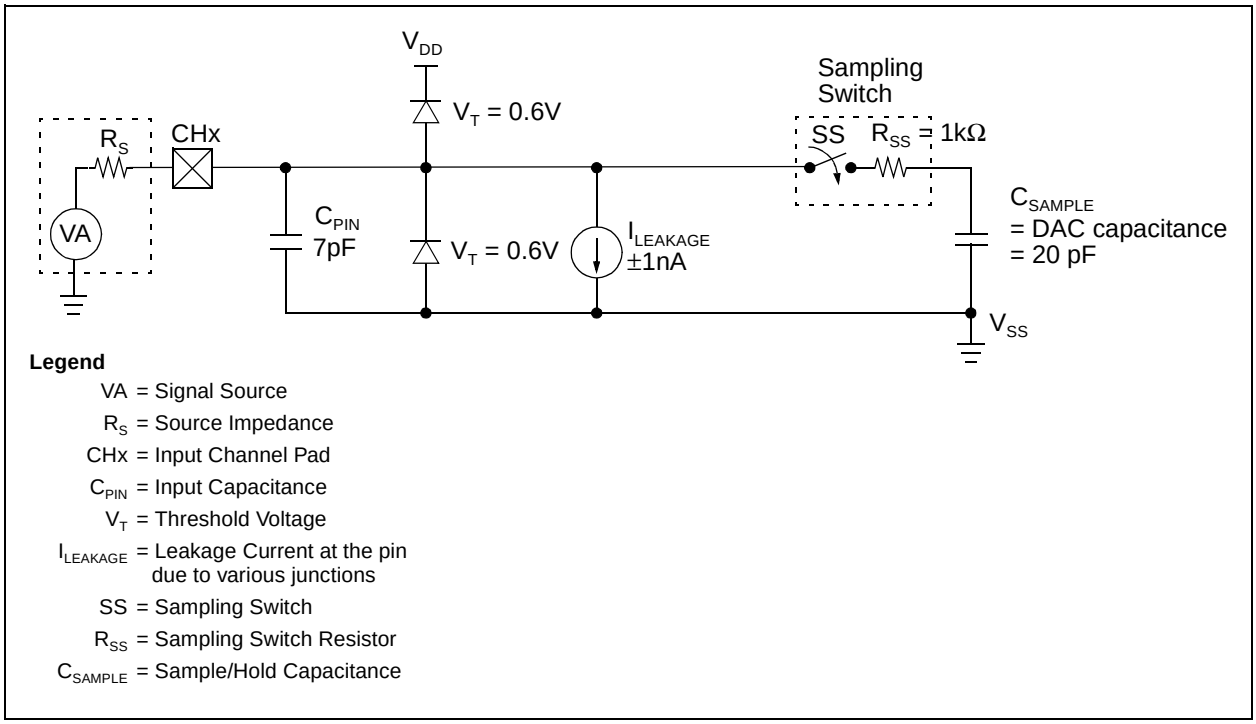


FIGURE 4-1: *Analog Input Model.*

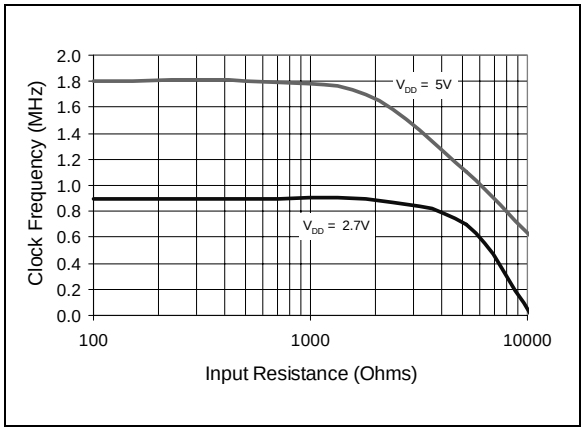


FIGURE 4-2: *Maximum Clock Frequency vs. Input Resistance (R_S) to maintain less than a 0.1 LSB deviation in INL from nominal conditions.*

5.0 SERIAL COMMUNICATIONS

5.1 Overview

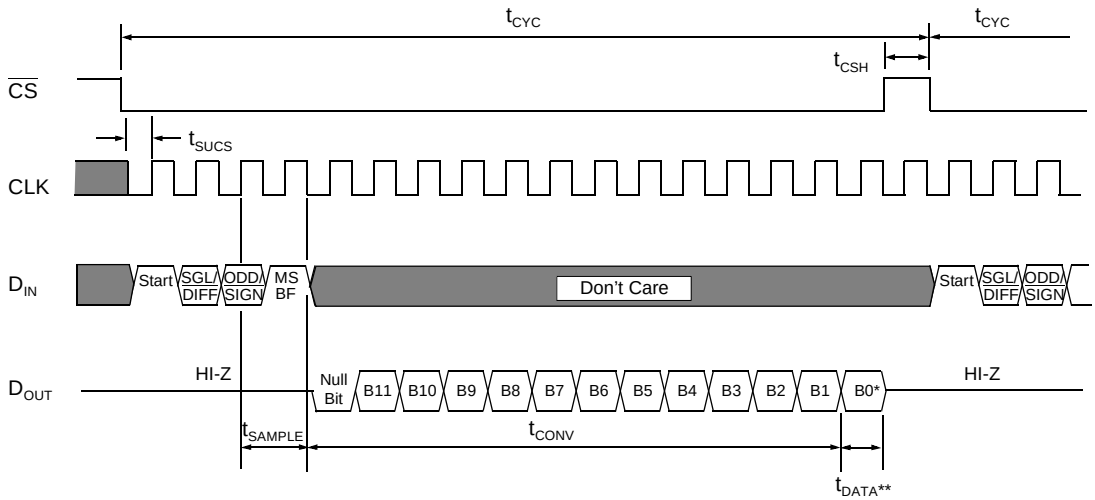
Communication with the MCP3202 is done using a standard SPI-compatible serial interface. Initiating communication with the device is done by bringing the $\overline{CS}$ line low. See Figure 5-1. If the device was powered up with the $\overline{CS}$ pin low, it must be brought high and back low to initiate communication. The first clock received with $\overline{CS}$ low and DIN high will constitute a start bit. The SGL/$\overline{DIFF}$ bit and the ODD/$\overline{SIGN}$ bit follow the start bit and are used to select the input channel configuration. The SGL/$\overline{DIFF}$ is used to select single ended or psuedo-differential mode. The ODD/$\overline{SIGN}$ bit selects which channel is used in single ended mode, and is used to determine polarity in pseudo-differential mode. Following the ODD/$\overline{SIGN}$ bit, the MSBF bit is transmitted to and is used to enable the LSB first format for the device. If the MSBF bit is low, then the data will come from the device in MSB first format and any further clocks with $\overline{CS}$ low will cause the device to output zeros. If the MSBF bit is high, then the device will output the converted word LSB first *after* the word has been transmitted in the MSB first format. See Figure 5-2. Table 5-1 shows the configuration bits for the MCP3202. The device will begin to sample the analog input on the second rising edge of the clock, after the start bit has been received. The sample period will end on the falling edge of the third clock following the start bit.

On the falling edge of the clock for the MSBF bit, the device will output a low null bit. The next sequential 12 clocks will output the result of the conversion with MSB first as shown in Figure 5-1. Data is always output from the device on the falling edge of the clock. If all 12 data bits have been transmitted and the device continues to receive clocks while the $\overline{CS}$ is held low, (and MSBF = 1), the device will output the conversion result LSB first as shown in Figure 5-2. If more clocks are provided to the device while $\overline{CS}$ is still low (after the LSB first data has been transmitted), the device will clock out zeros indefinitely.

If necessary, it is possible to bring $\overline{CS}$ low and clock in leading zeros on the D_{IN} line before the start bit. This is often done when dealing with microcontroller-based SPI ports that must send 8 bits at a time. Refer to Section 6.1 for more details on using the MCP3202 devices with hardware SPI ports.

	CONFIG BITS		CHANNEL SELECTION		GND
	SGL/$\overline{DIFF}$	ODD/$\overline{SIGN}$	0	1	
SINGLE ENDED MODE	1	0	+		-
	1	1		+	-
PSEUDO-DIFFERENTIAL MODE	0	0	IN+	IN-	
	0	1	IN-	IN+	

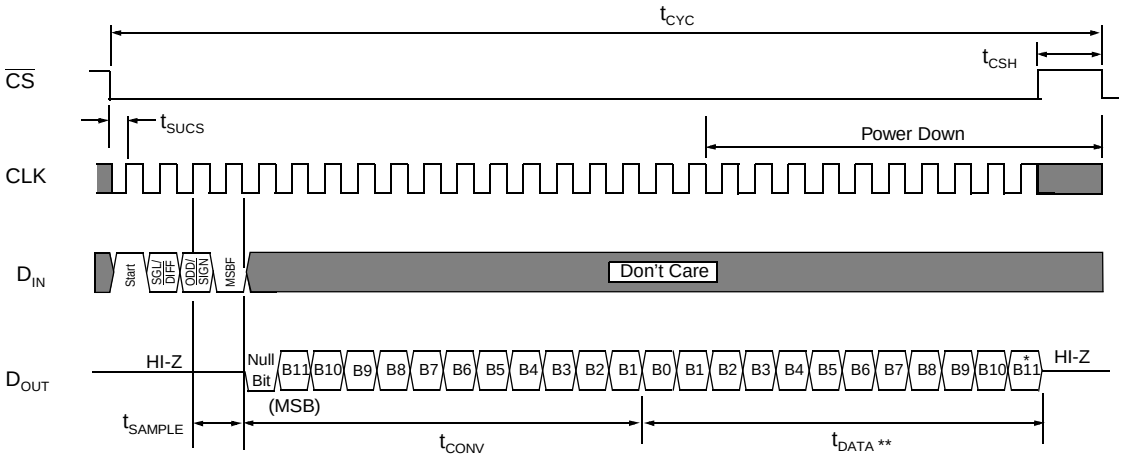
TABLE 5-1: *Configuration Bits for the MCP3202.*



* After completing the data transfer, if further clocks are applied with $\overline{CS}$ low, the A/D Converter will output zeros indefinitely. See Figure 5-2 below for details on obtaining LSB first data.

** t_{DATA}: during this time, the bias current and the comparator power down while the reference input becomes a high impedance node, leaving the CLK running to clock out the LSB-first data or zeros.

FIGURE 5-1: *Communication with the MCP3202 using MSB first format only.*



* After completing the data transfer, if further clocks are applied with $\overline{CS}$ low, the A/D Converter will output zeros indefinitely.

** t_{DATA}: During this time, the bias circuit and the comparator power down while the reference input becomes a high impedance node, leaving the CLK running to clock out LSB first data or zeroes.

FIGURE 5-2: *Communication with MCP3202 using LSB first format.*

6.0 APPLICATIONS INFORMATION

6.1 Using the MCP3202 with Microcontroller (MCU) SPI Ports

With most microcontroller SPI ports, it is required to send groups of eight bits. It is also required that the microcontroller SPI port be configured to clock out data on the falling edge of clock and latch data in on the rising edge. Depending on how communication routines are used, it is very possible that the number of clocks required for communication will not be a multiple of eight. Therefore, it may be necessary for the MCU to send more clocks than are actually required. This is usually done by sending 'leading zeros' before the start bit, which are ignored by the device. As an example, Figure 6-1 and Figure 6-2 show how the MCP3202 can be interfaced to a MCU with a hardware SPI port. Figure 6-1 depicts the operation shown in SPI Mode 0,0, which requires that the SCLK from the MCU idles in the 'low' state, while Figure 6-2 shows the similar case of SPI Mode 1,1 where the clock idles in the 'high' state.

As shown in Figure 6-1, the first byte transmitted to the A/D Converter contains seven leading zeros before the start bit. Arranging the leading zeros this way produces the output 12 bits to fall in positions easily manipulated by the MCU. The MSB is clocked out of the A/D Converter on the falling edge of clock number 12. After the second eight clocks have been sent to the device, the MCU receive buffer will contain three unknown bits (the output is at high impedance until the null bit is clocked out), the null bit and the highest order four bits of the conversion. After the third byte has been sent to the device, the receive register will contain the lowest order eight bits of the conversion results. Easier manipulation of the converted data can be obtained by using this method.

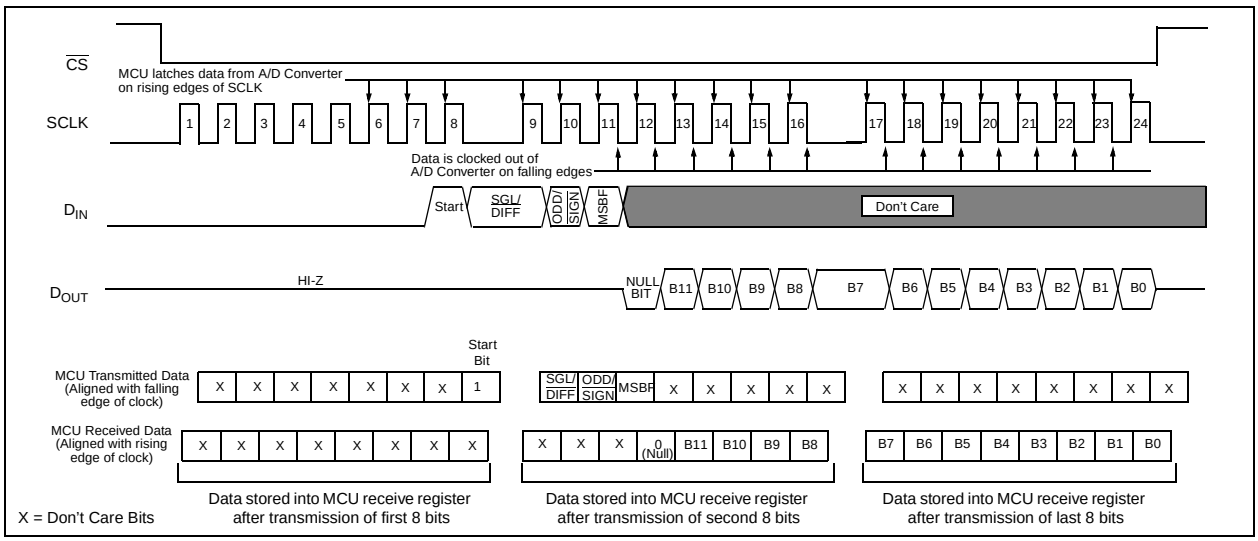


FIGURE 6-1: *SPI Communication using 8-bit segments (Mode 0,0: SCLK idles low).*

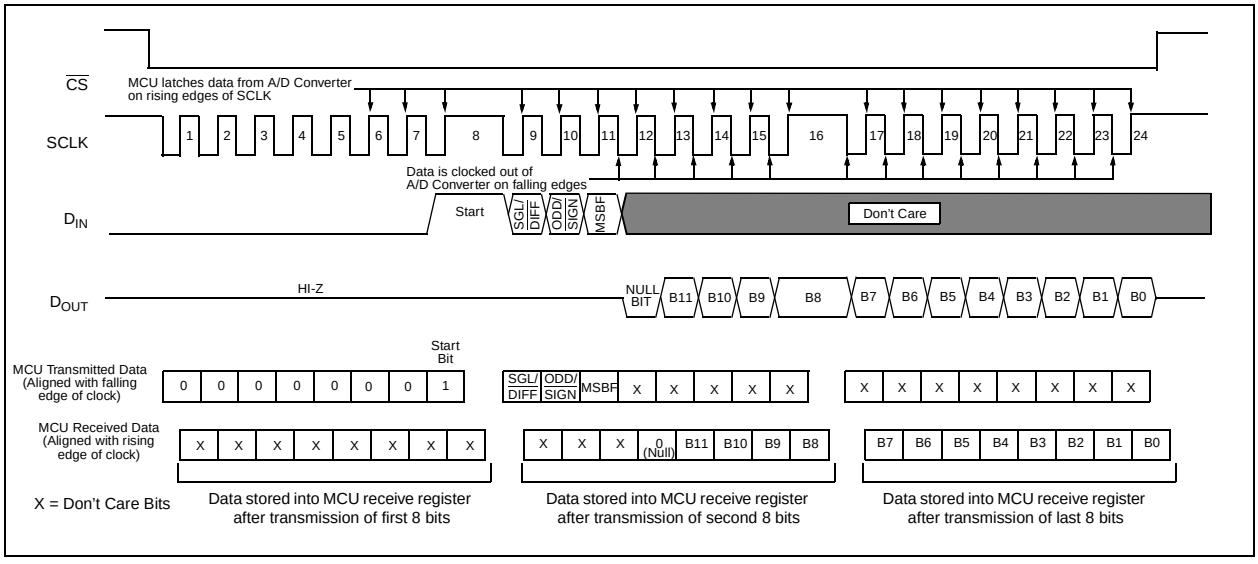


FIGURE 6-2: *SPI Communication using 8-bit segments (Mode 1,1: SCLK idles high).*

6.2 Maintaining Minimum Clock Speed

When the MCP3202 initiates the sample period, charge is stored on the sample capacitor. When the sample period is complete, the device converts one bit for each clock that is received. It is important for the user to note that a slow clock rate will allow charge to bleed off the sample cap while the conversion is taking place. At 85°C (worst case condition), the part will maintain proper charge on the sample capacitor for at least 1.2ms after the sample period has ended. This means that the time between the end of the sample period and the time that all 12 data bits have been clocked out must not exceed 1.2ms (effective clock frequency of 10kHz). Failure to meet this criteria may induce linearity errors into the conversion outside the rated specifications. It should be noted that during the entire conversion cycle, the A/D Converter does not require a constant clock speed or duty cycle, as long as all timing specifications are met.

6.3 Buffering/Filtering the Analog Inputs

If the signal source for the A/D Converter is not a low impedance source, it will have to be buffered or inaccurate conversion results may occur. It is also recommended that a filter be used to eliminate any signals that may be aliased back into the conversion results. This is illustrated in Figure 6-3 below where an op amp is used to drive the analog input of the MCP3202. This amplifier provides a low impedance output for the converter input and a low pass filter, which eliminates unwanted high frequency noise.

Low pass (anti-aliasing) filters can be designed using Microchip's interactive **FilterLab™** software. **FilterLab** will calculate capacitor and resistor values, as well as, determine the number of poles that are required for the application. For more information on filtering signals, see the application note AN699 *"Anti-Aliasing Analog Filters for Data Acquisition Systems."*

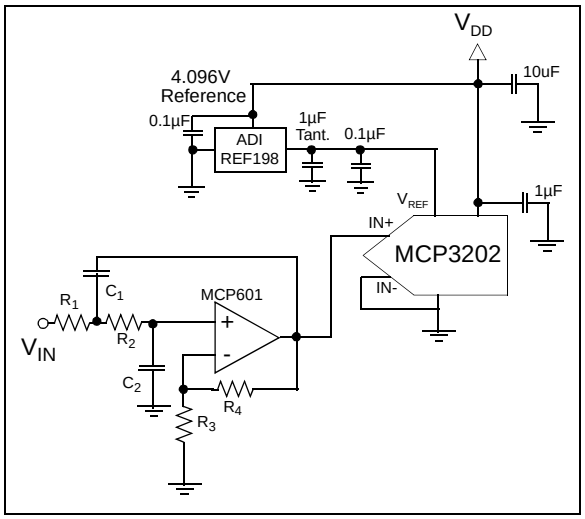


FIGURE 6-3: *The MCP601 Operational Amplifier is used to implement a 2nd order anti-aliasing filter for the signal being converted by the MCP3202.*

6.4 Layout Considerations

When laying out a printed circuit board for use with analog components, care should be taken to reduce noise wherever possible. A bypass capacitor should always be used with this device and should be placed as close as possible to the device pin. A bypass capacitor value of 1µF is recommended.

Digital and analog traces should be separated as much as possible on the board and no traces should run underneath the device or the bypass capacitor. Extra precautions should be taken to keep traces with high frequency signals (such as clock lines) as far as possible from analog traces.

Use of an analog ground plane is recommended in order to keep the ground potential the same for all devices on the board. Providing V_{DD} connections to devices in a "star" configuration can also reduce noise by eliminating current return paths and associated errors. See Figure 6-4. For more information on layout tips when using A/D Converters, refer to AN688 *"Layout Tips for 12-Bit A/D Converter Applications"*.

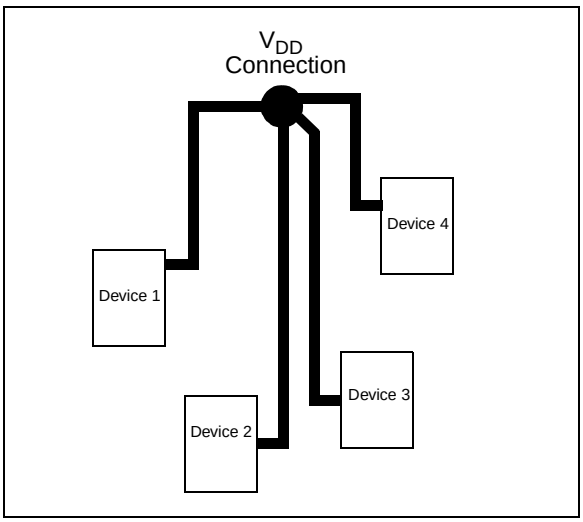


FIGURE 6-4: *V_{DD} traces arranged in a 'Star' configuration in order to reduce errors caused by current return paths.*

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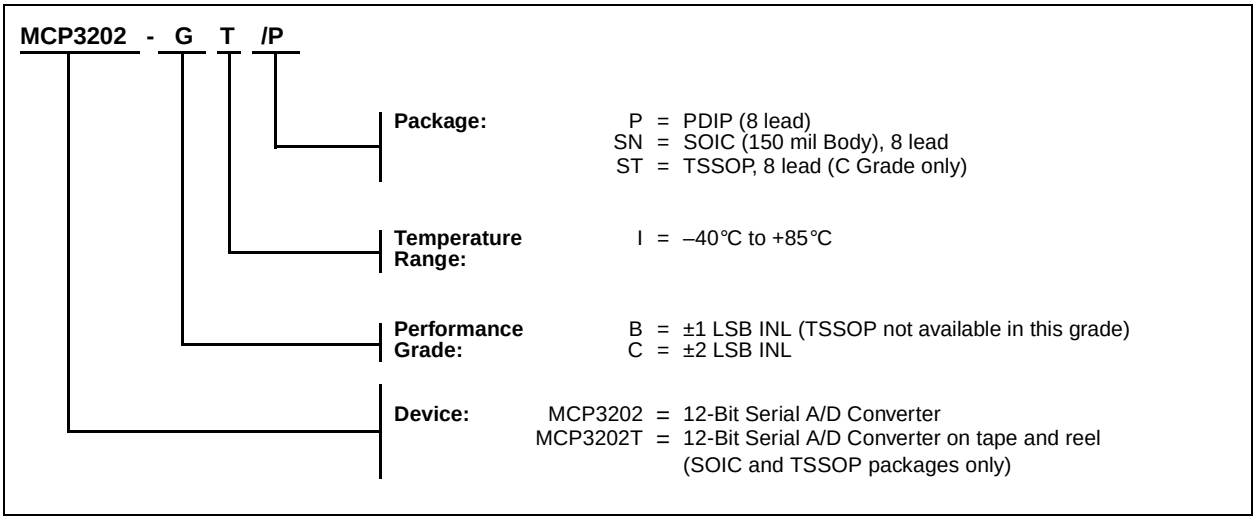
MCP3202 PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



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