FSDM311

Green Mode Fairchild Power Switch (FPS™)

Features

- Internal Avalanche Rugged Sense FET
- Precision Fixed Operating Frequency (67KHz)
- Consumes Under 0.2W at 265VAC & No Load with Advanced Burst-Mode Operation
- Internal Start-up Circuit
- Pulse-by-Pulse Current Limiting
- Over Voltage Protection (OVP)
- Over Load Protection (OLP)
- Internal Thermal Shutdown Function (TSD)
- Auto-Restart Mode
- Under Voltage Lockout (UVLO) with Hysteresis
- Built-in Soft Start
- Secondary Side Regulation

OUTPUT POWER TABLE		
PRODUCT	Open Frame(1)	
	230VAC±15%(2)	85-265VAC
FSDM311	13W	8W
FSDM311L	13W	8W

Notes:
1. Maximum practical continuous power in an open frame design with sufficient drain pattern as a heat sinker, at 50°C ambient.
2. 230 VAC or 100/115 VAC with doubler.

Applications

- Charger & Adapter for Mobile Phone, PDA & MP3
- Auxiliary Power for White Goods, PC, C-TV & Monitor

Related Application Notes

- AN-4137, 4141, 4147(Flyback) / AN-4134(Forward) / AN-4138(Charger)

Description

The FSDM311 consists of an integrated Pulse Width Modulator (PWM) and Sense FET, and is specifically designed for high performance off-line Switch Mode Power Supplies (SMPS) with minimal external components. This device is an integrated high voltage power switching regulator which combines an VDMOS Sense FET with a voltage mode PWM control block. The integrated PWM controller features include: a fixed oscillator, Under Voltage Lock Out (UVLO) protection, Leading Edge Blanking (LEB), an optimized gate turn-on/turn-off driver, Thermal Shut Down (TSD) protection and temperature compensated precision current sources for loop compensation and fault protection circuitry. When compared to a discrete MOSFET and controller or RCC switching converter solution, the FSDM311 device reduces total component count, design size, weight while increasing efficiency, productivity and system reliability. This device provides a basic platform that is well suited for the design of cost-effective flyback converters.

Typical Circuit

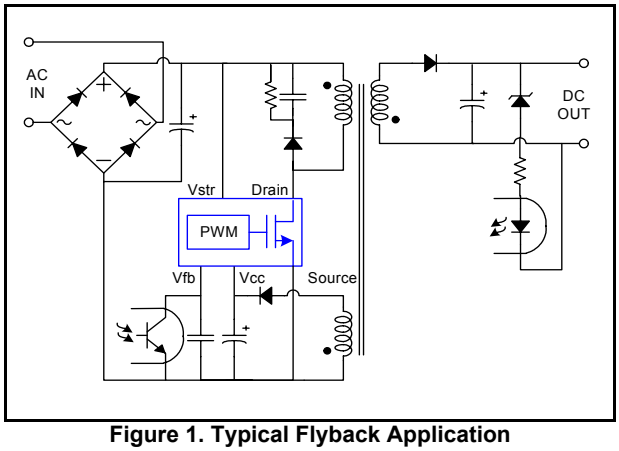


Figure 1. Typical Flyback Application

Internal Block Diagram

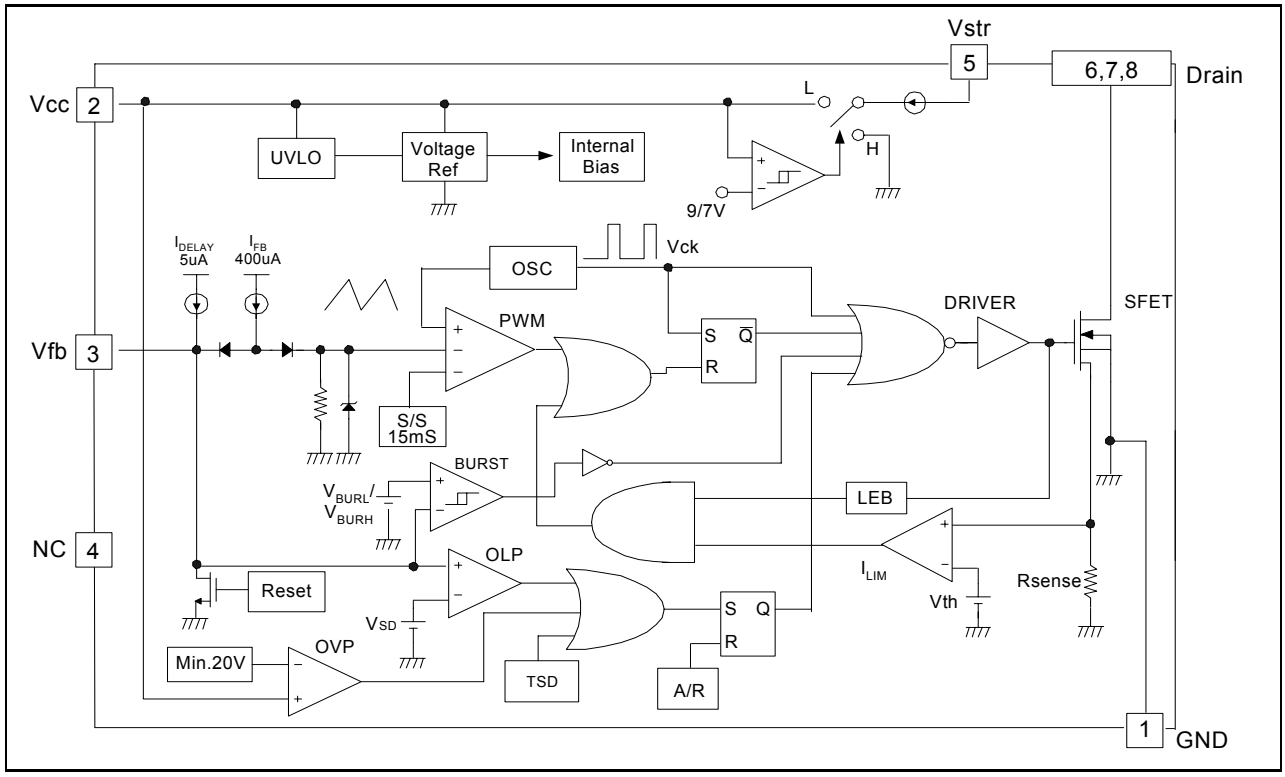


Figure 2. Functional Block Diagram of FSDM311

Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	GND	Sense FET source terminal on primary side and internal control ground.
2	Vcc	Positive supply voltage input. Although connected to an auxiliary transformer winding, current is supplied from pin 5 (Vstr) via an internal switch during startup (see Internal Block Diagram section). It is not until Vcc reaches the UVLO upper threshold (9V) that the internal start-up switch opens and device power is supplied via the auxiliary transformer winding.
3	Vfb	The feedback voltage pin is the inverting input to the PWM comparator with its normal input level lies between 0.5V and 2.5V. It has a 0.4mA current source connected internally while a capacitor and optocoupler are typically connected externally. A feedback voltage of 4.5V triggers over load protection (OLP). There is a time delay while charging external capacitor Cfb from 3V to 4.5V using an internal 5uA current source. This time delay prevents false triggering under transient conditions, but still allows the protection mechanism to operate under true overload conditions.
5	Vstr	This pin connects directly to the rectified AC line voltage source. At start up the internal switch supplies internal bias and charges an external storage capacitor placed between the Vcc pin and ground. Once the Vcc reaches 9V, the internal switch is opened.
6, 7, 8	Drain	The drain pins are designed to connect directly to the primary lead of the transformer and are capable of switching a maximum of 650V. Minimizing the length of the trace connecting these pins to the transformer will decrease leakage inductance.

Pin Configuration

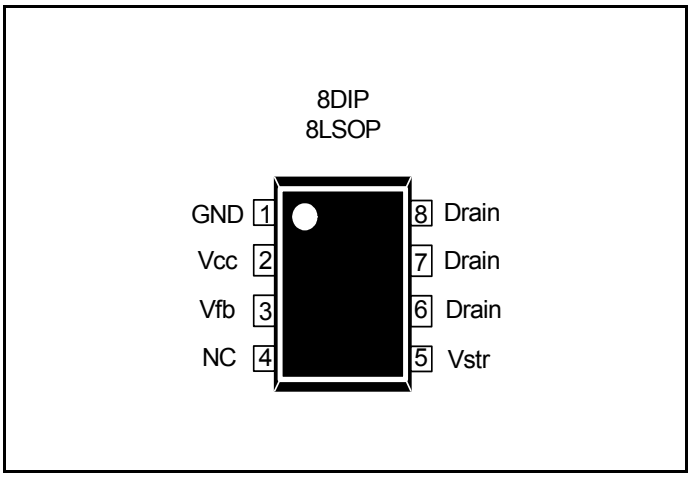


Figure 3. Pin Configuration (Top View)

Absolute Maximum Ratings

(Ta=25°C, unless otherwise specified)

Characteristic	Symbol	Value	Unit
Drain Pin Voltage	V_{DRAIN}	650	V
Vstr Pin Voltage	V_{STR}	650	V
Drain-Gate Voltage	V_{DG}	650	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current Pulsed(1)	I_{DM}	1.5	A
Continuous Drain Current (Tc=25℃)	I_D	0.5	A
Continuous Drain Current (Tc=100℃)	I_D	0.32	A
Single Pulsed Avalanche Energy(2)	E_{AS}	10	mJ
Supply Voltage	V_{CC}	20	V
Feedback Voltage Range	V_{FB}	-0.3 to V_{STOP}	V
Total Power Dissipation	P_D	1.40	W
Operating Junction Temperature	T_J	Internally limited	°C
Operating Ambient Temperature	T_A	-25 to +85	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Note:

1. Repetitive rating: Pulse width is limited by maximum junction temperature
2. L = 24mH, starting Tj = 25°C

Thermal Impedance

(Ta=25°C, unless otherwise specified)

Parameter	Symbol	Value	Unit
8DIP			
Junction-to-Ambient Thermal(1)	θ_{JA}	88.84	°C/W
Junction-to-Case Thermal(2)	θ_{JC}	13.94	°C/W

Note:

1. Free standing with no heatsink; Without copper clad.
   / Measurement Condition : Just before junction temperature T_J enters into OTP.
2. Measured on the DRAIN pin close to plastic interface.

- all items are tested with the standards JESD 51-2 and 51-10 (DIP).

Electrical Characteristics

(Ta = 25°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SENSE FET SECTION						
Zero-Gate-Voltage Drain Current	I_{DSS}	V_{DS}=650V, V_{GS}=0V	-	-	25	μA
		V_{DS}=520V, V_{GS}=0V, T_C=125°C	-	-	200	
Drain-Source On-State Resistance(1)	$R_{DS(ON)}$	V_{GS}=10V, I_D=0.5A	-	14	19	Ω
Forward Trans-Conductance	g_{fs}	V_{DS}=50V, I_D=0.5A	1.0	1.3	-	S
Input Capacitance	C_{ISS}	V_{GS}=0V, V_{DS}=25V, f=1MHz	-	162	-	pF
Output Capacitance	C_{OSS}		-	18	-	
Reverse Transfer Capacitance	C_{RSS}		-	3.8	-	
Turn-On Delay Time	$t_{d(on)}$	V_{DS}=325V, I_D=1.0A	-	9.5	-	ns
Rise Time	t_r		-	19	-	
Turn-Off Delay Time	$t_{d(off)}$		-	33	-	
Fall Time	t_f		-	42	-	
Total Gate Charge	Q_g	V_{GS}=10V, I_D=1.0A, V_{DS}=325V	-	7.0	-	nC
Gate-Source Charge	Q_{gs}		-	3.1	-	
Gate-Drain (Miller) Charge	Q_{gd}		-	0.4	-	
CONTROL SECTION						
Switching Frequency	f_{OSC}		61	67	73	KHz
Switching Frequency Variation(2)	Δf_{OSC}	-25°C ≤ Ta ≤ 85°C	-	±5	±10	%
Maximum Duty Cycle	D_{MAX}		60	67	74	%
UVLO Threshold Voltage	V_{START}	V_{FB}=GND	8	9	10	V
	V_{STOP}	V_{FB}=GND	6	7	8	V
Feedback Source Current	I_{FB}	0V ≤ V_{FB} ≤ 3V	0.35	0.40	0.45	mA
Internal Soft Start Time	$t_{S/S}$		10	15	20	ms
Reference Voltage(3)	V_{REF}		4.2	4.5	4.8	V
Reference Voltage Varaiation with Temperature(2)(3)	$\Delta V_{REF}/\Delta T$	-25°C ≤ Ta ≤ 85°C	-	0.3	0.6	mV/°C
BURST MODE SECTION						
Burst Mode Voltage	V_{BURH}	Tj=25°C	0.6	0.7	0.8	V
	V_{BURL}		0.45	0.55	0.65	V
	$V_{BUR(HYS)}$	Hysteresis	-	150	-	mV
PROTECTION SECTION						
Peak Current Limit	I_{LIM}		0.475	0.55	0.625	A
Thermal Shutdown Temperature(3)	T_{SD}		125	145	-	°C
Shutdown Feedback Voltage	V_{SD}		4.0	4.5	5.0	V
Over Voltage Protection	V_{OVP}		20	-	-	V
Shutdown Delay Current	I_{DELAY}	3V ≤ V_{FB} ≤ V_{SD}	4	5	6	μA
TOTAL DEVICE SECTION						
Operating Supply Current (control part only)	I_{OP}	V_{CC} ≤ 16V	-	1.5	3.0	mA
Start-Up Charging Current	I_{CH}	V_{CC}=0V , V_{STR}=50V	450	550	650	μA

Note:

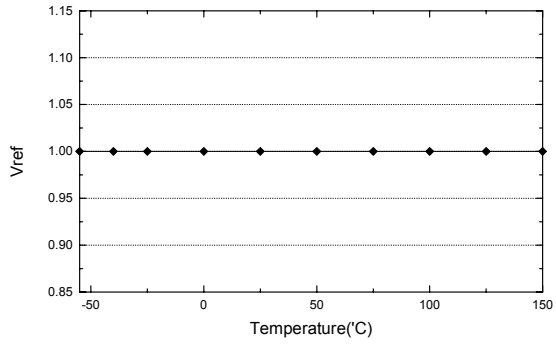
1. Pulse test: Pulse width ≤ 300us, duty ≤ 2%
2. These parameters, although guaranteed, are tested in EDS (wafer test) process
3. These parameters, although guaranteed, are not 100% tested in production

Comparison Between FSDH0165 and FSDM311

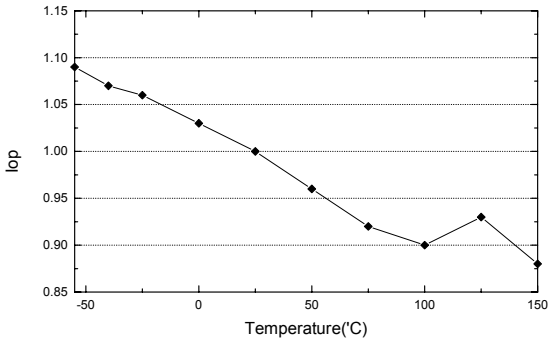
Function	FSDH0165	FSDM311	FSDM311 Advantages
Soft-Start	not applicable	15ms	• Gradually increasing current limit during soft-start further reduces peak current and voltage stresses • Eliminates external components used for soft-start in most applications • Reduces or eliminates output overshoot
Burst Mode Operation	not applicable	Built into controller	• Improves light load efficiency • Reduces power consumption at no-load • Transformer audible noise reduction
Drain Creepage at Package	1.02mm	3.56mm DIP 3.56mm LSOP	• Greater immunity to arcing provoked by dust, debris and other contaminants

Typical Performance Characteristics (Control Part)

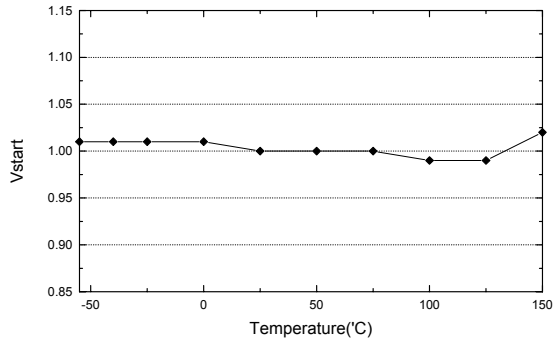
(These characteristic graphs are normalized at Ta = 25°C)



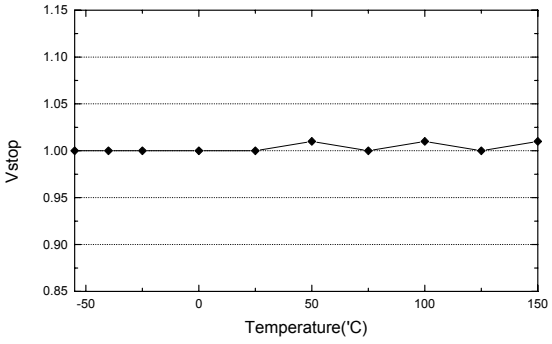
Reference Voltage (V_{REF}) vs. Ta



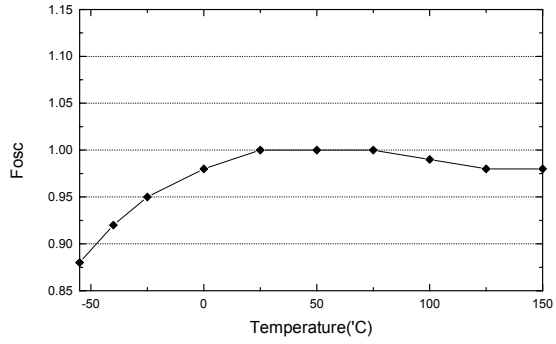
Operating Supply Current (I_{OP}) vs. Ta



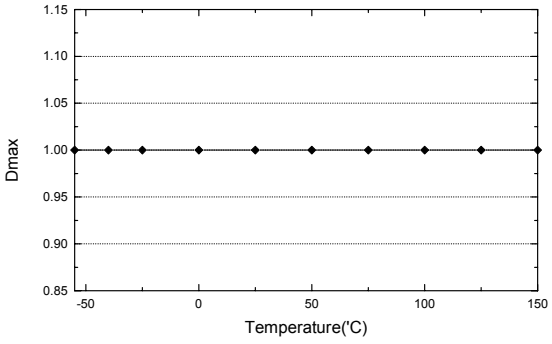
Start Threshold Voltage (V_{START}) vs. Ta



Stop Threshold Voltage (V_{STOP}) vs. Ta

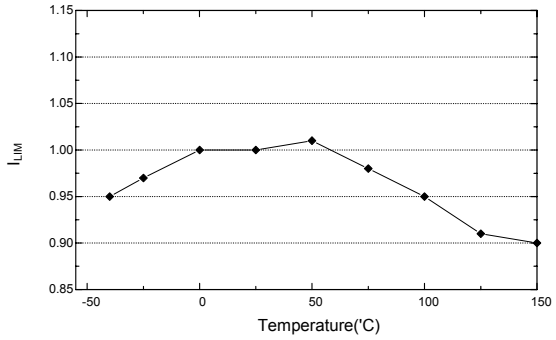


Operating Frequency (F_{OSC}) vs. Ta

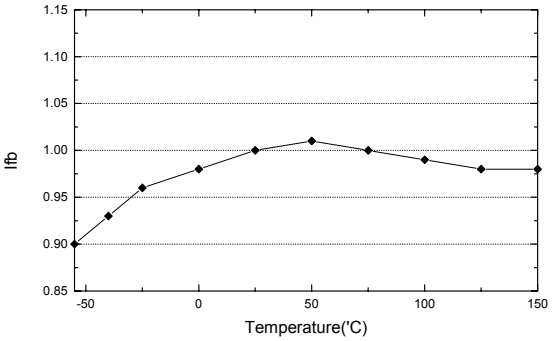


Maximum Duty Cycle (D_{MAX}) vs. Ta

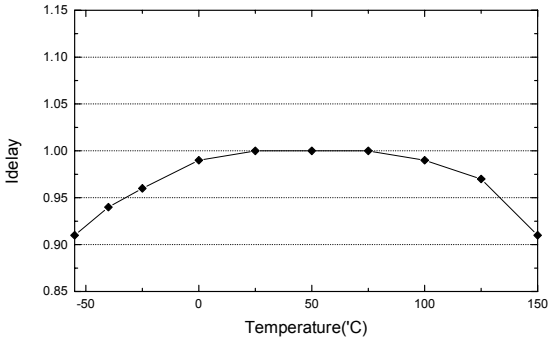
Typical Performance Characteristics (Continued)



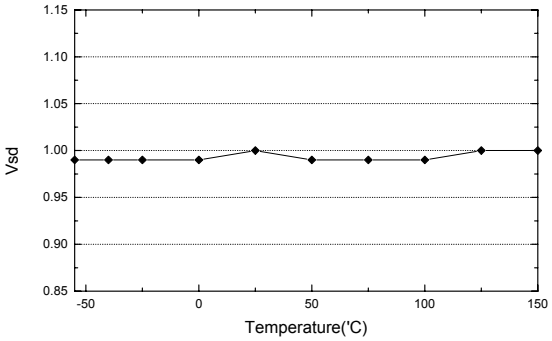
Peak Current Limit (I_{LIM}) vs. Ta



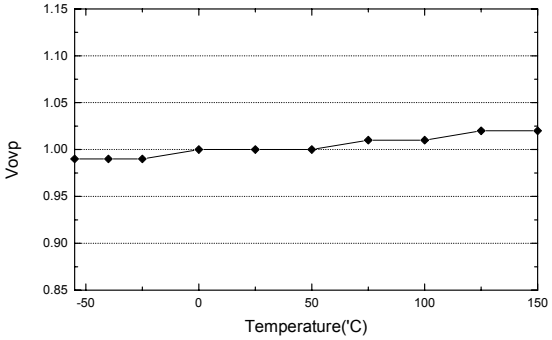
Feedback Source Current (I_{FB}) vs. Ta



Shutdown Delay Current (I_{DELAY}) vs. Ta



Shutdown Feedback Voltage (V_{SD}) vs. Ta



Over Voltage Protection (V_{OVP}) vs. Ta

Functional Description

1. Startup : At startup, the internal high voltage current source supplies the internal bias and charges the external Vcc capacitor as shown in Figure 4. In the case of the FSDM311, when Vcc reaches 9V the device starts switching and the internal high voltage current source is disabled. The device is in normal operation provided that Vcc does not drop below 7V. After startup the bias is supplied from the auxiliary transformer winding.

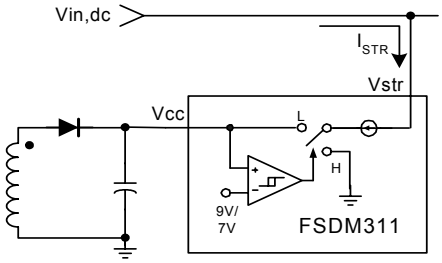


Figure 4. Internal Startup Circuit

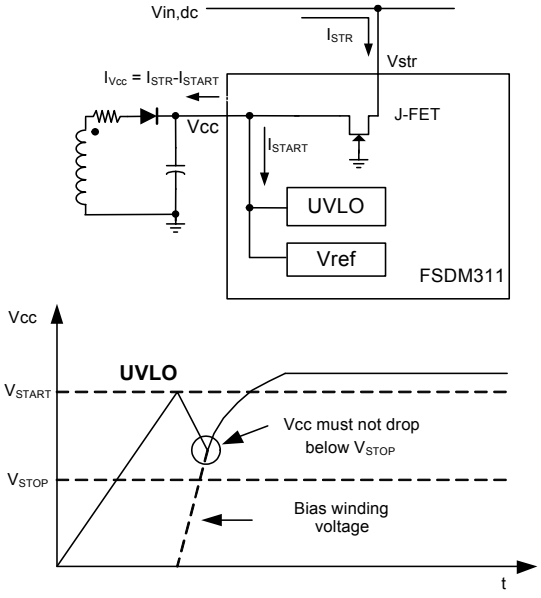


Figure 5. Charging Vcc Capacitor through Vstr

Calculating the Vcc capacitor is an important step to design with the FSDM311. At initial start-up in the FSDM311, the maximum value of start operating current I_{START} is about 100uA, which supplies current to UVLO and Vref Blocks. The charging current I_{Vcc} of the Vcc capacitor is equal to Istr - 100uA. After Vcc reaches the UVLO start voltage only the bias winding supplies Vcc current to device. When the bias winding voltage is not sufficient, the Vcc level decreases to the UVLO stop voltage. At this time Vcc oscillates. In order to prevent this oscillation it is recommended that the Vcc capacitor be chosen to have the value between 10uF and 47uF.

2. Feedback Control : The FSDM311 is the voltage mode controlled device as shown in Figure 6. Usually, an opto-coupler and KA431 type voltage reference are used to implement the feedback network. The feedback voltage is compared with an internally generated sawtooth waveform. This directly controls the duty cycle. When the KA431 reference pin voltage exceeds the internal reference voltage of 2.5V, the optocoupler LED current increases, the feedback voltage Vfb is pulled down and it reduces the duty cycle. This will happen when the input voltage increases or the output load decreases.

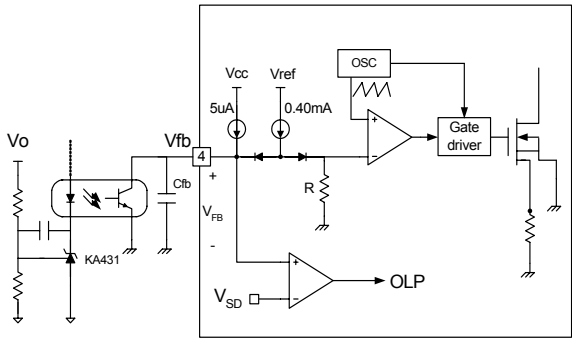


Figure 6. PWM and Feedback Circuit

3. Leading Edge Blanking (LEB) : At the instant the internal Sense FET is turned on, the primary side capacitance and secondary side rectifier diode reverse recovery typically cause a high current spike through the Sense FET. Excessive voltage across the Rsense resistor leads to incorrect feedback operation in the current mode PWM control. To counter this effect, the FPS employs a leading edge blanking (LEB) circuit. This circuit inhibits the PWM comparator for a short time (t_{LEB}) after the Sense FET is turned on.

4. Protection Circuit : The FSDM311 has several protective functions such as over load protection (OLP), over voltage protection (OVP), under voltage lock out (UVLO) and thermal shutdown (TSD). Because these protection circuits are fully integrated inside the IC without external components, the reliability is improved without increasing cost. Once a fault condition occurs, switching is terminated and the Sense FET remains off. This causes Vcc to fall. When Vcc reaches the UVLO stop voltage V_{STOP} (7V), the protection is reset and the internal high voltage current source charges the Vcc capacitor via the Vstr pin. When Vcc reaches the UVLO start voltage V_{START} (9V), the device resumes its normal operation. In this manner, the auto-restart can alternately enable and disable the switching of the power Sense FET until the fault condition is eliminated.

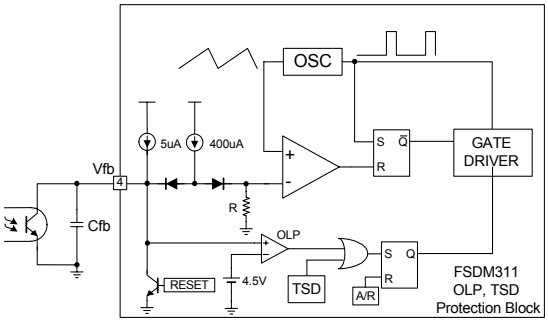


Figure 7. Protection Block

4.1 Over Load Protection (OLP) : Overload is defined as the load current exceeding a pre-set level due to an unexpected event. In this situation, the protection circuit should be activated in order to protect the SMPS. However, even when the SMPS is operating normally, the over load protection (OLP) circuit can be activated during the load transition. In order to avoid this undesired operation, the OLP circuit is designed to be activated after a specified time to determine whether it is a transient situation or an overload situation. In conjunction with the Ipk current limit pin (if used) the current mode feedback path would limit the current in the Sense FET when the maximum PWM duty cycle is attained. If the output consumes more than this maximum power, the output voltage (Vo) decreases below its rating voltage. This reduces the current through the opto-coupler LED, which also reduces the opto-coupler transistor current, thus increasing the feedback voltage (V_{FB}). If V_{FB} exceeds 3V, the feedback input diode is blocked and the 5uA current source (I_{DELAY}) starts to charge Cfb slowly up to Vcc. In this condition, V_{FB} increases until it reaches 4.5V, when the switching operation is terminated as shown in Figure 8. The shutdown delay time is the time required to charge Cfb from 3V to 4.5V with 5uA current source.

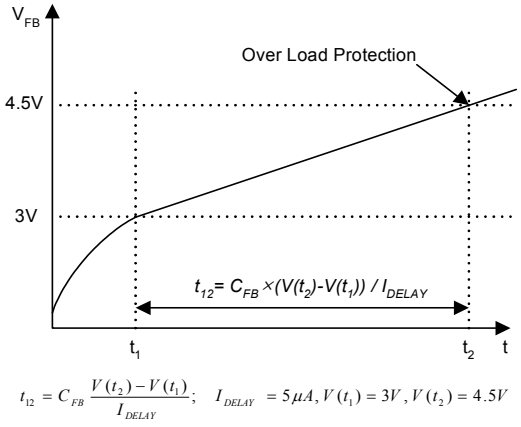


Figure 8. Over Load Protection (OLP)

4.2 Thermal Shutdown (TSD) : The Sense FET and the control IC are integrated, making it easier for the control IC to detect the temperature of the Sense FET. When the temperature exceeds approximately 145°C, thermal shutdown is activated.

5. Soft Start : The FPS has an internal soft start circuit that slowly increases the feedback voltage together with the Sense FET current after it starts up. The typical soft start time is 15msec, as shown in Figure 9, where progressive increments of the Sense FET current are allowed during the start-up phase. The pulse width to the power switching device is progressively increased to establish the correct working conditions for transformers, inductors, and capacitors. The voltage on the output capacitors is progressively increased with the intention of smoothly establishing the required output voltage. It also helps to prevent transformer saturation and reduce the stress on the secondary diode.

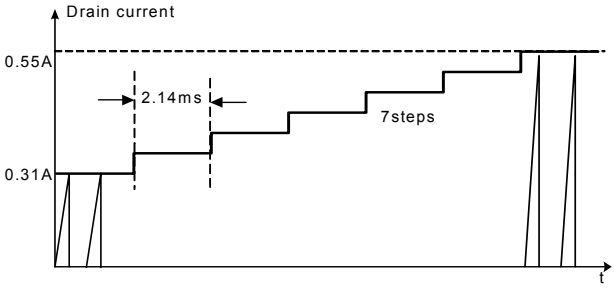


Figure 9. Internal Soft Start

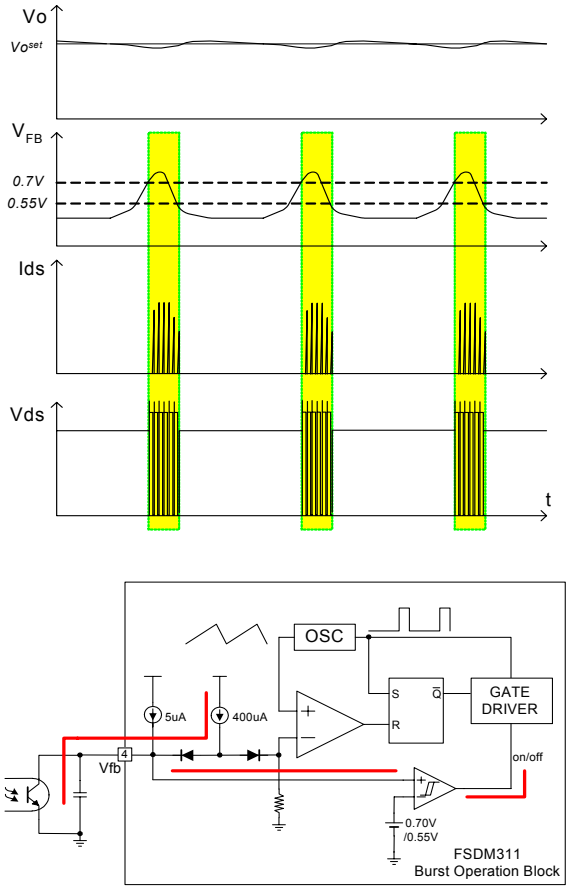


Figure 10. Burst Operation Function

6. Burst operation : In order to minimize the power dissipation in standby mode, the FSDM311 enters burst mode operation. As the load decreases, the feedback voltage decreases. The device automatically enters burst mode when the feedback voltage drops below V_{BURL}(0.55V). At this point switching stops and the output voltages start to drop. This causes the feedback voltage to rise. Once is passes V_{BURH}(0.70V) switching starts again. The feedback voltage falls and the process repeats. Burst mode operation alternately enables and disables switching of the power MOSFET to reduce the switching loss in the standby mode.

Application Tips

1. Methods of Reducing Audible Noise

Switching mode power converters have electronic and magnetic components, which generate audible noises when the operating frequency is in the range of 20~20,000 Hz. Even though they operate above 20 kHz, they can make noise depending on the load condition. Designers can employ several methods to reduce these noises. Here are three of these methods:

Glue or Varnish

The most common method involves using glue or varnish to tighten magnetic components. The motion of core, bobbin and coil and the chattering or magnetostriction of core can cause the transformer to produce audible noise. The use of rigid glue and varnish helps reduce the transformer noise. But, it also can crack the core. This is because sudden changes in the ambient temperature cause the core and the glue to expand or shrink in a different ratio according to the temperature.

Ceramic Capacitor

Using a film capacitor instead of a ceramic capacitor as a snubber capacitor is another noise reduction solution. Some dielectric materials show a piezoelectric effect depending on the electric field intensity. Hence, a snubber capacitor becomes one of the most significant sources of audible noise. It is considerable to use a zener clamp circuit instead of an RCD snubber for higher efficiency as well as lower audible noise.

Adjusting Sound Frequency

Moving the fundamental frequency of noise out of 2~4 kHz range is the third method. Generally, humans are more sensitive to noise in the range of 2~4 kHz. When the fundamental frequency of noise is located in this range, one perceives the noise as louder although the noise intensity level is identical. Refer to Figure 11. Equal Loudness Curves.

When FPS acts in Burst mode and the Burst operation is suspected to be a source of noise, this method may be helpful. If the frequency of Burst mode operation lies in the range of 2~4 kHz, adjusting feedback loop can shift the Burst operation frequency. In order to reduce the Burst operation frequency, increase a feedback gain capacitor (C_F), opto-coupler supply resistor (R_D) and feedback capacitor (C_B) and decrease a feedback gain resistor (R_F) as shown in Figure 12. Typical Feedback Network of FPS.

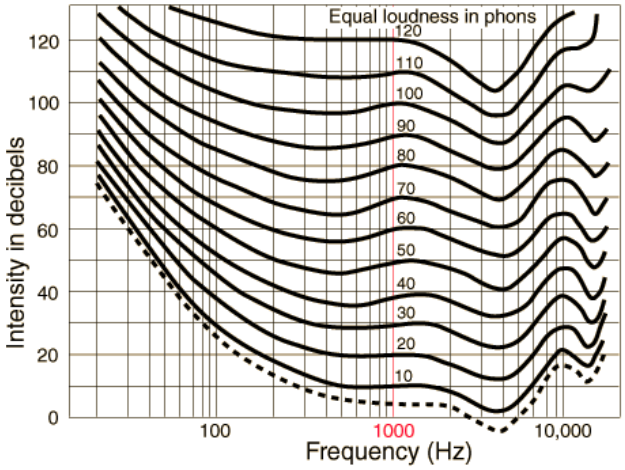


Figure 11. Equal Loudness Curves

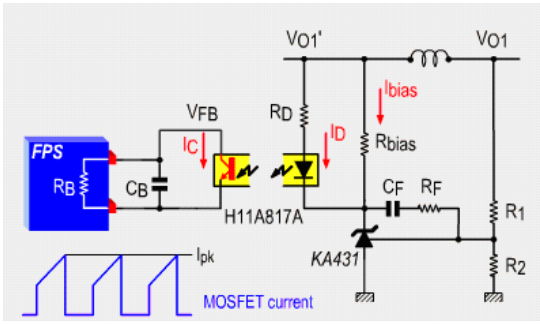


Figure 12. Typical Feedback Network of FPS

2. Other Reference Materials

AN-4134: Design Guidelines for Off-line Forward Converters Using Fairchild Power Switch (FPS™)

AN-4137: Design Guidelines for Off-line Flyback Converters Using Fairchild Power Switch (FPS)

AN-4138: Design Considerations for Battery Charger Using Green Mode Fairchild Power Switch (FPS™)

AN-4140: Transformer Design Consideration for Off-line Flyback Converters using Fairchild Power Switch (FPS™)

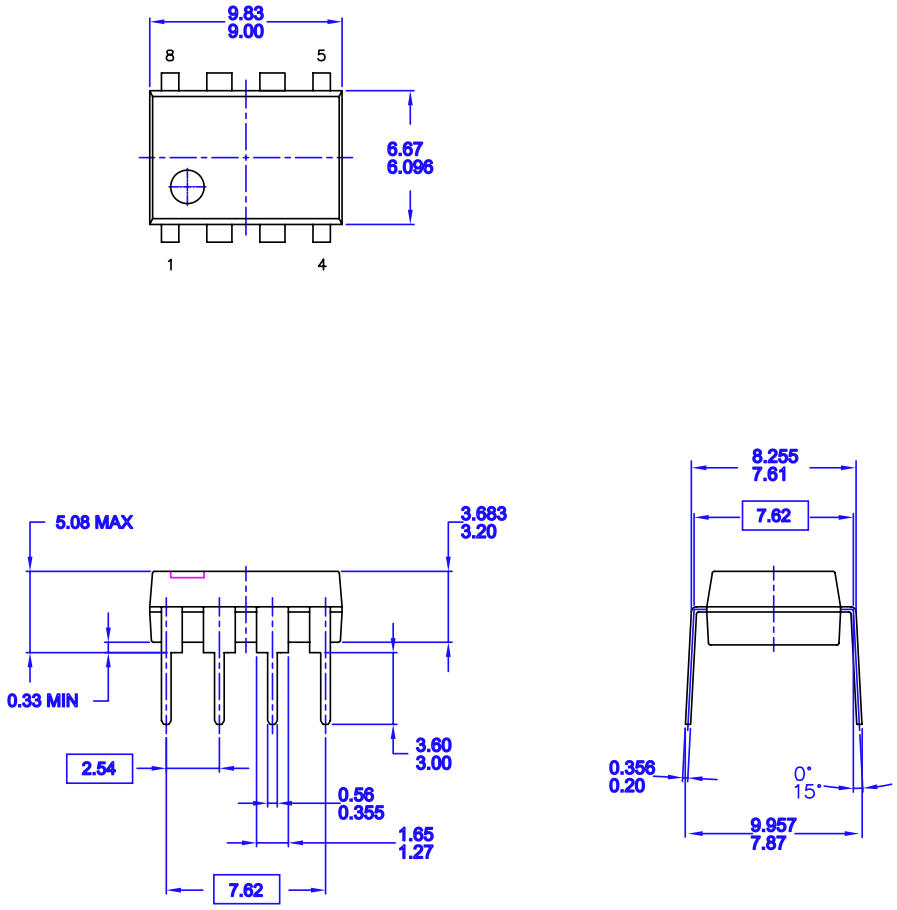
AN-4141: Troubleshooting and Design Tips for Fairchild Power Switch (FPS™) Flyback Applications

AN-4147: Design Guidelines for RCD Snubber of Flyback

AN-4148: Audible Noise Reduction Techniques for FPS Applications

Package Dimensions

8DIP

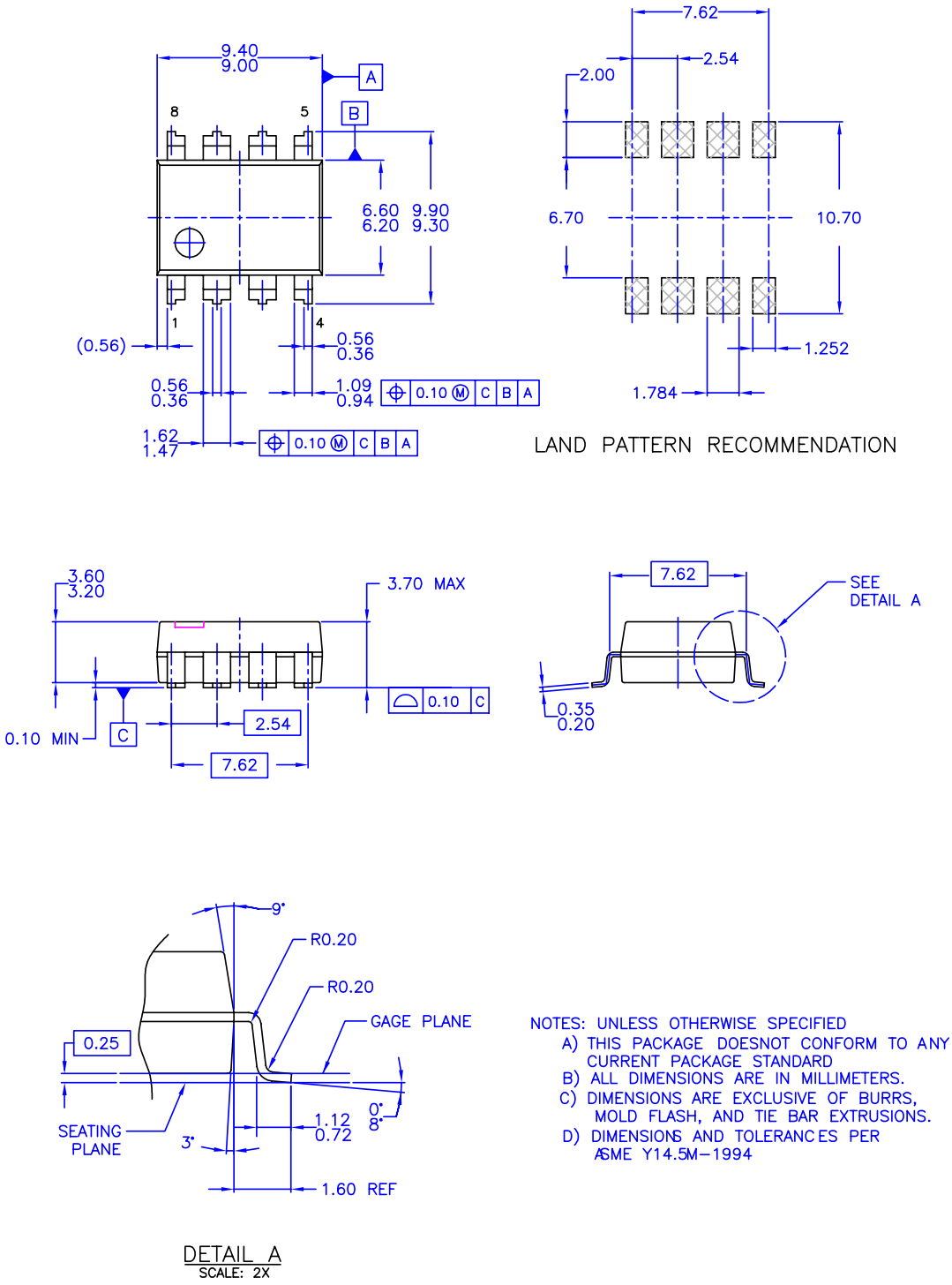


NOTES: UNLESS OTHERWISE SPECIFIED
A) THIS PACKAGE CONFORMS TO JEDEC MS-001 VARIATION BA
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
D) DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994

MKT-N08FrevB

Package Dimensions (Continued)

8LSOP



Ordering Information

Product Number	Package	Marking Code	BV_{DSS}	f_{OSC}	$R_{DS(ON)}$
FSDM311	8DIP	DM311	650V	67KHz	14Ω
FSDM311L	8LSOP	DM311	650V	67KHz	14Ω