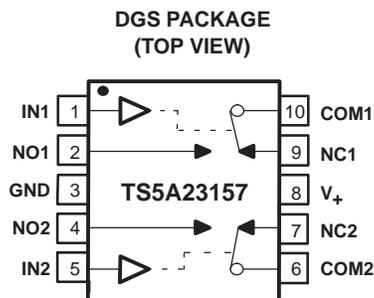


DESCRIPTION

The TS5A23157 is a dual, single-pole, double-throw (SPDT) analog switch designed to operate from 1.65 V to 5.5 V. This device can handle both digital and analog signals. Signals up to 5.5 V (peak) can be transmitted in either direction.

APPLICATIONS

- Sample-and-Hold Circuit
- Battery-Powered Equipments
- Audio and Video Signal Routing
- Communication Circuits



FUNCTION TABLE

INPUT	NC TO COM COM TO NC	NO TO COM COM TO NO
L	ON	OFF
H	OFF	ON

FEATURES

- Specified Break-Before-Make Switching
- Low ON-State Resistance (10 Ω)
- Control Inputs Are 5-V Tolerant
- Low Charge Injection
- Excellent ON-Resistance Matching
- Low Total Harmonic Distortion
- 1.8-V to 5.5-V Single-Supply Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)

SUMMARY OF CHARACTERISTICS

($V_+ = 5\text{ V}$; $T_A = 25^\circ\text{C}$)

CONFIGURATION	2:1 MULTIPLEXER/ DEMULTIPLEXER (2 × SPDT)
Number of channels	2
r_{on}	10 Ω
Δr_{on}	0.15 Ω
$r_{on(Flat)}$	4 Ω
t_{ON}/t_{OFF}	5.7 ns/3.8 ns
t_{BBM}	0.5 ns
Charge injection	7 pC
Bandwidth	220 MHz
OFF isolation	–65 dB at 10 MHz
Crosstalk	–66 dB at 10 MHz
Total harmonic distortion	0.01%
$I_{COM(OFF)}/I_{NC(OFF)}$	$\pm 1\ \mu\text{A}$
Package option	10-pin DGS

ORDERING INFORMATION

T_A	PACKAGE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	VSSOP (MSOP-10) – DGS Tape and reel	TS5A23157DGSR	JBR

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ABSOLUTE MAXIMUM RATINGS

(over operating free air temperature range unless otherwise noted)†

Supply voltage range, V_+ (see Note 1)	–0.5 V to 6.5 V
Analog voltage range, V_{NC} , V_{NO} , V_{COM} (see Notes 1, 2, and 3)	–0.5 V to $V_+ + 0.5$ V
Analog port diode current, $I_{I/OK}$ (V_{NC} , V_{NO} , $V_{COM} < 0$ or V_{NC} , V_{NO} , $V_{COM} > V_+$)	±50 mA
On-state switch current, I_{NC} , I_{NO} , I_{COM} (V_{NC} , V_{NO} , $V_{COM} = 0$ to V_+)	±50 mA
Digital input voltage range, V_{IN} (see Notes 1 and 2)	–0.5 V to 6.5 V
Digital input clamp current, I_{IK} ($V_{IN} < 0$)	–50 mA
Continuous current through V_+ or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 4)	165°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- (1) All voltages are with respect to ground, unless otherwise specified.
- (2) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) This value is limited to 5.5 V maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

ELECTRICAL CHARACTERISTICS FOR 5-V SUPPLY

($V_+ = 4.5$ V to 5.5 V; $T_A = -40^\circ\text{C}$ to 85°C) (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A	V_+	MIN	TYP†	MAX	UNIT	
ANALOG SWITCH									
Analog signal range	V_{COM} , V_{NO} , V_{NC}				0		V_+	V	
ON resistance	r_{on}	$0 \leq V_{NO}$ or $V_{NC} \leq V_+$, $I_{COM} = -30$ mA,	Full	4.5 V			10	Ω	
ON resistance match between channels	Δr_{on}	V_{NO} or $V_{NC} = 3.15$ V, $I_{COM} = -30$ mA,	25°C	4.5 V		0.15		Ω	
ON resistance flatness	$r_{on(Flat)}$	$0 \leq V_{NO}$ or $V_{NC} \leq V_+$, $I_{COM} = -30$ mA,	25°C	4.5 V		4		Ω	
NC, NO, OFF leakage current	$I_{NC(OFF)}$, $I_{NO(OFF)}$	V_{NC} or $V_{NO} = 0$ to V_+ , $V_{COM} = 0$ to V_+ ,	Switch OFF, see Figure 11	25°C	5.5 V	–1	0.05	1	μA
				Full					
NC, NO, ON leakage current	$I_{NC(ON)}$, $I_{NO(ON)}$	V_{NC} or $V_{NO} = 0$ to V_+ , $V_{COM} = \text{Open}$,	Switch ON, see Figure 11	25°C	5.5 V	–0.1		0.1	μA
				Full					
COM ON leakage current	$I_{COM(ON)}$	V_{NC} or $V_{NO} = \text{Open}$, $V_{COM} = 0$ to V_+ ,	Switch ON, see Figure 11	25°C	5.5 V	–0.1		0.1	μA
				Full					
DIGITAL INPUTS (IN1, IN2) (see Note 1)									
Input logic high	V_{IH}		Full		$V_+ \times 0.7$			V	
Input logic low	V_{IL}		Full		$V_+ \times 0.3$			V	
Input leakage current	I_{IH} , I_{IL}	$V_{IN} = 5.5$ V or 0	25°C	5.5 V	–1	0.05	1	μA	
			Full						

† $T_A = 25^\circ\text{C}$

(1) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS FOR 5-V SUPPLY (CONTINUED)

 ($V_+ = 4.5\text{ V to }5.5\text{ V}$; $T_A = -40^\circ\text{C to }85^\circ\text{C}$) (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A	V_+	MIN	TYP†	MAX	UNIT
DYNAMIC								
Turnon time	t_{ON}	$V_{NC} = \text{GND}$ and $V_{NO} = V_+$ or $V_{NC} = V_+$ and $V_{NO} = \text{GND}$, $R_L = 500\ \Omega$, $C_L = 50\ \text{pF}$, see Figure 13	Full	4.5 V to 5.5 V	1.7		5.7	ns
Turnoff time	t_{OFF}	$V_{NC} = \text{GND}$ and $V_{NO} = V_+$ or $V_{NC} = V_+$ and $V_{NO} = \text{GND}$, $R_L = 500\ \Omega$, $C_L = 50\ \text{pF}$, see Figure 13	Full	4.5 V to 5.5 V	0.8		3.8	ns
Break-before-make time	t_{BBM}	$V_{NC} = V_{NO} = V_+/2$, $R_L = 50\ \Omega$, $C_L = 35\ \text{pF}$, see Figure 14	Full	4.5 V to 5.5 V	0.5			ns
Charge injection	Q_C	$R_L = 1\ \text{M}\Omega$, $C_L = 0.1\ \text{nF}$, see Figure 18	25°C	5 V		7		pC
NC, NO OFF capacitance	$C_{NC(OFF)}$, $C_{NO(OFF)}$	V_{NC} or $V_{NO} = V_+$ or GND, Switch OFF, see Figure 12	25°C	5 V		5.5		pF
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or $V_{NO} = V_+$ or GND, Switch ON, see Figure 12	25°C	5 V		17.5		pF
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON, see Figure 12	25°C	5 V		17.5		pF
Digital input capacitance	C_{IN}	$V_{IN} = V_+$ or GND, see Figure 12	25°C	5 V		2.8		pF
Bandwidth	BW	$R_L = 50\ \Omega$, Switch ON, see Figure 15	25°C	4.5 V		220		MHz
OFF isolation	O_{ISO}	$R_L = 50\ \Omega$, $f = 10\ \text{MHz}$, Switch OFF, see Figure 16	25°C	4.5 V		-65		dB
Crosstalk	X_{TALK}	$R_L = 50\ \Omega$, $f = 10\ \text{MHz}$, Switch ON, see Figure 17	25°C	4.5 V		-66		dB
Total harmonic distortion	THD	$R_L = 600\ \Omega$, $C_L = 50\ \text{pF}$, $f = 600\ \text{Hz to }20\ \text{kHz}$, see Figure 19	25°C	4.5 V		0.01		%
SUPPLY								
Positive supply current	I_+	$V_{IN} = V_+$ or GND, Switch ON or OFF	25°C	5.5 V	1			μA
			Full		10			
Change in supply current	ΔI_+	$V_{IN} = V_+ - 0.6\ \text{V}$	Full	5.5 V	500			μA

 † $T_A = 25^\circ\text{C}$

TS5A23157

10-Ω SPDT ANALOG SWITCH

SCDS165 – MAY 2004

ELECTRICAL CHARACTERISTICS FOR 3.3-V SUPPLY

($V_+ = 3\text{ V to }3.6\text{ V}$; $T_A = -40\text{ }^\circ\text{C to }85\text{ }^\circ\text{C}$) (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A	V_+	MIN	TYP†	MAX	UNIT	
ANALOG SWITCH									
Analog signal range	V_{COM}, V_{NO}, V_{NC}				0		V_+	V	
ON resistance	r_{on}	$0 \leq V_{NO}$ or $V_{NC} \leq V_+$, $I_{COM} = -24\text{ mA}$,	Switch ON, see Figure 10	Full	3 V		18	Ω	
ON-resistance match between channels	Δr_{on}	V_{NO} or $V_{NC} = 2.1\text{ V}$, $I_{COM} = -24\text{ mA}$,	Switch ON, see Figure 10	25°C	3 V	0.2		Ω	
ON-resistance flatness	$r_{on(Flat)}$	$0 \leq V_{NO}$ or $V_{NC} \leq V_+$, $I_{COM} = -24\text{ mA}$,	Switch ON, see Figure 12	25°C	3 V	9		Ω	
NC, NO OFF leakage current	$I_{NC(OFF)}, I_{NO(OFF)}$	V_{NC} or $V_{NO} = 0$ to V_+ , $V_{COM} = 0$ to V_+ ,	Switch OFF, see Figure 11	25°C	3.6 V	-1	0.05	1	μA
				Full		-1		1	
NC, NO ON leakage current	$I_{NC(ON)}, I_{NO(ON)}$	V_{NC} or $V_{NO} = 0$ to V_+ , $V_{COM} = \text{Open}$,	Switch ON, see Figure 11	25°C	3.6 V	-0.1		0.1	μA
				Full		-1		1	
COM ON leakage current	$I_{COM(ON)}$	V_{NC} or $V_{NO} = \text{Open}$, $V_{COM} = 0$ to V_+ ,	Switch ON, see Figure 11	25°C	3.6 V	-0.1		0.1	μA
				Full		-1		1	
DIGITAL INPUTS (IN1, IN2) (see Note 1)									
Input logic high	V_{IH}			Full		$V_+ \times 0.7$		V	
Input logic low	V_{IL}			Full		$V_+ \times 0.3$		V	
Input leakage current	I_{IH}, I_{IL}	$V_{IN} = 5.5\text{ V}$ or 0		25°C	3.6 V	-1	0.05	1	μA
				Full		-1		1	
DYNAMIC									
Turnon time	t_{ON}	$V_{NC} = \text{GND}$ and $V_{NO} = V_+$ or $V_{NC} = V_+$ and $V_{NO} = \text{GND}$,	$R_L = 500\ \Omega$, $C_L = 50\text{ pF}$, see Figure 13	Full	3 V to 3.6 V	2.5		7.6	ns
Turnoff time	t_{OFF}	$V_{NC} = \text{GND}$ and $V_{NO} = V_+$ or $V_{NC} = V_+$ and $V_{NO} = \text{GND}$,	$R_L = 500\ \Omega$, $C_L = 50\text{ pF}$, see Figure 13	Full	3 V to 3.6 V	1.5		5.3	ns
Break-before-make time	t_{BBM}	$V_{NC} = V_{NO} = V_+/2$, $R_L = 50\ \Omega$,	$C_L = 35\text{ pF}$, see Figure 14	Full	3 V to 3.6 V	0.5			ns
Charge injection	Q_C	$R_L = 1\text{ M}\Omega$, $C_L = 0.1\text{ nF}$,	see Figure 18	25°C	3.3 V		3		pC
Bandwidth	BW	$R_L = 50\ \Omega$, Switch ON,	see Figure 15	25°C	3 V		220		MHz
OFF isolation	O_{ISO}	$R_L = 50\ \Omega$, $f = 10\text{ MHz}$,	Switch OFF, see Figure 16	25°C	3 V		-65		dB
Crosstalk	XTALK	$R_L = 50\ \Omega$, $f = 10\text{ MHz}$,	Switch ON, see Figure 17	25°C	3 V		-66		dB
Total harmonic distortion	THD	$R_L = 600\ \Omega$, $C_L = 50\text{ pF}$,	$f = 600\text{ Hz to }20\text{ kHz}$, see Figure 19	25°C	3 V		0.015		%
SUPPLY									
Positive supply current	I_+	$V_{IN} = V_+$ or GND,	Switch ON or OFF	25°C	3.6 V			1	μA
				Full				10	
Change in supply current	ΔI_+	$V_{IN} = V_+ - 0.6\text{ V}$		Full	3.6 V			500	μA

† $T_A = 25^\circ\text{C}$

(1) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS FOR 2.5-V SUPPLY

($V_+ = 2.3\text{ V to }2.7\text{ V}$; $T_A = -40^\circ\text{C to }85^\circ\text{C}$) (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A	V_+	MIN	TYP†	MAX	UNIT	
ANALOG SWITCH									
Analog signal range	V_{COM}, V_{NO}, V_{NC}				0		V_+	V	
ON resistance	r_{on}	$0 \leq V_{NO}$ or $V_{NC} \leq V_+$, $I_{COM} = -8\text{ mA}$,	Switch ON, see Figure 10	Full	2.3 V		45	Ω	
ON-resistance match between channels	Δr_{on}	V_{NO} or $V_{NC} = 1.6\text{ V}$, $I_{COM} = -8\text{ mA}$,	Switch ON, see Figure 10	25°C	2.3 V	0.5		Ω	
ON-resistance flatness	$r_{on(flat)}$	$0 \leq V_{NO}$ or $V_{NC} \leq V_+$, $I_{COM} = -8\text{ mA}$,	Switch ON, see Figure 10	25°C	2.3 V	27		Ω	
NC, NO OFF leakage current	$I_{NC(OFF)}, I_{NO(OFF)}$	V_{NC} or $V_{NO} = 0$ to V_+ , $V_{COM} = 0$ to V_+ ,	Switch OFF, see Figure 11	25°C	2.7 V	-1	0.05	1	μA
				Full		-1		1	
NC, NO ON leakage current	$I_{NC(ON)}, I_{NO(ON)}$	V_{NC} or $V_{NO} = 0$ to V_+ , $V_{COM} = \text{Open}$,	Switch ON, see Figure 11	25°C	2.7 V	-0.1		0.1	μA
				Full		-1		1	
COM ON leakage current	$I_{COM(ON)}$	V_{NC} or $V_{NO} = \text{Open}$, $V_{COM} = 0$ to V_+ ,	Switch ON, see Figure 11	25°C	2.7 V	-0.1		0.1	μA
				Full		-1		1	
DIGITAL INPUTS (IN1, IN2) (see Note 1)									
Input logic high	V_{IH}			Full		$V_+ \times 0.7$		V	
Input logic low	V_{IL}			Full		$V_+ \times 0.3$		V	
Input leakage current	I_{IH}, I_{IL}	$V_{IN} = 5.5\text{ V or }0$		25°C	2.7 V	-1	0.05	1	μA
				Full		-1		1	
DYNAMIC									
Turnon time	t_{ON}	$V_{NC} = \text{GND}$ and $V_{NO} = V_+$ or $V_{NC} = V_+$ and $V_{NO} = \text{GND}$,	$R_L = 500\ \Omega$, $C_L = 50\text{ pF}$, see Figure 13	Full	2.3 V to 2.7 V	3.5		14	ns
Turnoff time	t_{OFF}	$V_{NC} = \text{GND}$ and $V_{NO} = V_+$ or $V_{NC} = V_+$ and $V_{NO} = \text{GND}$,	$R_L = 500\ \Omega$, $C_L = 50\text{ pF}$, see Figure 13	Full	2.3 V to 2.7 V	2		7.5	ns
Break-before-make time	t_{BBM}	$V_{NC} = V_{NO} = V_+/2$, $R_L = 50\ \Omega$,	$C_L = 35\text{ pF}$, see Figure 14	Full	2.3 V to 2.7 V	0.5			ns
Bandwidth	BW	$R_L = 50\ \Omega$,	Switch ON, see Figure 15	25°C	2.3 V	220			MHz
OFF isolation	O_{ISO}	$R_L = 50\ \Omega$, $f = 10\text{ MHz}$,	Switch OFF, see Figure 16	25°C	2.3 V	-65			dB
Crosstalk	X_{TALK}	$R_L = 50\ \Omega$, $f = 10\text{ MHz}$,	Switch ON, see Figure 17	25°C	2.3 V	-66			dB
Total harmonic distortion	THD	$R_L = 600\ \Omega$, $C_L = 50\text{ pF}$,	$f = 600\text{ Hz to }20\text{ kHz}$, see Figure 19	25°C	2.3 V	0.025			%
SUPPLY									
Positive supply current	I_+	$V_{IN} = V_+$ or GND,	Switch ON or OFF	25°C	2.7 V			1	μA
				Full				10	
Change in supply current	ΔI_+	$V_{IN} = V_+ - 0.6\text{ V}$		Full	2.7 V			500	μA

† $T_A = 25^\circ\text{C}$

(1) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

TS5A23157

10-Ω SPDT ANALOG SWITCH

SCDS165 – MAY 2004

ELECTRICAL CHARACTERISTICS FOR 1.8-V SUPPLY

($V_+ = 1.65\text{ V to }1.95\text{ V}$; $T_A = -40^\circ\text{C to }85^\circ\text{C}$) (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A	V_+	MIN	TYP†	MAX	UNIT	
ANALOG SWITCH									
Analog signal range	V_{COM}, V_{NO}, V_{NC}				0		V_+	V	
ON resistance	r_{on}	$0 \leq V_{NO} \text{ or } V_{NC} \leq V_+$, $I_{COM} = -4\text{ mA}$,	Switch ON, see Figure 10	Full	1.65 V		140	Ω	
ON-resistance match between channels	Δr_{on}	$V_{NO} \text{ or } V_{NC} = 1.15\text{ V}$, $I_{COM} = -4\text{ mA}$,	Switch ON, see Figure 10	25°C	1.65 V	1		Ω	
ON-resistance flatness	$r_{on}(\text{flat})$	$0 \leq V_{NO} \text{ or } V_{NC} \leq V_+$, $I_{COM} = -4\text{ mA}$,	Switch ON, see Figure 10	25°C	1.65 V	110		Ω	
NC, NO OFF leakage current	$I_{NC}(\text{OFF}), I_{NO}(\text{OFF})$	$V_{NC} \text{ or } V_{NO} = 0 \text{ to } V_+$, $V_{COM} = 0 \text{ to } V_+$,	Switch OFF, see Figure 11	25°C	1.95 V	-1	0.05	1	μA
				Full		-1		1	
NC, NO ON leakage current	$I_{NC}(\text{ON}), I_{NO}(\text{ON})$	$V_{NC} \text{ or } V_{NO} = 0 \text{ to } V_+$, $V_{COM} = \text{Open}$,	Switch ON, see Figure 11	25°C	1.95 V	-0.1		0.1	μA
				Full		-1		1	
COM ON leakage current	$I_{COM}(\text{ON})$	$V_{NC} \text{ or } V_{NO} = \text{Open}$, $V_{COM} = 0 \text{ to } V_+$,	Switch ON, see Figure 11	25°C	1.95 V	-0.1		0.1	μA
				Full		-1		1	
DIGITAL INPUTS (IN1, IN2) (see Note 1)									
Input logic high	V_{IH}			Full		$V_+ \times 0.75$		V	
Input logic low	V_{IL}			Full		$V_+ \times 0.25$		V	
Input leakage current	I_{IH}, I_{IL}	$V_{IN} = 5.5\text{ V or }0$		25°C	1.95 V	-1	0.05	1	μA
				Full		-1		1	
DYNAMIC									
Turnon time	t_{ON}	$V_{NC} = \text{GND and } V_{NO} = V_+$ or $V_{NC} = V_+ \text{ and } V_{NO} = \text{GND}$,	$R_L = 500\ \Omega$, $C_L = 50\ \text{pF}$, see Figure 13	Full	1.65 V to 1.95 V	7	24	ns	
Turnoff time	t_{OFF}	$V_{NC} = \text{GND and } V_{NO} = V_+$ or $V_{NC} = V_+ \text{ and } V_{NO} = \text{GND}$,	$R_L = 500\ \Omega$, $C_L = 50\ \text{pF}$, see Figure 13	Full	1.65 V to 1.95 V	3	13	ns	
Break-before-make time	t_{BBM}	$V_{NC} = V_{NO} = V_+/2$, $R_L = 50\ \Omega$,	$C_L = 35\ \text{pF}$, see Figure 14	Full	1.65 V to 1.95 V	0.5		ns	
Bandwidth	BW	$R_L = 50\ \Omega$,	Switch ON, see Figure 15	25°C	1.8 V	220		MHz	
OFF isolation	O_{ISO}	$R_L = 50\ \Omega$, $f = 10\ \text{MHz}$,	Switch OFF, see Figure 16	25°C	1.8 V	-60		dB	
Crosstalk	X_{TALK}	$R_L = 50\ \Omega$, $f = 10\ \text{MHz}$,	Switch ON, see Figure 17	25°C	1.8 V	-66		dB	
Total harmonic distortion	THD	$R_L = 600\ \text{k}\Omega$, $C_L = 50\ \text{pF}$,	$f = 600\ \text{Hz to }20\ \text{kHz}$, see Figure 19	25°C	1.8 V	0.015		%	
SUPPLY									
Positive supply current	I_+	$V_{IN} = V_+ \text{ or GND}$,	Switch ON or OFF	25°C	1.95 V		1	μA	
				Full			10		
Change in supply current	ΔI_+	$V_{IN} = V_+ - 0.6\text{ V}$		Full	1.95 V		500	μA	

† $T_A = 25^\circ\text{C}$

(1) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

TYPICAL PERFORMANCE

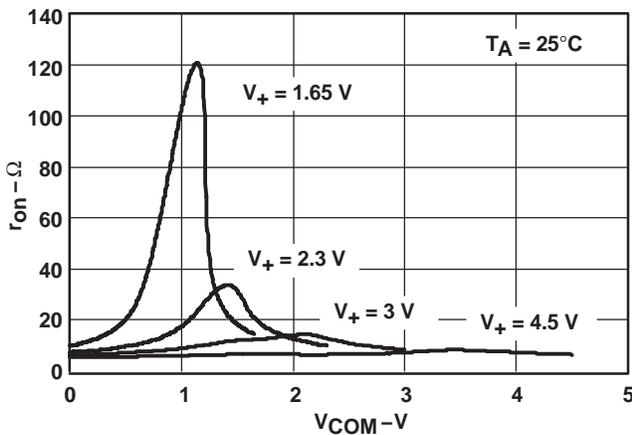


Figure 1. r_{on} vs V_{COM}

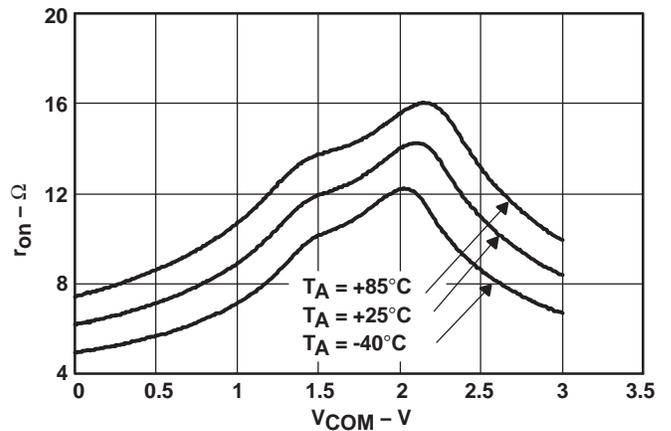


Figure 2. r_{on} vs V_{COM} ($V_+ = 3$ V)

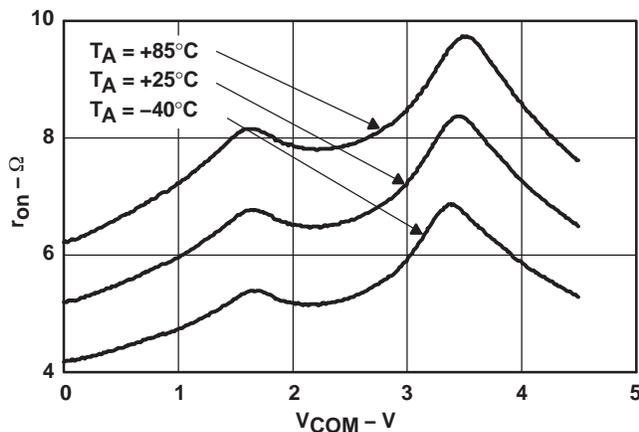


Figure 3. r_{on} vs V_{COM} ($V_+ = 5$ V)

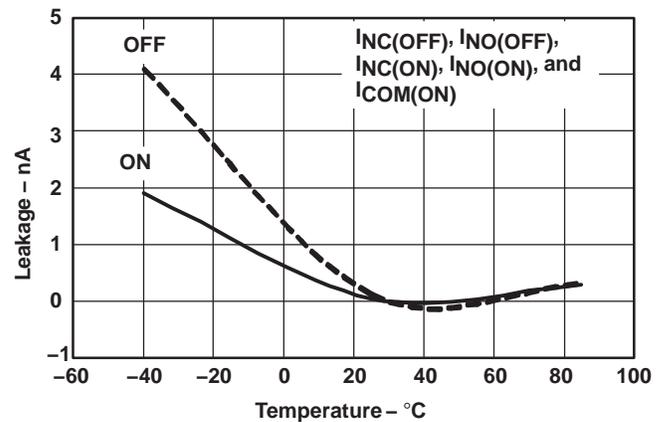


Figure 4. Leakage Current vs Temperature ($V_+ = 5.5$ V)

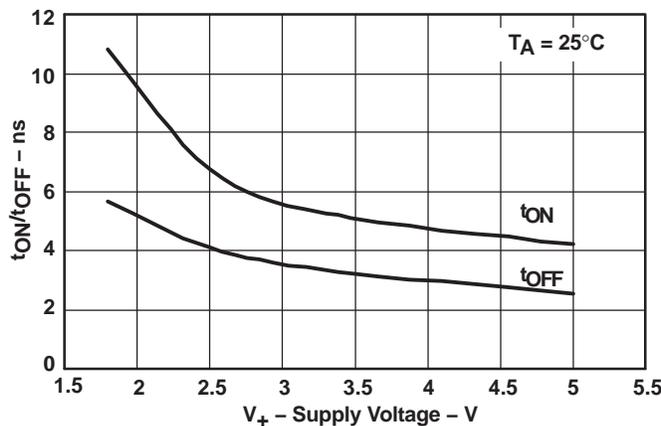


Figure 5. t_{ON} and t_{OFF} vs V_+

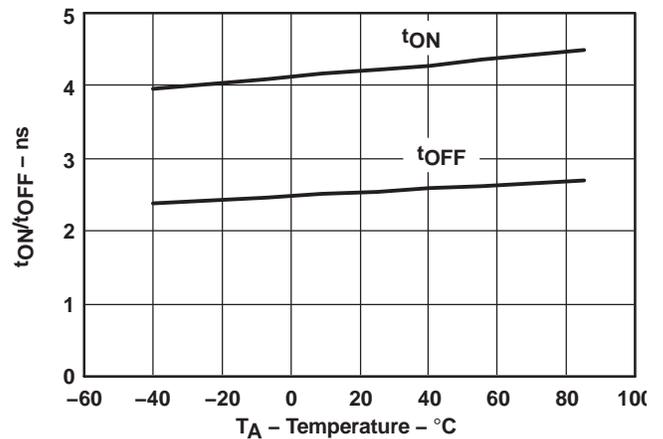


Figure 6. t_{ON} and t_{OFF} vs Temperature ($V_+ = 5$ V)

TYPICAL PERFORMANCE (continued)

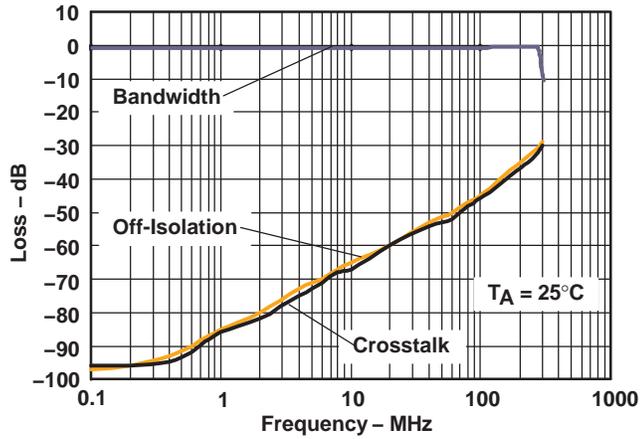


Figure 7. Frequency Response ($V_+ = 3\text{ V}$)

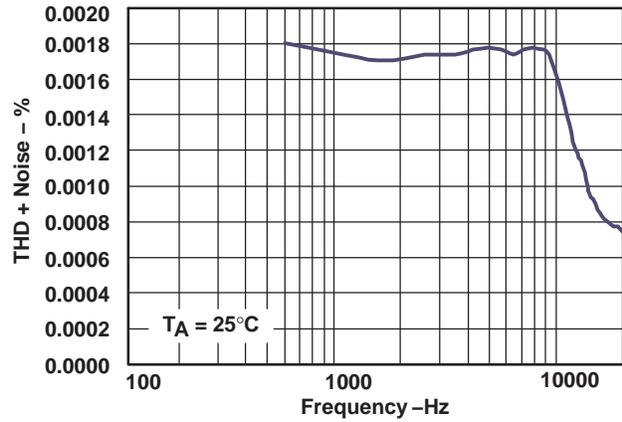


Figure 8. Total Harmonic Distortion (THD) vs Frequency ($V_+ = 3\text{ V}$)

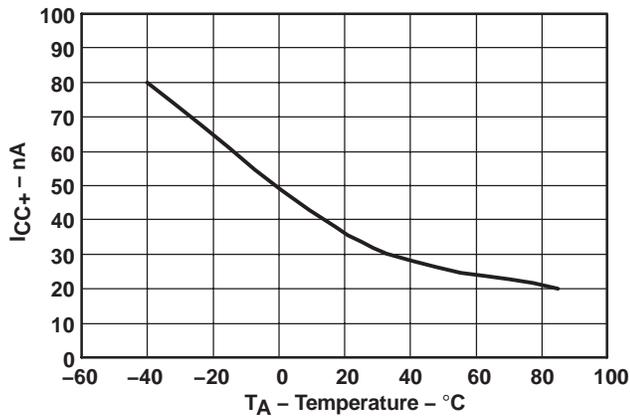


Figure 9. Power-Supply Current vs Temperature ($V_+ = 5\text{ V}$)

PIN DESCRIPTION

PIN NUMBER	NAME	DESCRIPTION
1	IN1	Digital control pin to connect the COM terminal to the NO or NC terminals
2	NO1	Normally-open terminal
3	GND	Digital ground
4	NO2	Normally-open terminal
5	IN2	Digital control pin to connect the COM terminal to the NO or NC terminals
6	COM2	Common terminal
7	NC2	Normally-closed terminal
8	V ₊	Power supply
9	NC1	Normally-closed terminal
10	COM1	Common terminal

PARAMETER DESCRIPTION

SYMBOL	DESCRIPTION
V _{COM}	Voltage at the COM pin
V _{NC}	Voltage at the NC pin
V _{NO}	Voltage at the NO pin
r _{on}	Resistance between COM and NC or COM and NO ports when the channel is ON
Δr _{on}	Difference of r _{on} between channels
r _{on(flat)}	Difference between the maximum and minimum value of r _{on} in a channel over the specified range of conditions
I _{NC(OFF)}	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the OFF state under worst-case input and output conditions.
I _{NO(OFF)}	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state under worst-case input and output conditions
I _{NC(ON)}	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the ON state and the output (COM) being open
I _{NO(ON)}	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) being open
I _{COM(ON)}	Leakage current measured at the COM port, with the corresponding channel (NO to COM or NC to COM) in the ON state and the output (NC or NO) being open
V _{IH}	Minimum input voltage for logic high for the control input (IN)
V _{IL}	Minimum input voltage for logic low for the control input (IN)
V _{IN}	Voltage at the IN pin
I _{IH} , I _{IL}	Leakage current measured at the IN pin
t _{ON}	Turnon time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog outputs (COM/NC/NO) signal when the switch is turning ON.
t _{OFF}	Turnoff time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog outputs (COM/NC/NO) signal when the switch is turning OFF.
t _{BBM}	Break-before-make time. This parameter is measured under the specified range of conditions and by the propagation delay between the output of two adjacent analog channels (NC and NO) when the control signal changes state.
Q _C	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NC, NO, or COM) output. This is measured in coulombs (C) and measured by the total charge induced due to switching of the control input. Charge injection, Q _C = C _L × ΔV _O , C _L is the load capacitance and ΔV _O is the change in analog output voltage.

PARAMETER DESCRIPTION (continued)

SYMBOL	DESCRIPTION
$C_{NC(OFF)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is OFF
$C_{NO(OFF)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is OFF
$C_{NC(ON)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is ON
$C_{NO(ON)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is ON
$C_{COM(ON)}$	Capacitance at the COM port when the corresponding channel (COM to NC or COM to NO) is ON
C_{IN}	Capacitance of the IN input
O_{ISO}	OFF isolation of the switch is a measurement of off-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NC to COM or NO to COM) in the OFF state. OFF isolation, $O_{ISO} = 20 \text{ LOG } (V_{NC}/V_{COM})$ dB, V_{COM} is the input and V_{NC} is the output.
X_{TALK}	Crosstalk is a measurement of unwanted signal coupling from an ON channel to an OFF channel (NC to NO or NO to NC). This is measured at a specific frequency and in dB. Crosstalk, $X_{TALK} = 20 \text{ log } (V_{NC1}/V_{NO1})$, V_{NO1} is the input and V_{NC1} is the output.
BW	Bandwidth of the switch. This is the frequency where the gain of an ON channel is -3 dB below the dc gain. Gain is measured from the equation, $20 \text{ log } (V_{NC}/V_{COM})$ dB, where V_{NC} is the output and V_{COM} is the input.
I_+	Static power-supply current with the control (IN) pin at V_+ or GND
ΔI_+	This is the increase in I_+ for each control (IN) input that is at the specified voltage rather than at V_+ or GND.

PARAMETER MEASUREMENT INFORMATION

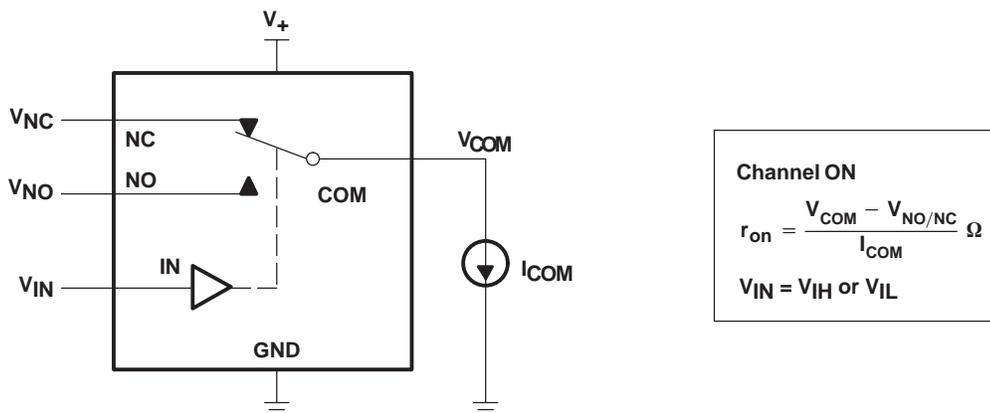


Figure 10. ON-State Resistance (r_{on})

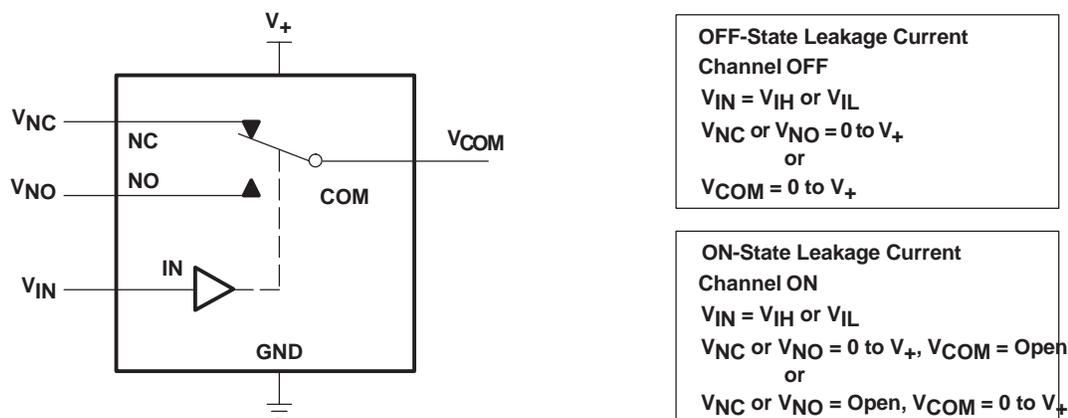


Figure 11. ON- and OFF-State Leakage Current ($I_{COM(ON)}$, $I_{NC(OFF)}$, $I_{NO(OFF)}$, $I_{NC(ON)}$, $I_{NO(ON)}$)

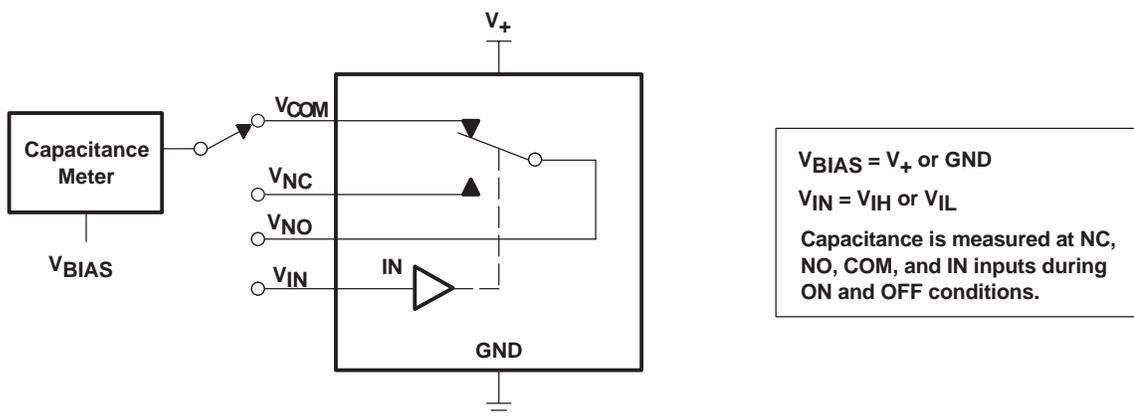


Figure 12. Capacitance (C_{IN} , $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NO(OFF)}$, $C_{NC(ON)}$, $C_{NO(ON)}$)

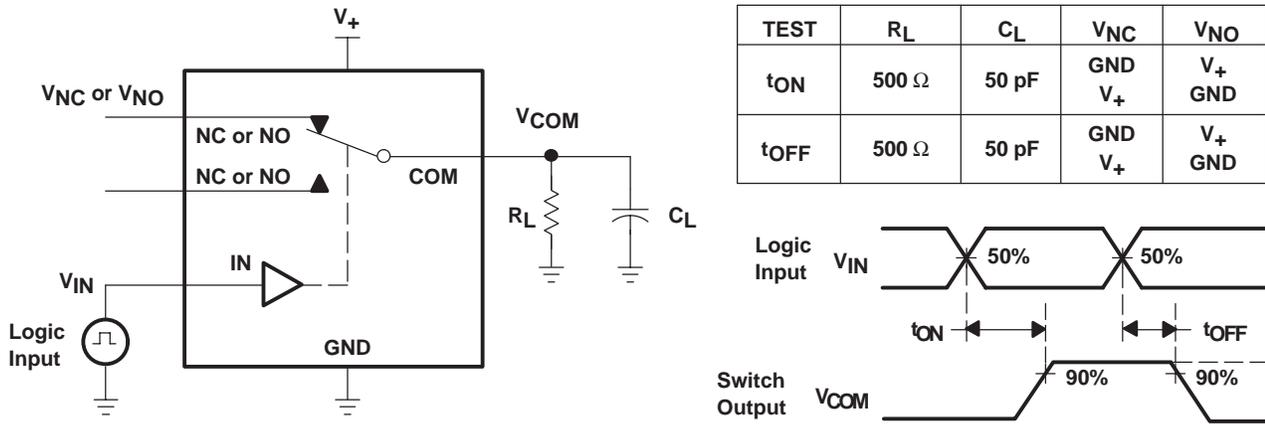


Figure 13. Turnon (tON) and Turnoff(tOFF) Time

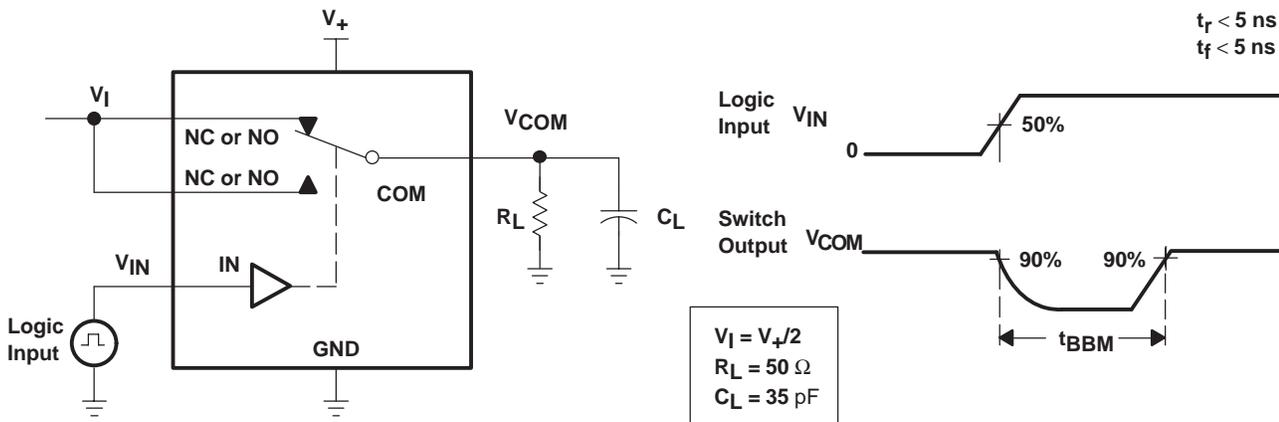


Figure 14. Break-Before-Make (tBBM) Time

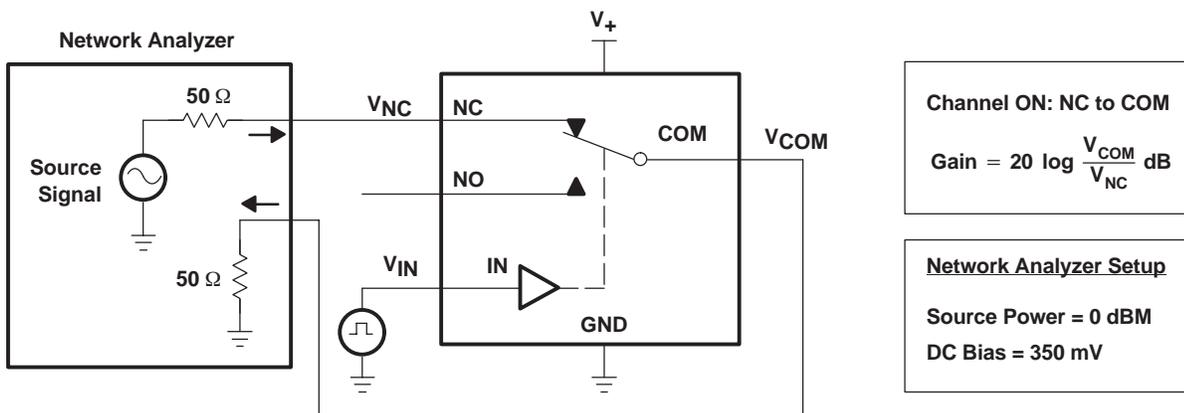


Figure 15. Frequency Response (BW)

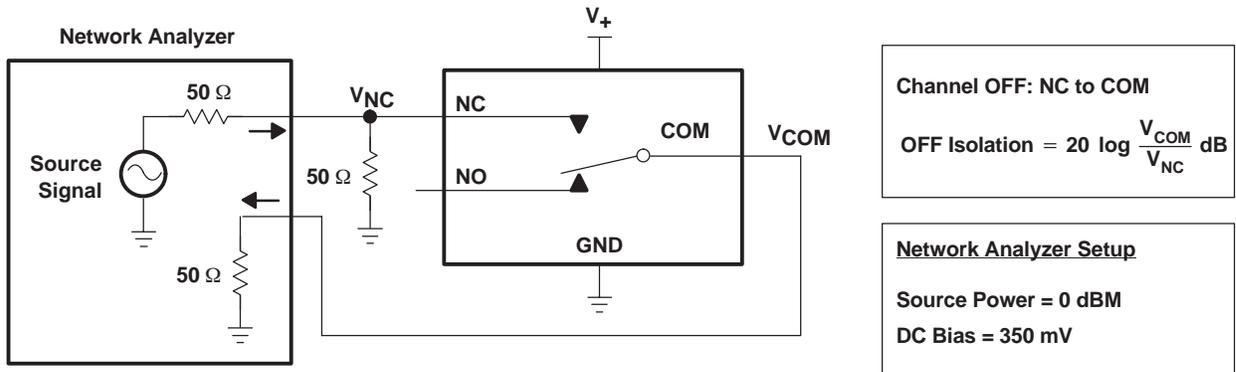


Figure 16. OFF Isolation (O_{ISO})

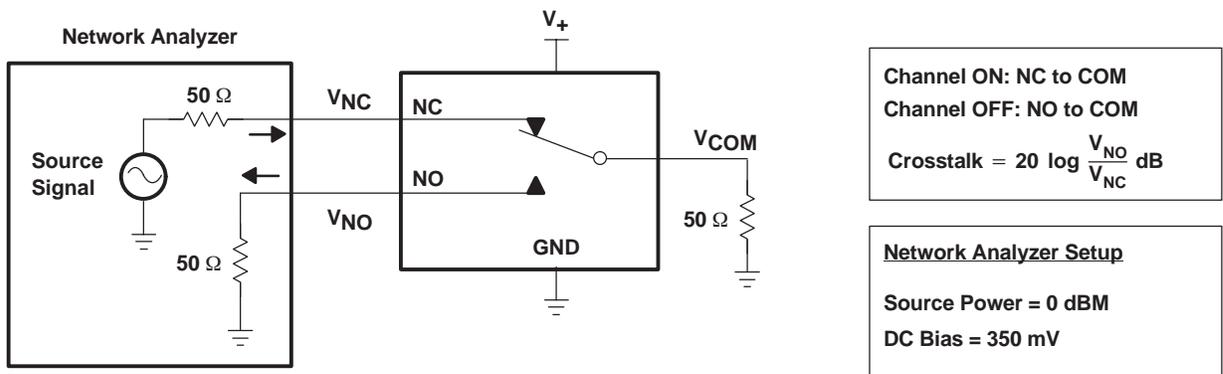


Figure 17. Crosstalk (X_{TALK})

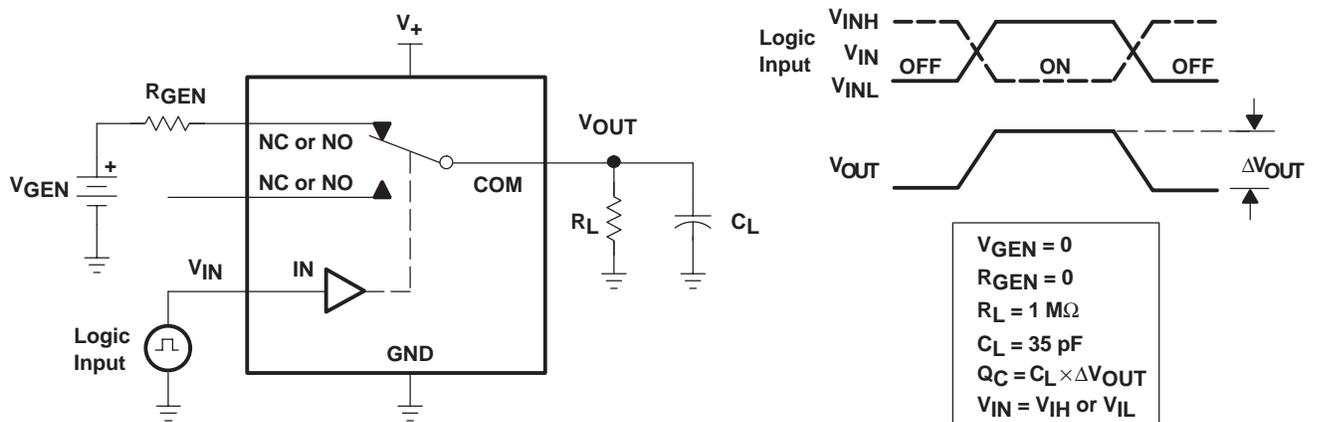


Figure 18. Charge Injection (Q_C)

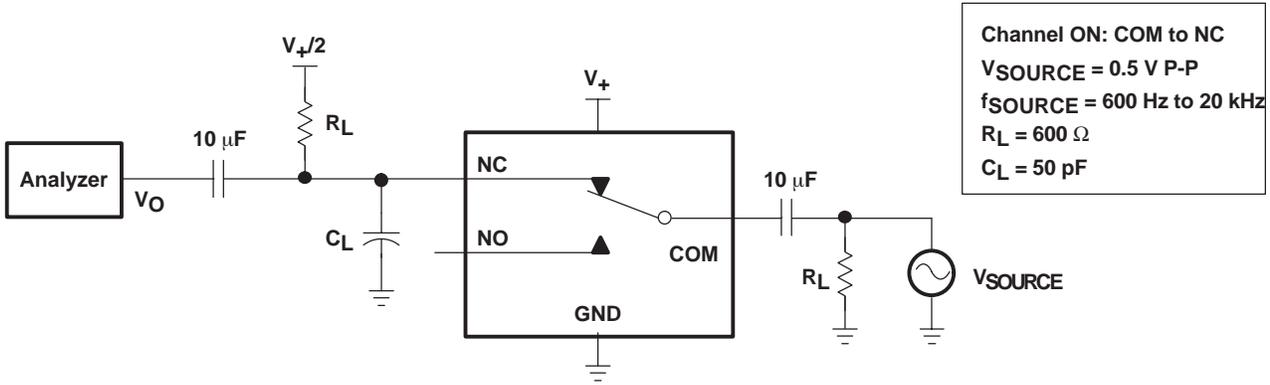
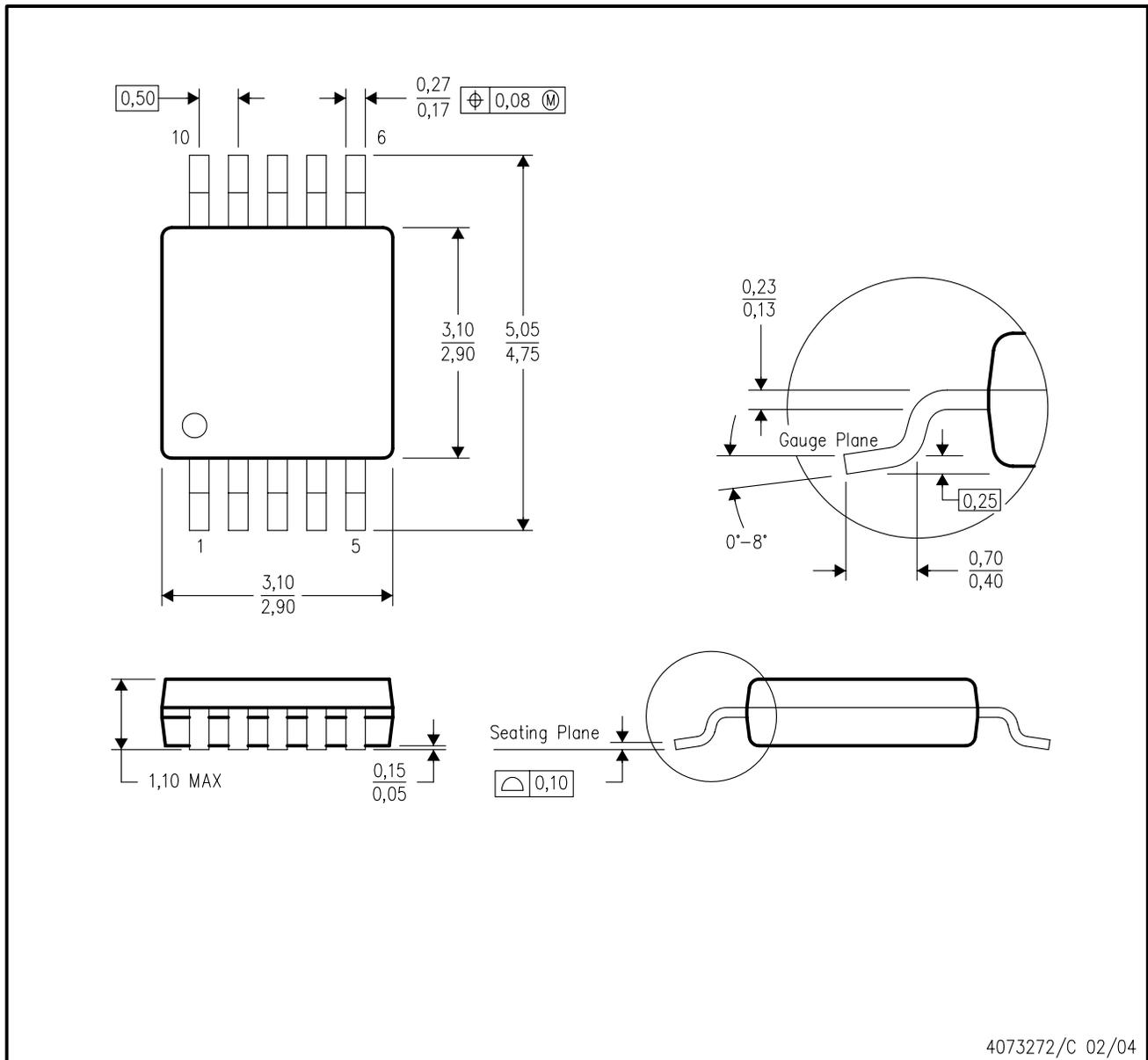


Figure 19. Total Harmonic Distortion (THD)

DGS (S-PDSO-G10)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion.
 - D. Falls within JEDEC MO-187 variation BA.

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