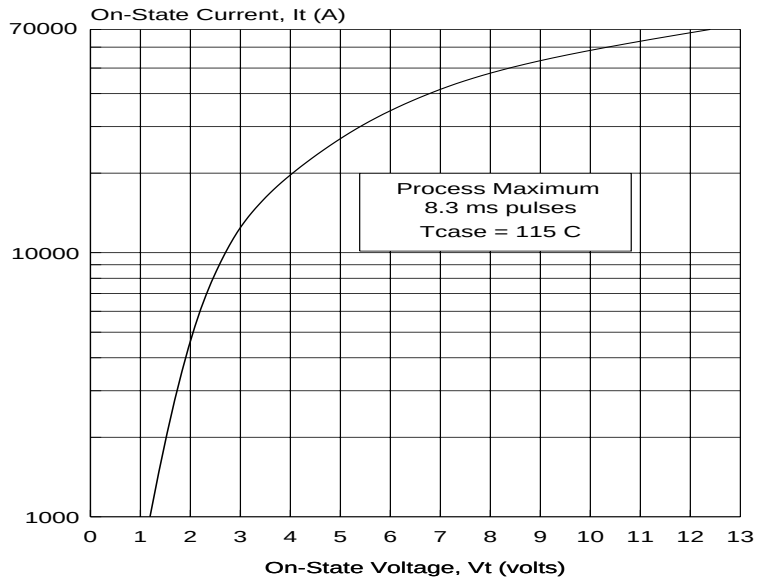
SPT401 125mm THYRISTOR
5000V 5000A

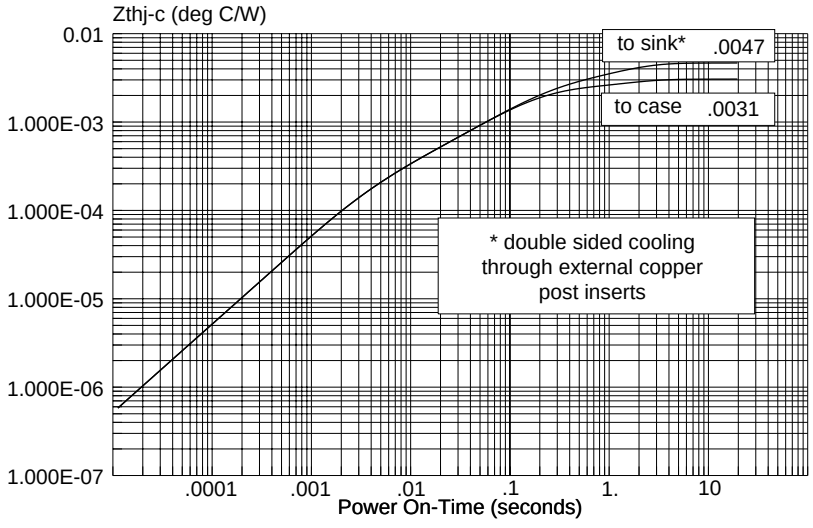
Type SPT401 thyristor is suitable for phase control applications such as for HVDC valves, static VAR compensators and synchronous motor drives. A second generation pilot gate and a unique orientation of emitter shorts are employed which promote the lateral expansion of conducting plasma resulting in lower spreading losses and high dv/dt withstand. It is supplied in a **reliable plastic light weight package**. The design utilizes SPCO's revolutionary "Lightweight Silicon Sandwich", **LSS** technology, a new termination technique which eliminates heavy refractory metal as a substrate while retaining an alloyed anode interface necessary for high surge current duty. External posts are available for adjoining commercially available heat dissipators using clamping hardware.

ON-STATE CHARACTERISTIC
Process Maximum



96d:t401onst

THERMAL IMPEDANCE vs. ON-TIME



7/1/97 rev 96d:

Maximum Off-State & Reverse Blocking Voltage Ratings

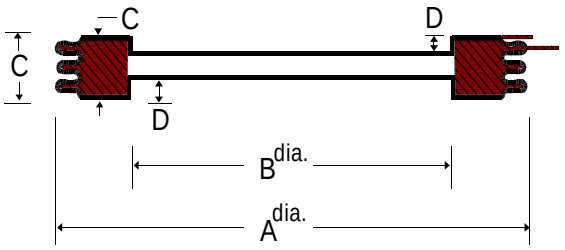
T_J = 0 to 115°C

	V_{DRM} (volts)	V_{RRM} (volts)
SPT401HT	5000	5000
SPT401HS	4900	4900
SPT401HR	4800	4800
SPT401HP	4700	4700
SPT401HM	4600	4600
SPT401HK	4500	4500

External clamping force
25000 lb minimum

Optional external posts drw.# 0215B8315
Ni plated copper, 0.35" thick each.
Compressed thickness including external posts
0.89" - 0.90"

Weight: 18 oz
3 lb 10 oz with posts



Nominal Dimensions

	inch	mm
A dia.	6 13/32	162.7
B dia.	4 3/16	106.4
C	51/64	20.24
D	0.2961	7.52

Rev 5 2/10/2000

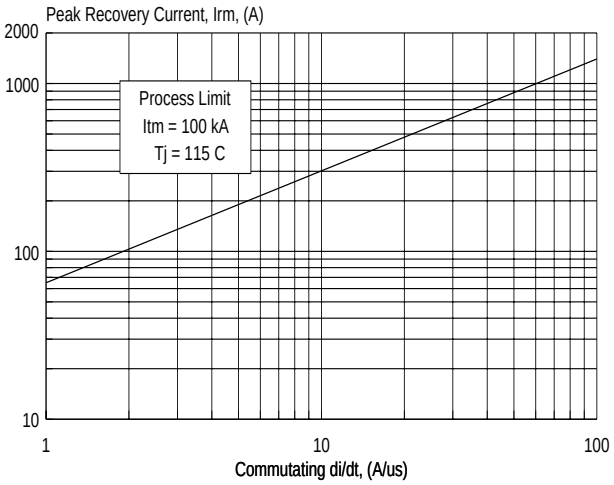
97c:pm5

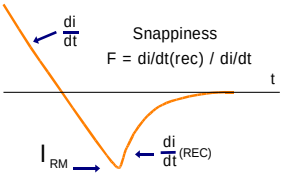
175 GREAT VALLEY PKWY. MALVERN, PA 19355
USA

LIMITING CHARACTERISTICS AND RATINGS

Repetitive peak off-state & reverse volts	V_{DRM} V_{RRM}	T_J=0 to 115°C	up to 5000	V
Repetitive working crest voltage	V_{DWM} V_{RWM}	T_J=0 to 115°C	0.8V_{DRM} 0.8V_{RRM}	V
Peak off-state & reverse current	I_{DWM} I_{RWM}	T_J=0 to 115°C	250 100	ma
Average on-state current	$I_{T(AV)}$	T_{case}= 70°C	5000	A
Peak half-cycle non-rep surge current	I_{TSM}	8.3 ms 1.5 ms T_J=115°C	70 105	kA
On-state voltage	V_{TM}	I_T=4000A t_p=8.3ms T_J=115°C	1.80	V
Critical gate trigger current / voltage	I_{GT} V_{GT}	V_D = 12 V T_J = 25°C	150 5.0	ma V
Non-trigger gate current	I_{GD} V_{GD}	V_D = 2000V T_J= 115°C	15 0.8	ma V
Maximum peak recovery current	I_{RM}	di/dt = 2 A/us T_J = 115°C	110 snappiness	A F = 2-3
Critical rate of rise of on-state current	di/dt rep	T_J=115°C 60 Hz with 60A snubber discharge	100	A/us
Critical rate of rise of off-state voltage	dv/dt	T_J=115°C V_D= 67% V_{DRM}	1000	V/us
Turn-on delay	t_d	V_D= 50%V_{DRM} T_J=115°C	4	us
Turn-off time	T_{off}	5A/us, -100V 20V/us to 2000V	400	us

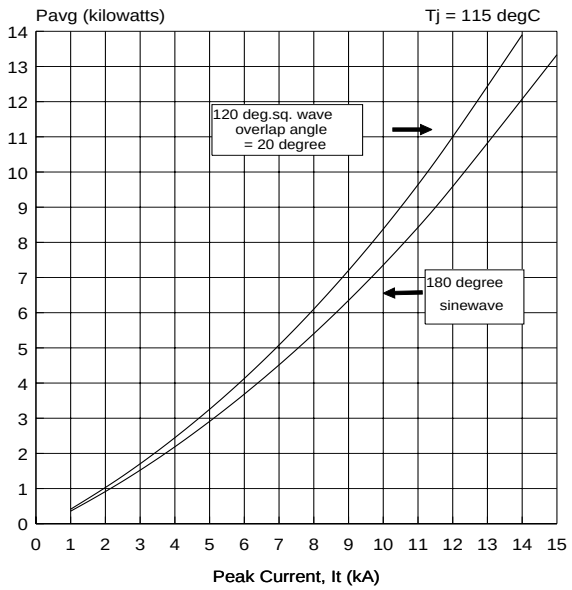
Peak Recovery Current Relationship with Commutating di/dt





Recommended gate drive to sustain turn-on di/dt rating
V_{OC} = 50 V
I_{SS} = 5 A
rise time = 0.5 us
duration 10 - 20 us

FULL CYCLE AVERAGE POWER LOSS
versus
PEAK CURRENT at 50/60 Hz
(plasma spreading and conduction loss)



FULL CYCLE AVERAGE POWER LOSS
50 / 60 Hz T_J = 115°C

I_T (peak)	half-sine 180°	3ph 120°
amperes	watts	watts
1000	359	414
2000	900	1013
3000	1511	1689
4000	2179	2432
5000	2900	3242
6000	3676	4119
7000	4506	5068
8000	5393	6090
9000	6339	7188
10000	7345	8365
11000	8414	9623
12000	9545	10964
13000	10742	12390
14000	12005	13902
15000	13335	15503