DATA SHEET

TEA1504
GreenChip™ SMPS control IC

Preliminary specification
Supersedes data of 1998 Mar 17
File under Integrated Circuits, IC11

1999 Dec 07

Philips
Semiconductors

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FEATURES

Distinctive features

- High level of integration reduces the number of components by up to 50 compared to power supply using discrete components
- On/off functional switch replaces expensive mains switch
- Direct off-line operation (90 to 276 V AC)
- 5% accurate on-chip oscillator.

Green features

- Low power consumption in off-mode (<100 mW)
- Fast and efficient on-chip start-up current source
- Burst mode standby (<2 W) for overall improved system efficiency
- Low power operation mode with lower frequency reduces switching losses
- Low Overcurrent Protection (OCP) level.

Protection features

- Demagnetization protection
- Cycle-by-cycle current limitation with programmable current trip level
- Overvoltage protection
- Overtemperature protection
- Safe-restart mode with reduced power for system fault conditions.

Highly versatile

- Usable in buck and flyback topology
- Interfaces both primary and secondary side feedback.

GENERAL DESCRIPTION

The GreenChip™ TEA1504 is intended for off-line 90 to 276 V (AC) power supply applications. It is one of a family of high voltage ICs integrating both analog and digital circuit functions for controlling a switched mode power supply (SMPS). Its functions include integrated high voltage start-up current source, voltage Pulse Width Mode (PWM) control, 5% accurate oscillator, band-gap derived reference voltages, comprehensive fault protection and leading edge blanking. Its high level of integration allows power supplies to be cost effective, compact, lightweight, highly efficient, more reliable, and simple to design. Efficient green features permit very low power operation modes, and an innovative on/off function allows an expensive mains switch to be replaced with a low-cost functional switch.

THE GREENCHIP™ FAMILY

The GreenChip™ family of ICs are fully integrated with most common PWM functions such as error amplifier, oscillator, bias current generator and band-gap based reference voltage circuits. The high level of integration allows easy and cost effective power supply design.
The ICs are made by a Philips proprietary high voltage BCDMOS process which produces low voltage circuit devices with inputs that are able to withstand up to 720 V.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA1504	DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1

BLOCK DIAGRAM

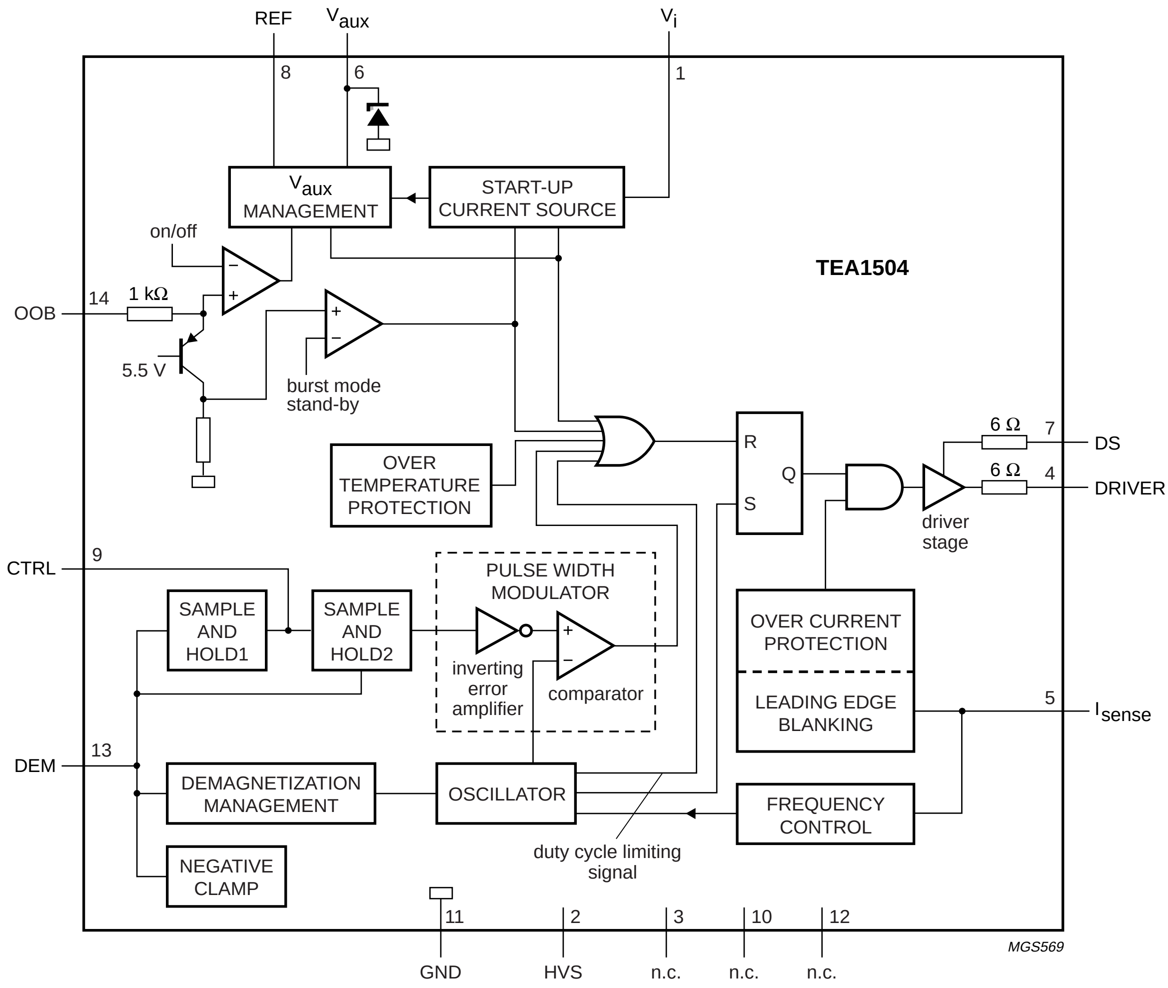


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_i	1	start-up current source input; connects to MOSFET Drain supply
HVS	2	high voltage safety spacer
n.c.	3	not connected
DRIVER	4	driver output; connects to Gate of power MOSFET
I_{sense}	5	current sense input; connects to current sense resistor
V_{aux}	6	IC supply; connects to supply capacitor
DS	7	internal driver supply
REF	8	reference input; connects to reference resistor for setting internal reference currents
CTRL	9	duty cycle control input
n.c.	10	not connected
GND	11	ground
n.c.	12	not connected
DEM	13	demagnetization signal input
OOB	14	burst mode standby on/off control signal input

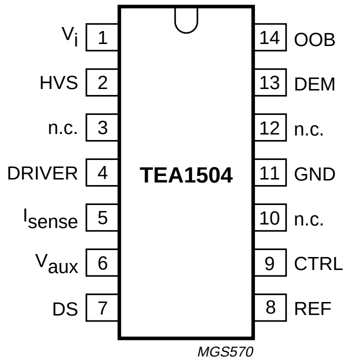


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

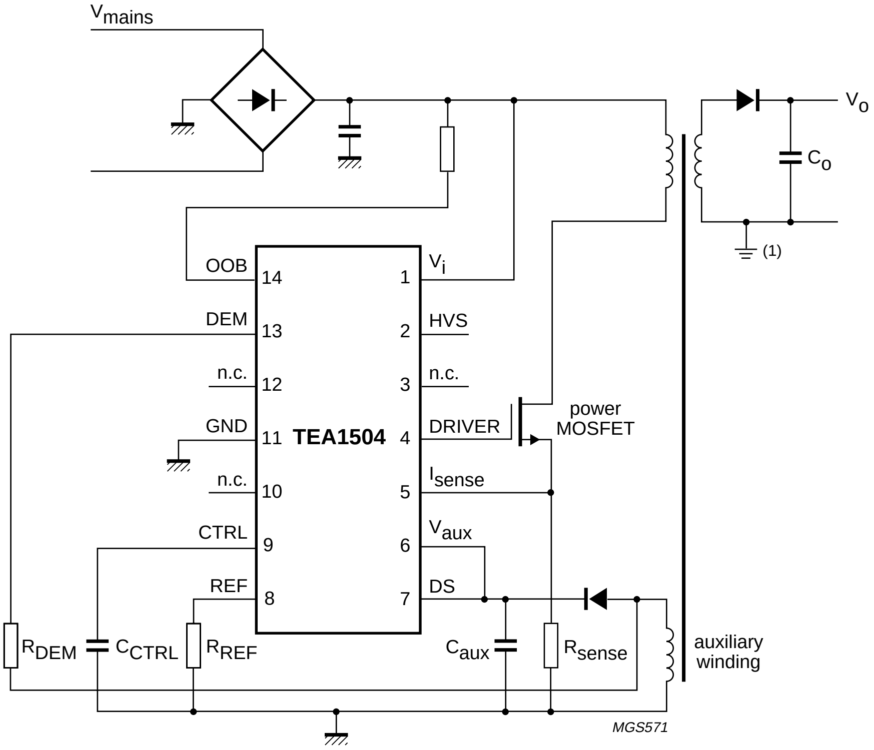
Negligible power is dissipated by the TEA1504 after start-up, due to its fast and efficient start-up circuit. It has an accurate saw tooth oscillator whose output signal is compared with a voltage feedback control circuit to generate a pulse width modulated signal for driving the Gate of an external power MOSFET. The number of external components required for regulating the supply are reduced due to an innovative design implementing both primary and secondary side regulation. Overvoltage, overcurrent, overtemperature and demagnetization features protect the IC from system fault conditions. Off-mode, Burst mode standby, and a Low power operation mode are advanced features that greatly enhance the efficiency of the overall system. Off-mode, reduces the power consumption of the IC below 100 mW. Burst mode standby, reduces the power consumption of the system to below 2 W. Low power operation mode, reduces the operating frequency of the system during low load conditions to reduce switching losses.

Start-up current source and V_{aux} management

A versatile on-chip start-up current source eliminates the need for an external, highly dissipative trickle-charge circuit. See Figs 1 and 3. The start-up current source is supplied by rectified mains power via V_i (pin 1). It supplies charging current to the IC supply capacitor (C_{aux}) and also supplies current to the IC control circuit (V_{aux} management) (see $I_{start(Vaux)L}$ and $I_{start(Vaux)H}$ in Chapter “Characteristics”). Once C_{aux} is charged to its start-up voltage level (11 V), the oscillator starts oscillating and the IC starts switching the power MOSFET. Power is then supplied to the load via the secondary winding. C_{aux} is also supplied by an auxiliary winding on the primary side which is coupled to the secondary winding supplying the output capacitor (C_o). As the voltage on C_o increases and approaches its nominal value, C_{aux} is re-supplied with current by the auxiliary winding (see Fig.4). For correct operation, it is important that C_{aux} starts to be re-supplied with current by the auxiliary winding before its voltage drops to the Under Voltage Lockout (UVLO) level of 8.05 V.

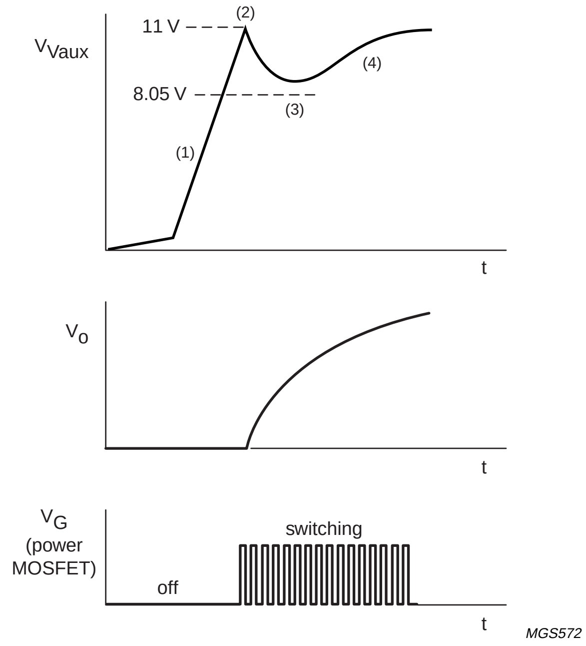
The start-up current source also helps to implement the safe-restart or ‘hiccup’ mode required during system fault conditions: output short-circuit, output open-circuit, and overvoltage. Under these fault conditions, the IC inhibits the normal operation of the system and stops delivering output power. If the output is short-circuited, C_{aux} is no longer supplied by the auxiliary winding and its voltage drops to the UVLO level. If the output open-circuits, the output voltage rises to the Overvoltage Protection (OVP) level. The IC detects this state and stops switching the power MOSFET, which stops re-supplying current to C_{aux} whose voltage starts to drop. Once the voltage on C_{aux} drops to the UVLO level, the start-up current source re-activates and charges C_{aux} to the start-up level, and the system begins the safe-restart mode cycle, similar to the normal start-up cycle.

Figure 5 shows the relevant waveforms during safe-restart mode. To achieve a low ‘hiccup’ duty cycle, the current charging C_{aux} during the safe-restart mode is lower than it is during normal start-up (see $I_{restart(Vaux)}$ and $I_{start(Vaux)H}$ in Chapter “Characteristics”). This reduces the risk, during an output short-circuit condition, of any physical damage being caused to output secondary winding devices, and of any breach of safety. The start-up current source is also important for implementing burst mode standby, explained in Section “Burst mode standby” (see $I_{restart(Vaux)}$ in Chapter “Characteristics”).



(1) Secondary earthing points are isolated from their primary earthing points.

Fig.3 Typical flyback application.



(1) Start-up current source charges C_{aux}.
(2) Start-up voltage.
(3) UVLO level.
(4) Auxiliary winding charges C_{aux}.

Fig.4 Normal start-up waveforms.

Reference

All reference voltages are derived from a temperature compensated, on-chip, band-gap. The band-gap reference voltage is also used with an external resistor (R_{REF}) connected to REF (pin 8), to generate accurate, temperature independent, IC internal bias currents. $I_{REF} = \frac{V_{REF}}{R_{REF}}[A]$.

R_{REF} also affects the frequency of the oscillator (see Section “Oscillator”).

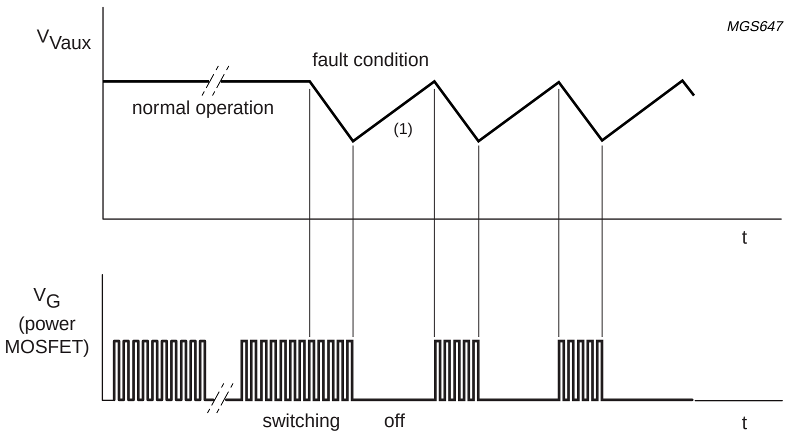
Sample-and-hold

The TEA1504 uses voltage feedback with an innovative sample-and-hold circuit to regulate the output voltage. In a primary feedback configuration, the sample-and-hold circuit samples the current into DEM (pin 13), fed by R_{DEM}, which relates to the output voltage (V_o) during the period that current flows in the secondary winding.

$aV_o = I_{REF} \times R_{DEM} + V_{clamp(DEM)(pos)}$.

$V_{clamp(DEM)(pos)}$ is specified in Chapter “Characteristics”; ‘a’ = a constant determined by the turns ratio of the transformer.

The sampled current is held in the external capacitor (C_{CTRL}). The PWM uses the voltage on C_{CTRL} to set the operating duty cycle of the power MOSFET. When the TEA1504 is used in a secondary feedback configuration, the feedback voltage is provided by an opto-coupler.



(1) Start-up current source charges C_{aux}.

Fig.5 Safe-restart mode waveforms.

Pulse width modulator

The PWM comprises an inverting error amplifier and a comparator (see Fig.1) which drives the power MOSFET with a duty cycle that is inversely proportional to the voltage at CTRL (pin 9). A signal from the oscillator sets a latch that turns on the power MOSFET. The latch is then reset either by the signal from the PWM or by a duty cycle limiting signal from the oscillator. The latch stops the power MOSFET from being switched incorrectly if the PWM output signal becomes unstable. The maximum duty cycle is internally set to 80%. The IC switching signals during normal operation are shown in Fig.7.

Oscillator

The oscillator determines the switching duty cycle.
Its ramp signal voltage is compared to the output of the error amplifier by the PWM. The fully integrated oscillator circuit works by charging and discharging an internal capacitor between two voltage levels to create a sawtooth waveform with a rising edge that is 80% of the oscillator period (high frequency mode). This ratio sets a maximum switching duty cycle of 80% for the IC. The accuracy of the oscillator frequency is internally set to 5%. Its frequency can be adjusted between 50 and 100 kHz by changing the value of R_{REF}. This gives the power supply designer greater flexibility in the choice of system components. The relationship between frequency and the value of R_{REF} is shown in Fig.6. The range of R_{REF} values and the frequencies of f_{oscL} and f_{oscH} are specified in Chapter “Characteristics”.

Multi frequency control

When the power supply operates at or below $\frac{1}{9}$ of its peak power, the IC changes to low power operation mode. This lowers the frequency of the oscillator to reduce the power supply switching losses. The ratio between the high and the low oscillator frequency is maintained at 1 : 2.5 (see f_{oscL} in Chapter “Characteristics”). An innovative design ensures that the transfer from high-to-low frequency and vice versa does not effect output voltage regulation.

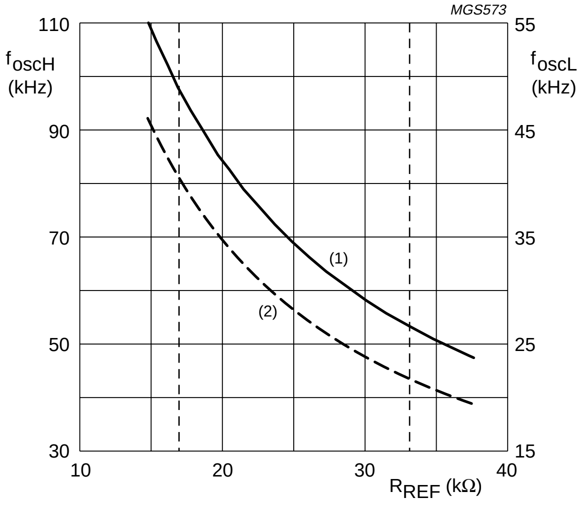
Gate driver

The driver circuit to the Gate of the power MOSFET has a totem-pole output stage that has current sourcing capability of 120 mA and a current sink capability of 550 mA. This permits fast turn-on and turn-off of the power MOSFET for efficient operation. This circuit design allows the power supply designer to control the source and sink currents of the Gate driver circuit with a minimum number of external components.

A low driver source current has been chosen in order to limit the $\Delta V/\Delta t$ at switch-on. This reduces Electro Magnetic Interference (EMI) and also the current spike across R_{sense}.

Demagnetization protection

The demagnetization protection feature ensures discontinuous conduction of the power supply, simplifying the design of feedback control and giving a faster transient response. It protects against saturation of the transformer/inductor and also protects the power supply components against excessive stresses at start-up, when all energy storage components are completely discharged. During a system output short-circuit fault condition, it provides cycle-by-cycle protection of the converter configuration. The demagnetization resistor (R_{DEM}) value can be calculated using the formula given in Section “Sample-and-hold”.



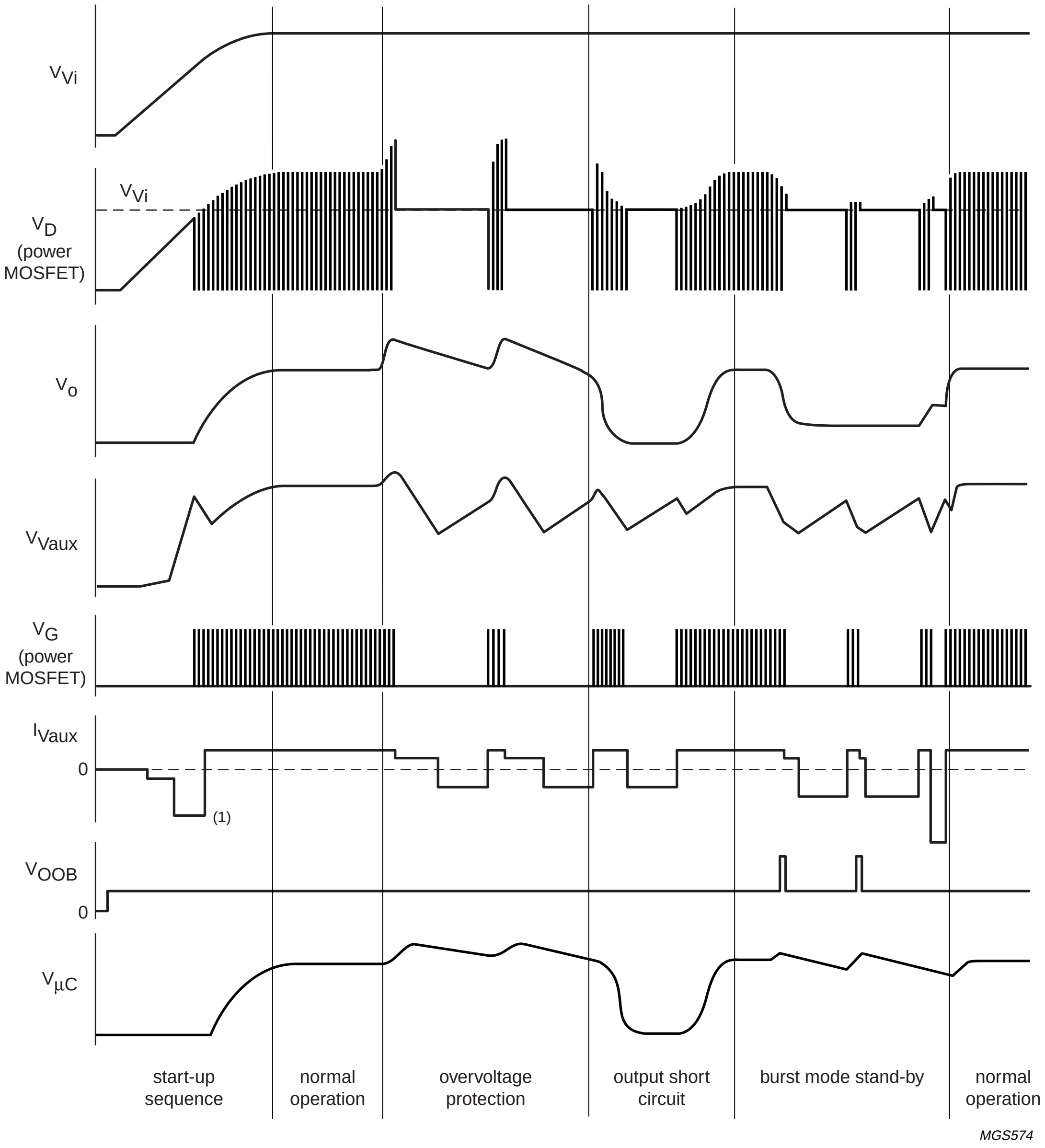
(1) High frequency mode.

(2) Low frequency mode.

Fig.6 Frequency as function of R_{REF} value.

Negative clamp

The negative clamp circuit ensures correct operation of the IC by preventing the voltage at DEM (pin 13) dropping below –0.45 V, during the period when the power MOSFET turns on and the auxiliary winding voltage goes negative.



(1) All negative currents flow out of the IC.

Fig.7 Typical waveforms.

Overvoltage protection

The OVP circuit senses the voltage at V_{aux} (pin 6). If the output voltage exceeds the preset voltage limit, the OVP circuit turns off the power MOSFET preventing the re-supply of current to C_{aux}. V_{Vaux} drops to the UVLO level and the system enters the low dissipation safe-restart mode described earlier. The system recovers from the safe-restart mode only if the OVP condition is removed.

Overcurrent protection

Cycle-by-cycle OCP is provided by sensing the voltage on R_{sense}. The voltage on R_{sense} relates to the amplitude of the primary current, and is internally compared with a reference voltage using a high speed comparator.
The comparator threshold voltage is specified as $V_{th(Isense)}$ in the Chapter “Characteristics”.

The maximum primary (protection) current is therefore:

$$I_{prot} = \frac{V_{th(Isense)}}{R_{sense}}[A] .$$

If the power MOSFET current exceeds the current limit, the comparator changes state, turning off the power MOSFET. The power MOSFET is typically turned off in 210 ns (see $t_{d(Isense\text{-}DRIVER)}$ in Chapter “Characteristics”).

Having R_{sense} off-chip allows the power supply designer greater flexibility for programming the OCP threshold level. It also reduces the risk of an overcurrent condition being sensed incorrectly. When the power MOSFET turns on, the discharge current from the demagnetization $\Delta V/\Delta t$ limiting capacitor, flows through the power MOSFET instead of through R_{sense}.

The Leading Edge Blanking circuit inhibits the operation of the OCP comparator for a short period when the power MOSFET turns on (see $t_{blank(le)}$ in Chapter “Characteristics”). This ensures that the power MOSFET is not turned off prematurely due to the false sensing of an overcurrent condition caused by current spikes produced by the discharge of primary-side snubber and parasitic capacitances. The $t_{blank(le)}$ is not fixed and tracks the oscillator frequency.

Overtemperature protection

Overtemperature protection is provided by an analog temperature sensing circuit which turns off the power MOSFET when the temperature exceeds typically 140 °C.

On/off mode

The on/off mode allows an expensive mains switch to be replaced by an in-expensive functional switch.

Figure 8 shows a flyback converter configured to use the on/off mode. Switch S1 connects OOB (pin 14) to either a voltage close to ground, or to a voltage typically greater than 2.5 V. The OOB voltage is detected internally by the IC. If V_{OOB} is low, the IC enters the off-mode, consuming a current of typically 350 μA (see $I_{off(Vi)}$ in Chapter “Characteristics”). If V_{OOB} is typically 2.5 V, the IC enters the start-up sequence and begins normal operation (see $V_{th(on/off)}$ in Chapter “Characteristics”).
Figure 9 shows a ‘Mains Under Voltage Lock Out’ (MUVLO) circuit using 3 resistors. Assuming that R3 is chosen to be a very high value, the IC starts operating when: $V_{mains} \approx \frac{R1}{R2} \times V_{OOB}[V]$; where R1 >> R2.

This ensures that the power supply only starts working above a V_{mains} of 80 V for example. The bleeder current through R1 should be low (e.g. 30 μA at 300 V).

Burst mode standby

OOB (pin 14) is also used to implement the burst mode standby. In burst mode standby, the power supply enters a special low dissipation state where it typically consumes less than 2 W of power. Figure 9 shows a flyback converter using the burst mode standby function.
The system enters burst mode standby when the microcontroller closes switches S2 and S3 on the secondary side. Switch S2 connects the output secondary winding to microcontroller capacitor ($C_{\mu C}$) bypassing C_o. When the voltage on ($C_{\mu C}$) exceeds the zener voltage, the opto-coupler is activated sending a signal to OOB.
In response to this signal, the IC stops switching and enters a ‘hiccup’ mode. Figure 7 shows the burst-mode standby signals. The hiccup mode during burst mode standby operation differs from the hiccup mode in safe-restart mode during a system fault condition.
For safe-restart mode, the power has to be reduced. Burst mode standby requires sufficient power to supply the microcontroller. To prevent transformer rattle, the transformer peak current is reduced by a factor of 3. Burst mode standby operation continues until the microcontroller opens switches S2 and S3. The system then enters the start-up sequence and begins normal switching behaviour.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); note 1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_i	DC voltage on pin V_i	measured at 200 μA	–	720	V
V_{OOB}	voltage on pin OOB		–0.3	+14	V
I_{DEM}	current on pin DEM		–	±1	mA
V_{CTRL}	voltage on pin CTRL		–0.3	+5	V
V_{Isense}	voltage on pin I_{sense}		–0.3	+5	V
I_{REF}	current on pin REF		–	–1	mA
V_{Vaux}	voltage on pin V_{aux}		–0.3	+18	V
V_{DS}	voltage on pin DS		–0.3	+18	V
T_j	junction temperature		–10	+140	°C
T_{stg}	storage temperature		–40	+150	°C
V_{esd}	electrostatic discharge	class 1			
	human body model	note 2	–	1250	V
	machine model	note 3	–	200	V

Notes

1. All voltages are referenced to GND (pin 11).
2. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.
3. Equivalent to discharging a 200 pF capacitor through a 0.75 mH coil.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	70	K/W

QUALITY SPECIFICATION

Quality specification *“SNW-FQ-611 part E”* is applicable.

CHARACTERISTICS

T_j = –10 to +110 °C; V_{Vi} = 300 V; R_{REF} = 24.9 kΩ (0.1%); V_{Vaux} = 8.6 to 13 V. Positive currents flow into the IC. Negative currents flow out of the IC. All voltages are referenced to GND (pin 11).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Start-up current source and V_{aux} management (pins 1 and 6)						
$V_{start(Vi)(min)}$	minimum start-up voltage on V_i		100	–	–	V
$V_{start(Vaux)}$	start-up voltage on V_{aux}		10.4	11	11.6	V
$V_{UVLO(Vaux)}$	under-voltage lockout on V_{aux}		7.4	8.05	8.6	V
$V_{hys(Vaux)}$	hysteresis voltage on V_{aux}	$V_{start(Vaux)} – V_{UVLO(Vaux)}$	2.60	2.95	3.30	V
$I_{i(Vi)}$	input current on V_i	normal operation	20	60	100	μA
$I_{off(Vi)}$	off mode current on V_i	V_{OOB} < 1.95 V	150	350	550	μA
$I_{start(Vaux)L}$	low start-up current on V_{aux}	0 V < V_{Vaux} < 0.73 V	–270	–230	–190	μA
$I_{start(Vaux)H}$	high start-up current on V_{aux}	0.5 V < V_{Vaux} < $V_{start(Vaux)}$	–5.0	–3.0	–1.0	mA
$I_{sup(Vaux)(oper)}$	operating supply current on V_{aux}	no load on DRIVER (pin 4)	3.5	3.85	4.2	mA
$I_{restart(Vaux)}$	restart current on V_{aux}	in OCP mode	–600	–530	–460	μA
		in burst standby mode	–2.5	–2.1	–1.7	mA
$V_{clamp(Vaux)}$	clamping voltage on V_{aux}	I_{Vaux} = 5 mA	15	–	18	V
Reference input (pin 8)						
$V_{i(REF)}$	reference input voltage		2.37	2.47	2.57	V
$R_{REF(oper)}$	operating reference resistor		16.9	24.9	33.2	kΩ
Oscillator						
f_{oscL}	oscillator low frequency	low power operation mode	27.5	29	30.5	kHz
f_{oscH}	oscillator high frequency	normal mode	66	70	74	kHz
δ_{max}	maximum duty cycle	$f = f_{oscH}$	78	80	82	%
f_{oscH}/f_{oscL}	ratio between oscillator high and low frequencies		2.30	2.45	2.60	
Δf_{oscH}	oscillator high frequency range	with changing R_{REF}	50	70	100	kHz
Demagnetization management (pin 13)						
$V_{th(DEM)}$	demagnetization comparator threshold voltage on DEM	V_{DEM} decreasing	50	65	80	mV
$t_{P(DEM-BUF)}$	propagation delay from DEM to output buffer		300	500	700	ns
$I_{i(bias)(DEM)}$	input bias current on DEM	V_{DEM} = 65 mV	–0.5(1)	–	–0.1(1)	μA
$V_{clamp(DEM)(neg)}$	negative clamp voltage level on DEM	I_{DEM} = –500 μA	–0.45	–0.35	0	V
$V_{clamp(DEM)(pos)}$	positive clamp voltage level on DEM	I_{DEM} = 100 μA	2.3	2.6	2.9	V
Sample-and-hold (pin 13)						
$I_{ctrl(DEM)(oper)}$	operating control current on DEM	I_{REF} = 100 μA	90	100	110	μA
$I_{th(sample)}$	sample threshold current as % of $I_{ctrl(DEM)}$		78	83	88	%
$t_{P(DEM-COMP)}$	propagation delay from DEM to current comparator	$\Delta V_{DEM}/\Delta t$ positive (500 V/μs)	170	450	730	ns
		$\Delta V_{DEM}/\Delta t$ negative (10 V/μs)	20	90	160	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Overvoltage protection (pin 6)						
$V_{OVP(max)}$	maximum OVP voltage level	fixed maximum level	14.0	14.7	15.5	V
$t_{d(OVP)}$	OVP delay time		350	550	800	ns
I_{sense} Overcurrent protection and low power operation mode (pin 5)						
$t_{blank(le)}$	leading edge blanking time	$R_{REF} = 0.7 \times R_{REF(nominal)}$	180	260	340	ns
		$R_{REF} = R_{REF(nominal)}$	240	340	440	ns
		$R_{REF} = 1.3 \times R_{REF(nominal)}$	415	470	560	ns
$V_{th(Isense)}$	comparator threshold voltage on I_{sense}	at maximum current	0.46	0.49	0.53	V
$t_{d(Isense\text{-}DRIVER)}$	delay from I_{sense} to DRIVER (MOSFET off)	at $\Delta V/\Delta t$ = 200 mV/μs	150	210	270	ns
$V_{th(lpom)}$	threshold voltage for switch-over to low power operation mode		155	165	175	mV
Duty cycle control (pin 9)						
$\Delta\delta/\Delta V_{CTRL}$	variation of duty cycle with voltage on CTRL	f_{oscH}	95	85	75	%/V
		f_{oscL}	60	50	40	%/V
$V_{CTRL(min)}$	minimum control voltage on CTRL		2.00	2.15	2.30	V
$V_{CTRL(max)}$	maximum control voltage on CTRL		2.90	3.05	3.20	V
$I_{L(CTRL)}$	input/output leakage current on CTRL		–1(1)	–	+1(1)	μA
Overtemperature protection						
$T_{th(over)}$	threshold overtemperature		130	140	155	°C
On/off mode and burst mode standby (pin 14)						
$V_{th(on/off)}$	switch-over to on/off mode threshold voltage		2.3	2.5	2.8	V
$V_{th(burst)(on)}$	burst mode standby active threshold voltage		6.5	–	7.5	V
$V_{th(burst)(off)}$	burst mode standby inactive threshold voltage		–	–	5.5	V
$I_{O(OOB)}$	output current on OOB	V_{OOB} > 400 mV	–0.5(1)	–	–0.1(1)	μA
DRIVER (pin 4)						
R_{DSonH}	Drain/Source on-state resistance (output going high)	V_{Vaux} = 8.5 V and V_{DRIVER} = 6.5 V	15	22	50	Ω
R_{DSonL}	Drain/Source on-state resistance (output going low)	V_{Vaux} = 8.5 V and V_{DRIVER} = 2 V	3	6	15	Ω
I_{source}	source current of MOSFET	V_{Vaux} = 8.5 V and V_{DRIVER} = 2 V	–280	–120	–100	mA
I_{sink}	sink current of MOSFET	V_{Vaux} = 8.5 V and V_{DRIVER} = 2 V	150	250	500	mA
		V_{Vaux} = 8.5 V and V_{DRIVER} = 8.5 V	400	550	900	mA

Note

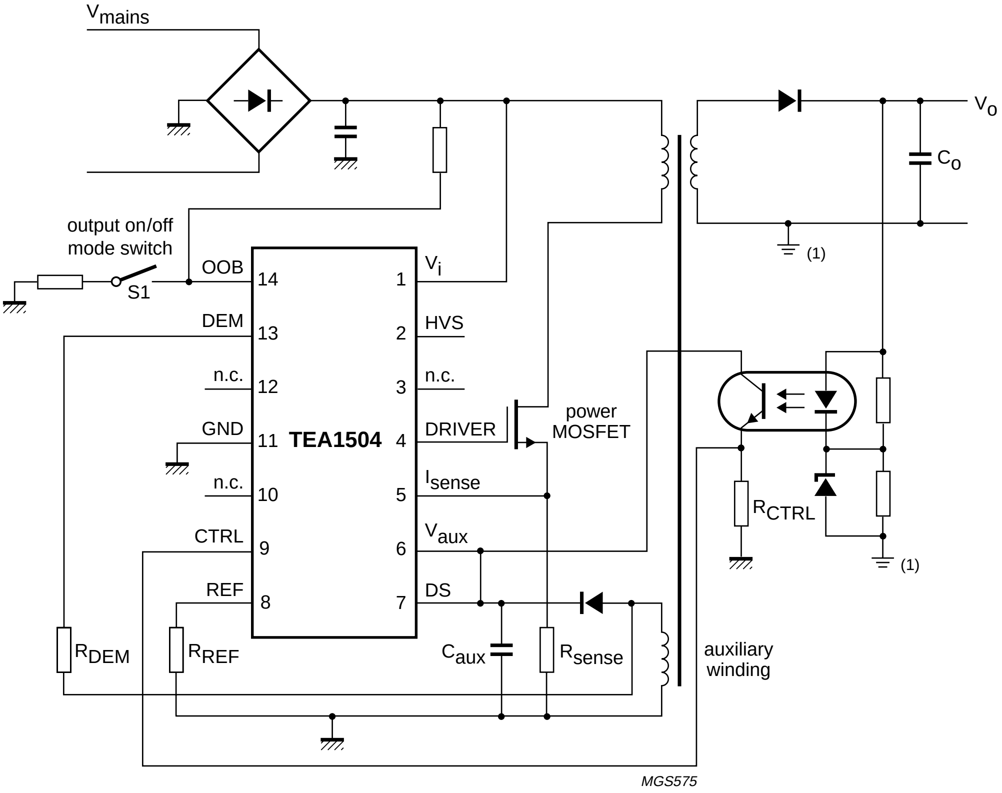
1. Guaranteed by design.

APPLICATION INFORMATION

A converter using the TEA1504 is usually either a flyback or a buck converter that comprises EMI filter, full bridge rectifier, filter capacitor, transformer, output stage(s) and some snubber circuitry. Depending upon the type of feedback used, either an auxiliary winding (primary regulation) or an opto-coupler (secondary regulation) is used. Very few external components are used due to the high level of chip integration. A sense resistor (R_{sense}) converts the primary current into a voltage at I_{sense} (pin 5). The IC uses this voltage to set the peak current of the converter. An auxiliary winding supplies capacitor C_{aux} which buffers the IC's internal supply. The auxiliary winding is also used as part of the primary output voltage regulation circuit. A resistor (R_{REF}) determines the IC's reference currents into REF (pin 8).

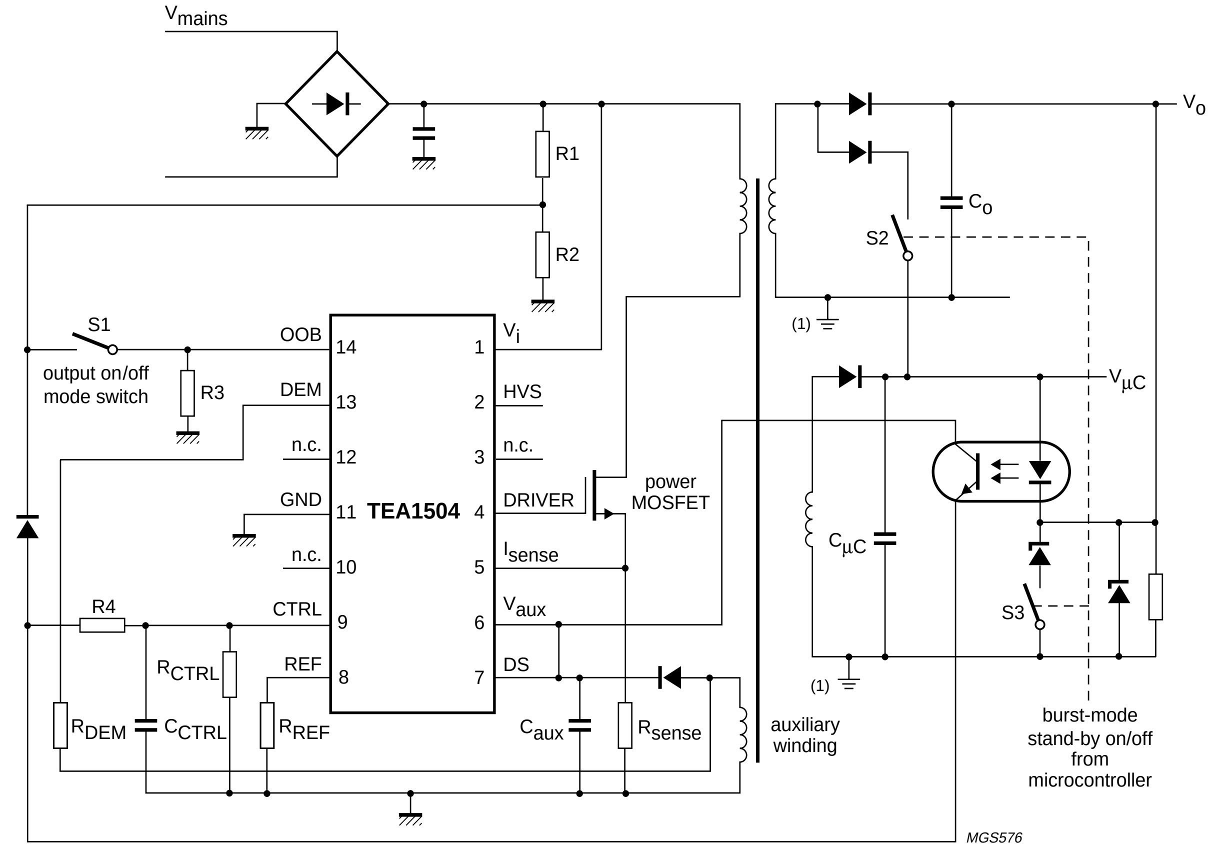
A capacitor (C_{CTRL}) having a low value of typically 0.2 to 2 nF is used by the internal sample-and-hold circuit to regulate the primary feedback circuit. C_{CTRL} is connected to CTRL (pin 9). This pin is also the input for the opto-coupler signal in a secondary sensing configuration. Pin 11 is connected to ground. The primary side auxiliary winding is connected by resistor (R_{DEM}) to DEM (pin 13). The DEM input is also used for primary side regulation. Input OOB (pin 14) implements both the on/off and the burst mode standby functions. The supply connected to V_i (pin 1) is used by the internal start-up current source for charging capacitor C_{aux} during start-up and safe-restart modes.

For additional information also see: *'application note AN98011: "200 W SMPS with TEA1504"*.



(1) Secondary earthing points are isolated from their primary earthing points.

Fig.8 Typical flyback configuration with secondary sensing and on/off feature.



(1) Secondary earthing points are isolated from their primary earthing points.

Fig.9 Flyback configuration with secondary sensing using the burst mode standby and on/off feature.

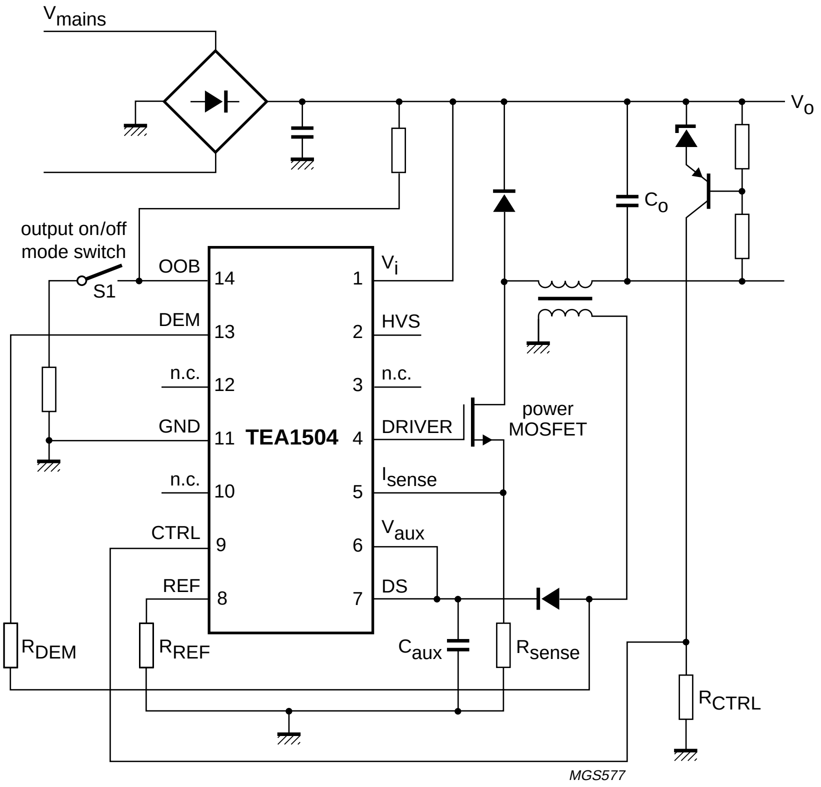


Fig.10 Typical buck configuration with secondary sensing.

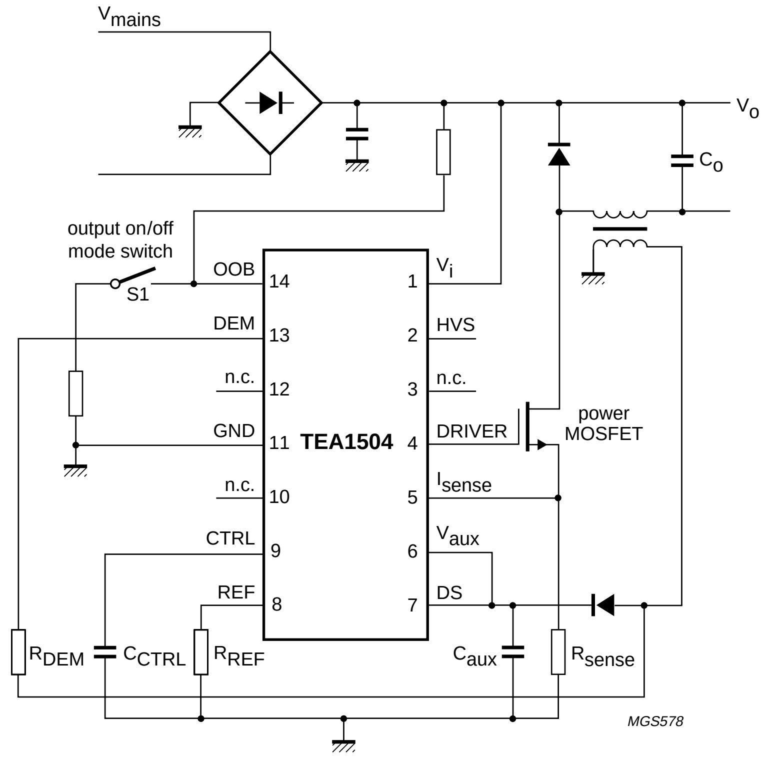
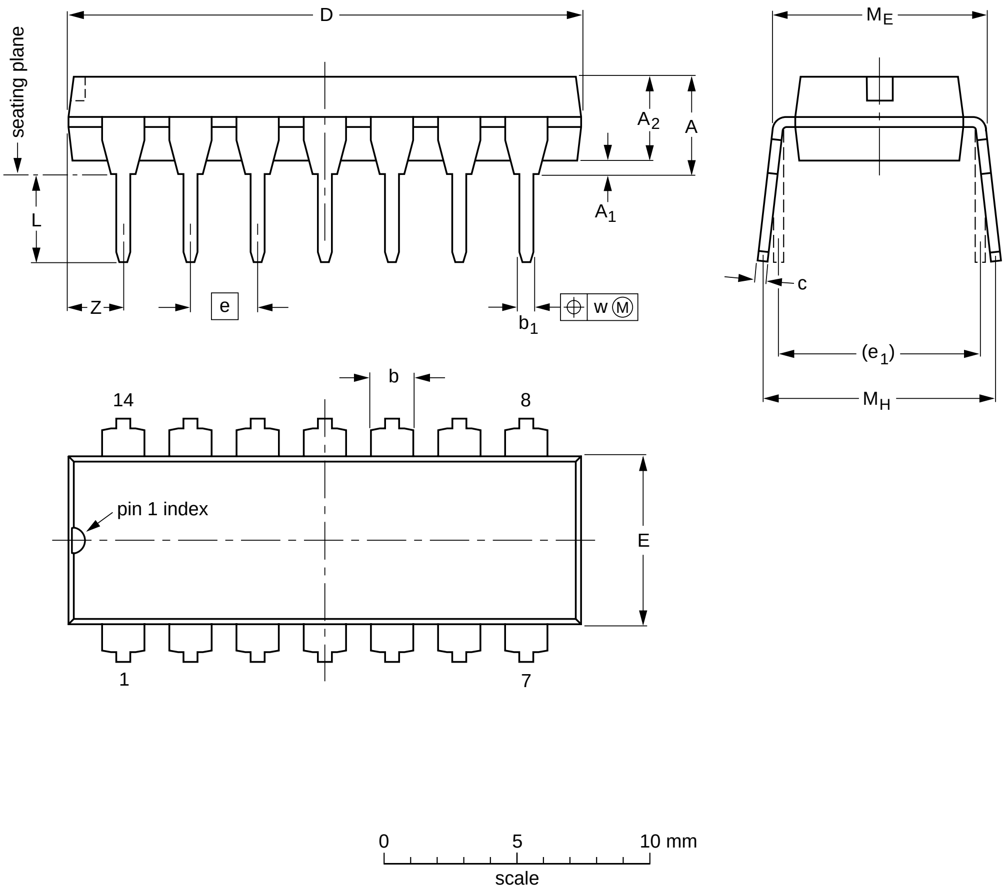


Fig.11 Typical buck configuration with primary sensing.

PACKAGE OUTLINE

DIP14: plastic dual in-line package; 14 leads (300 mil) SOT27-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.020	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT27-1	050G04	MO-001AA				~~92-11-17~~ 95-03-11

SOLDERING

Introduction to soldering through-hole mount packages

This text gives a brief insight to wave, dip and manual soldering. A more in-depth account of soldering ICs can be found in our *“Data Handbook IC26; Integrated Circuit Packages”* (document order number 9398 652 90011).

Wave soldering is the preferred method for mounting of through-hole mount IC packages on a printed-circuit board.

Soldering by dipping or by solder wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

Suitability of through-hole mount IC packages for dipping and wave soldering methods

PACKAGE	SOLDERING METHOD	
	DIPPING	WAVE
DBS, DIP, HDIP, SDIP, SIL	suitable	suitable[1]

Note

1. For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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