NEC

# BIPOLAR ANALOG INTEGRATED CIRCUIT

# μPC1853

## MATRIX SURROUND IC WITH I²C BUS

The μPC1853 is a phase shift matrix surround IC. Only 2 speakers on the front side implement wide sound expansion, and by adding rear speakers, rich three-dimensional sound can obtained.

The μPC1853 can perform all controls (mode switching, volume control and so on) through the I²C bus.

### FEATURES

- Any control is possible through the I²C bus.
- Surround effect can be realized by only 2 speakers on the front side.
- On-chip tone (bass and treble) control circuit.
- Level-adjustable output pin for heavy bass sound.
- Level-adjustable output pin for AV amplifier.
- μPC1853-01 : On-chip low boost circuit.
  On-chip volume and balance control circuits.
- μPC1853-02 : On-chip L-channel volume and R-channel volume control circuits.

### APPLICATION

- TV, audio

### ORDERING INFORMATION

| Part Number | Package |
|---|---|
| μPC1853CT-01 | 30-pin plastic shrink DIP (400 mil) |
| μPC1853CT-02 | 〃 |



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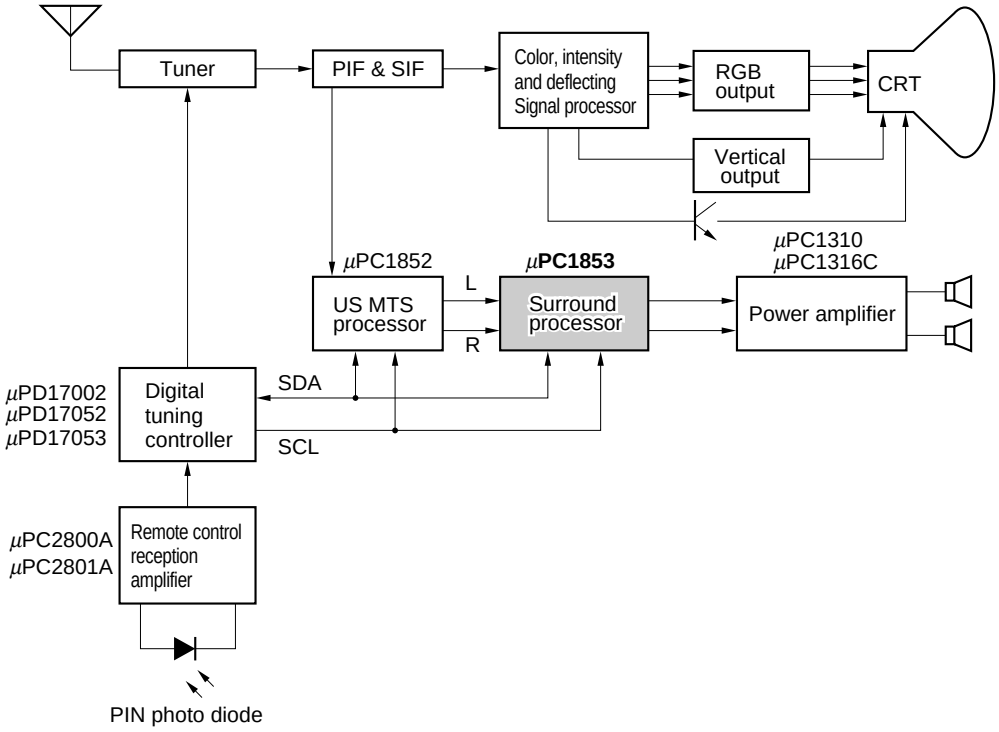
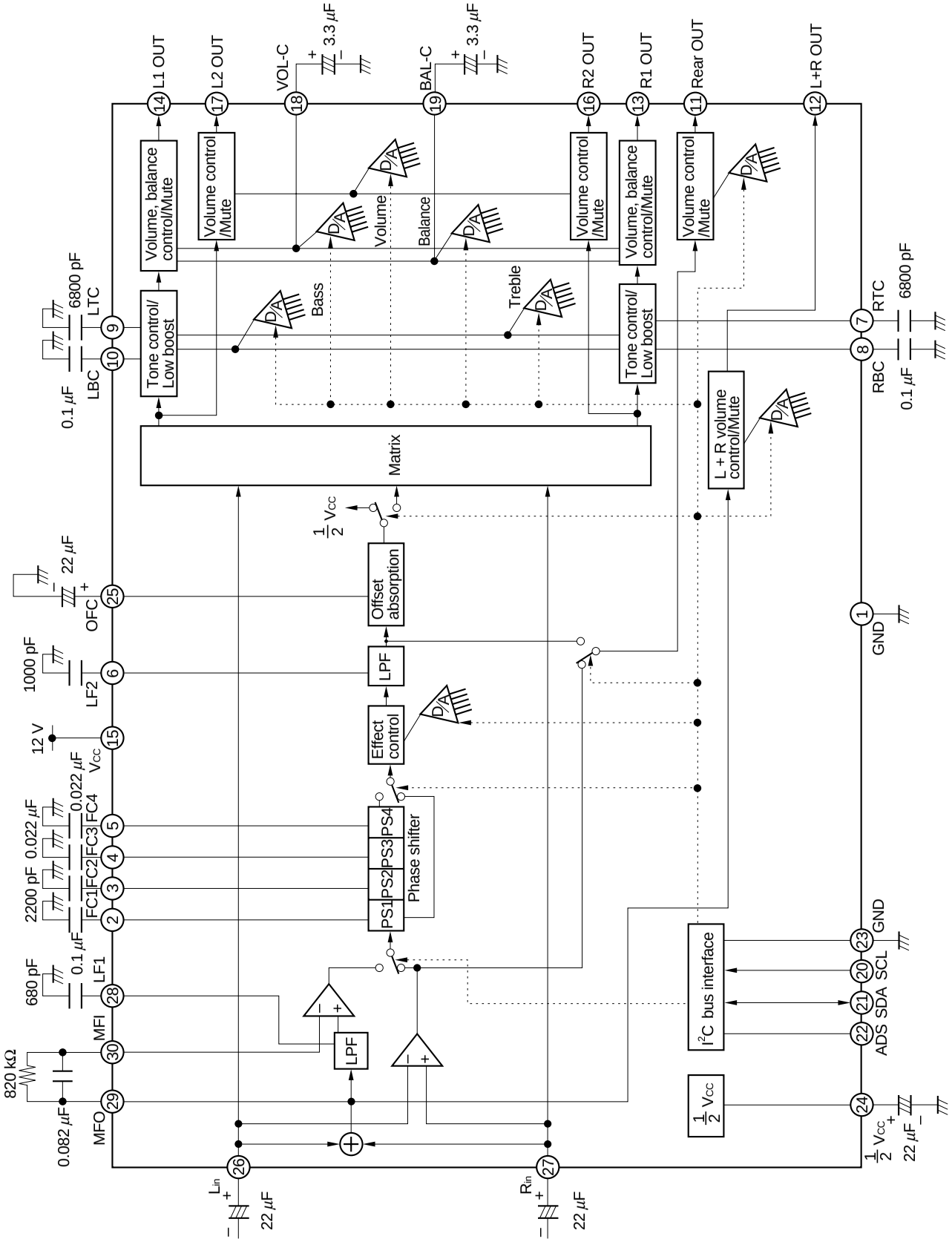
## SYSTEM BLOCK DIAGRAM

- TV

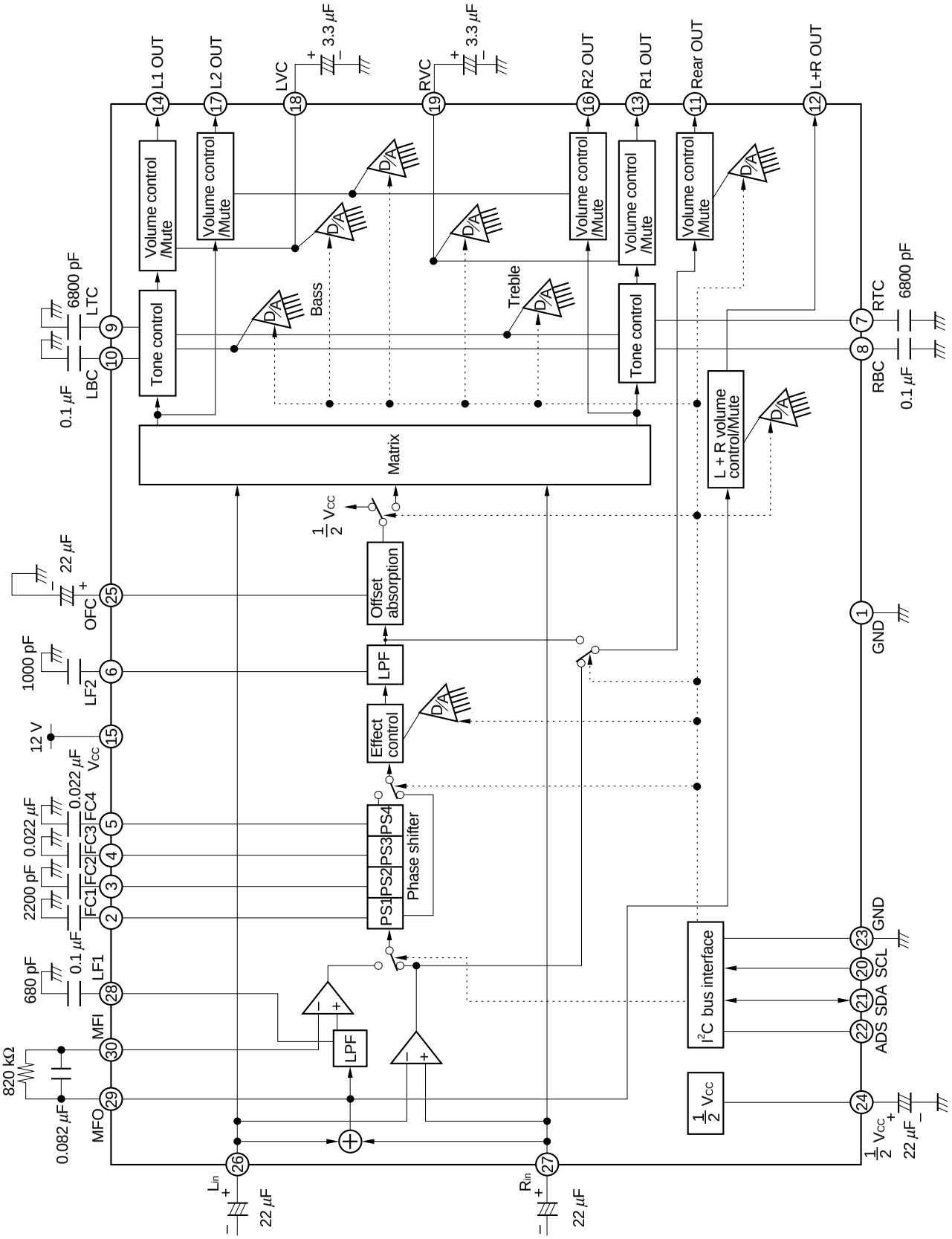


## BLOCK DIAGRAM

### (1) μPC1853-01

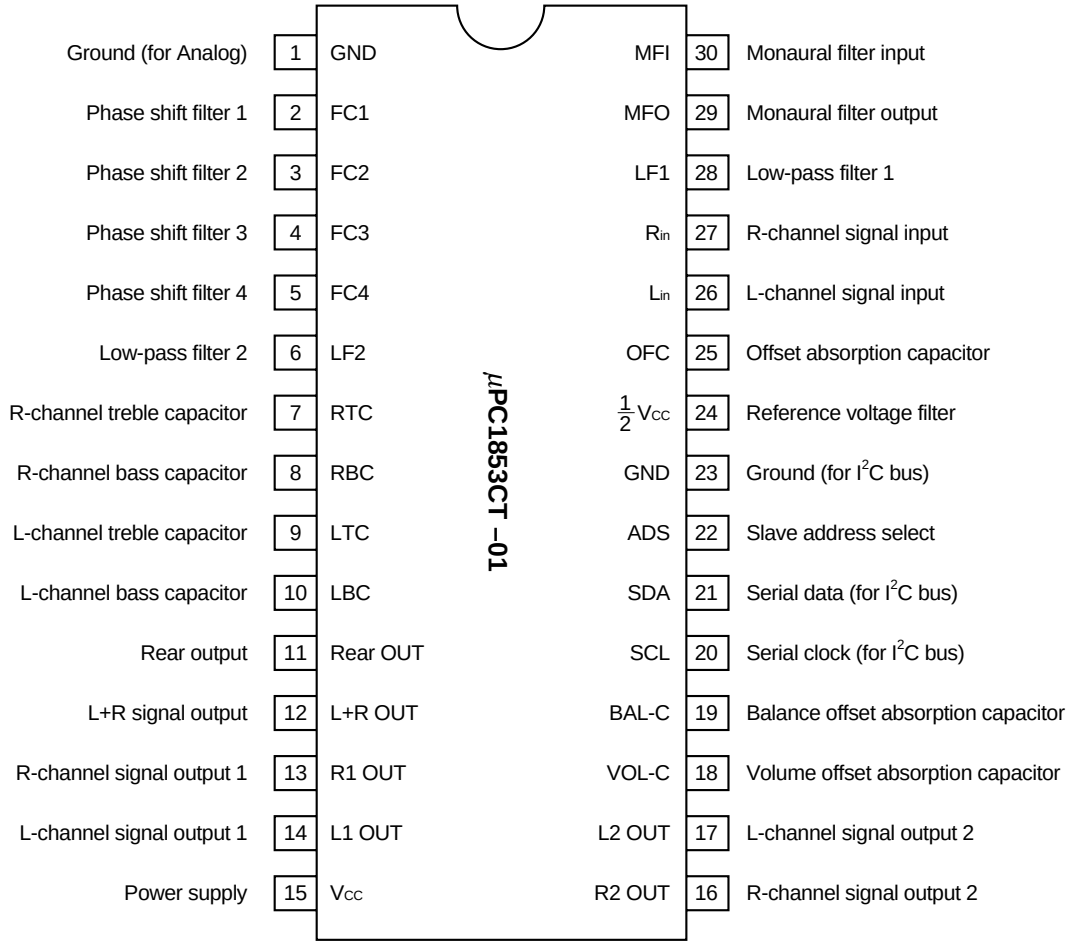


**(2) μPC1853-02**

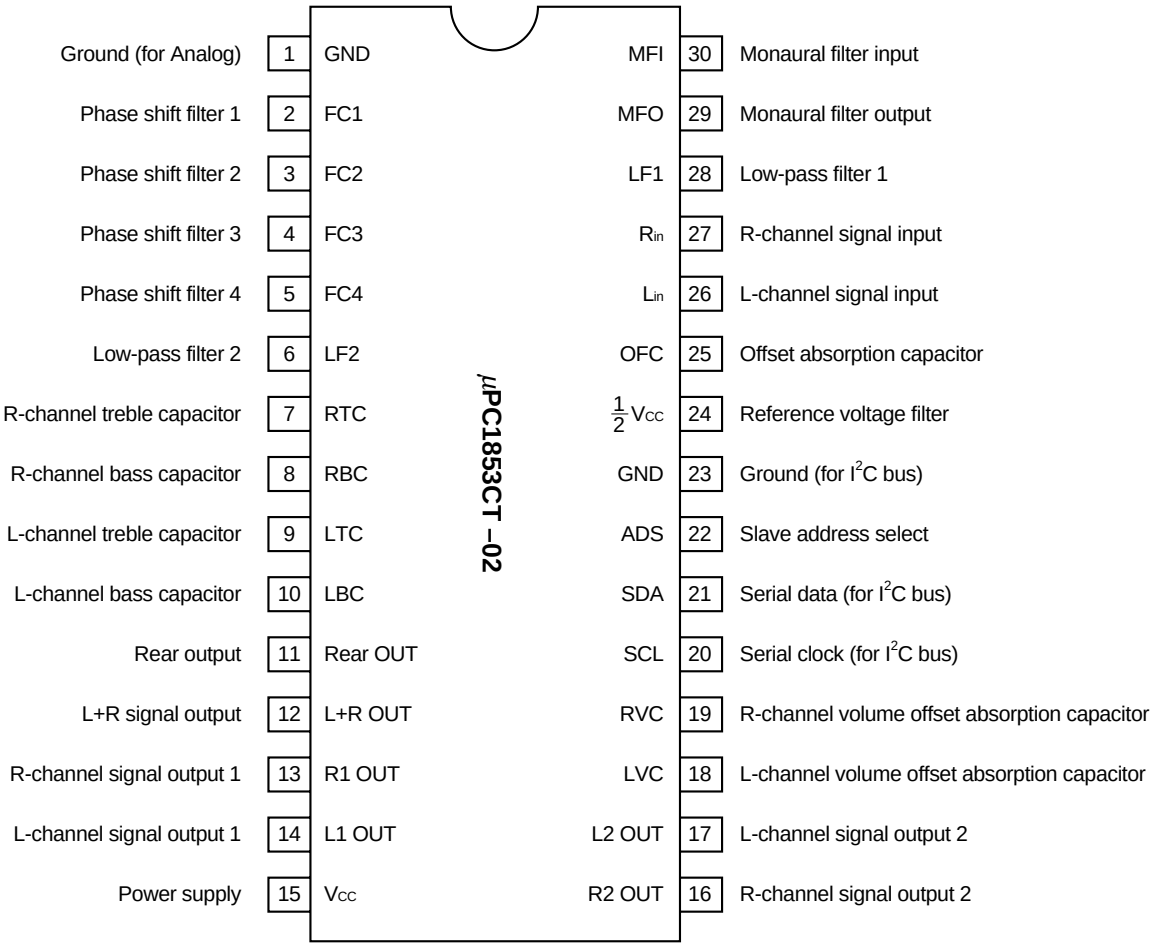

L1 OUT
L2 OUT
LVC
RVC
R2 OUT
R1 OUT
Rear OUT
L+R OUT
3.3 μF
Volume control /Mute
D/A
Bass
Treble
Tone control
Matrix
L + R volume control/Mute
Offset absorption
LPF
Effect control
Phase shifter
PS1
PS2
PS3
PS4
i²C bus interface
6800 pF
LTC
LBC
0.1 μF
RTC
RBC
22 μF
OFC
1000 pF
LF2
12 V
VCC
0.022 μF
FC4
FC3
FC2
FC1
2200 pF
680 pF
LF1
MFI
820 kΩ
0.082 μF
MFO
GND
ADS
SDA
SCL
Lin
Rin

## PIN CONFIGURATION (Top View)

### (1) μPC1853-01



**(2) μPC1853-02**


μPC1853CT–02
Ground (for Analog) 1 GND
Phase shift filter 1 2 FC1
Phase shift filter 2 3 FC2
Phase shift filter 3 4 FC3
Phase shift filter 4 5 FC4
Low-pass filter 2 6 LF2
R-channel treble capacitor 7 RTC
R-channel bass capacitor 8 RBC
L-channel treble capacitor 9 LTC
L-channel bass capacitor 10 LBC
Rear output 11 Rear OUT
L+R signal output 12 L+R OUT
R-channel signal output 1 13 R1 OUT
L-channel signal output 1 14 L1 OUT
Power supply 15 VCC
MFI 30 Monaural filter input
MFO 29 Monaural filter output
LF1 28 Low-pass filter 1
Rin 27 R-channel signal input
Lin 26 L-channel signal input
OFC 25 Offset absorption capacitor
1/2 VCC 24 Reference voltage filter
GND 23 Ground (for I2C bus)
ADS 22 Slave address select
SDA 21 Serial data (for I2C bus)
SCL 20 Serial clock (for I2C bus)
RVC 19 R-channel volume offset absorption capacitor
LVC 18 L-channel volume offset absorption capacitor
L2 OUT 17 L-channel signal output 2
R2 OUT 16 R-channel signal output 2

CONTENTS

## 1. EXPLANATION OF PINS

**Table 1-1 Explanation of Pins (1/8)**

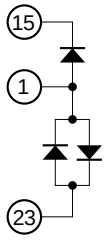
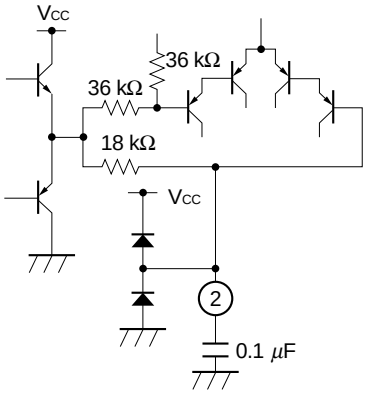
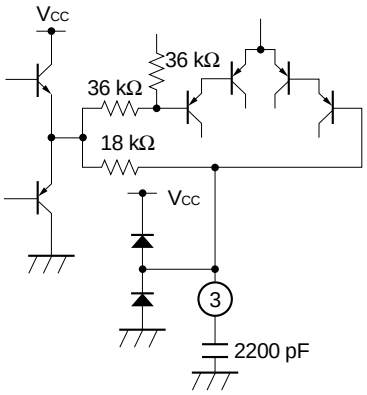
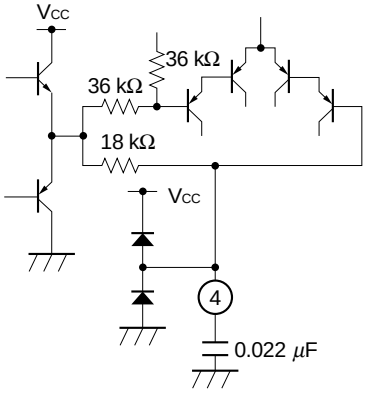
| Pin Number | Pin Name | Equivalent Circuit | Description |
|---|---|---|---|
| 1 | GND |  | Ground for analog signal.<br>Pin voltage: approx. 0.0 V |
| 2 | FC1 |  | Capacitor connection pin which determines time constant of phase shifter.<br>Pin voltage: approx. 6.0 V |
| 3 | FC2 |  | |
| 4 | FC3 |  | |

**Table 1-1 Explanation of Pins (2/8)**

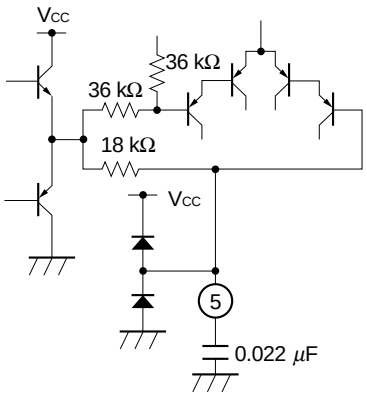
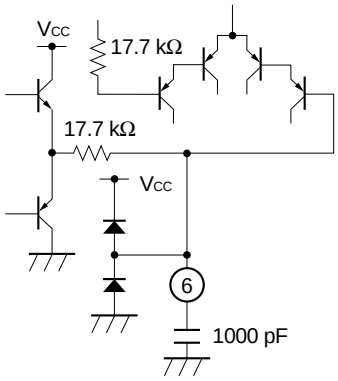
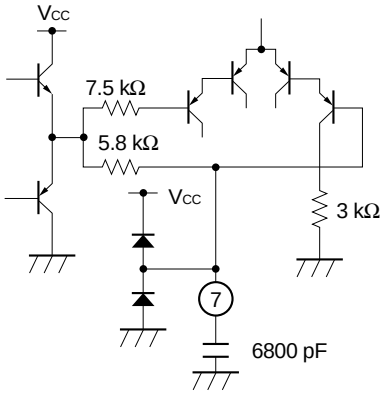
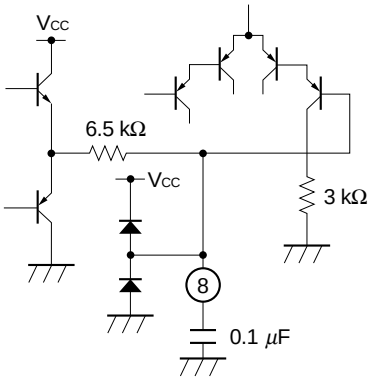
| Pin Number | Pin Name | Equivalent Circuit | Description |
|---|---|---|---|
| 5 | FC4 |  | Capacitor connection pin which determines time constant of phase shifter.<br>Pin voltage: approx. 6.0 V |
| 6 | LF2 |  | Low-pass filter.<br>Pin voltage: approx. 6.0 V |
| 7 | RTC |  | Capacitor connection pin for treble boost/cut frequency characteristic of R-channel signal.<br>Pin voltage: approx. 6.0 V |
| 8 | RBC |  | Capacitor connection pin for bass boost/cut frequency characteristic of R-channel signal.<br>Pin voltage: approx. 6.0 V |

**Table 1-1 Explanation of Pins (3/8)**

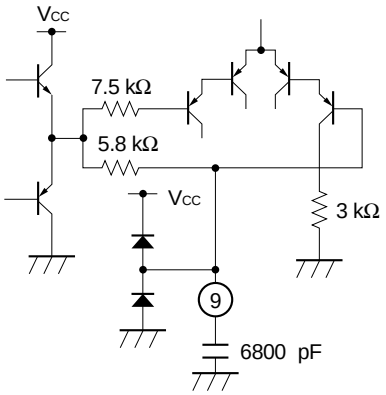
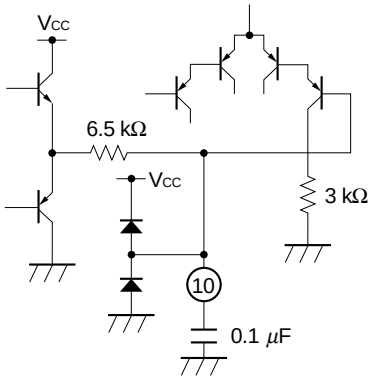
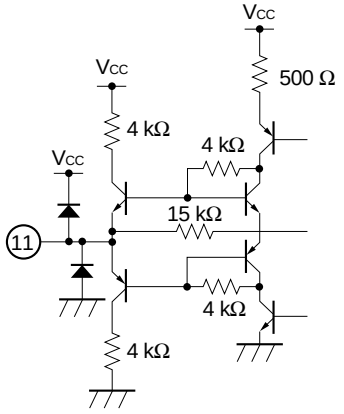
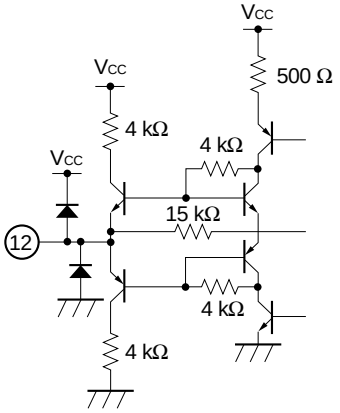
| Pin Number | Pin Name | Equivalent Circuit | Description |
|---|---|---|---|
| 9 | LTC |  | Capacitor connection pin for treble boost/cut frequency characteristic of L-channel signal.<br>Pin voltage: approx. 6.0 V |
| 10 | LBC |  | Capacitor connection pin for bass boost/cut frequency characteristic of L-channel signal.<br>Pin voltage: approx. 6.0 V |
| 11 | Rear OUT |  | L-R signal output pin. Select the output signal (φ(L-R) signal or (L-R) signal) (see **4.4.1(4)** or **4.4.2(2) Rear output selection**).<br>• φ(L-R): Phase-shifted.<br>• (L-R) : Not phase-shifted.<br>Pin voltage: approx. 6.0 V |
| 12 | L+R OUT |  | L+R signal output pin.<br>Pin voltage: approx. 6.0 V |

**Table 1-1 Explanation of Pins (4/8)**

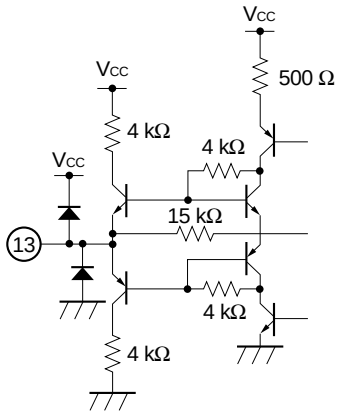
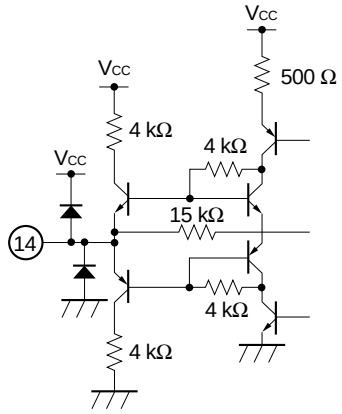
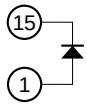
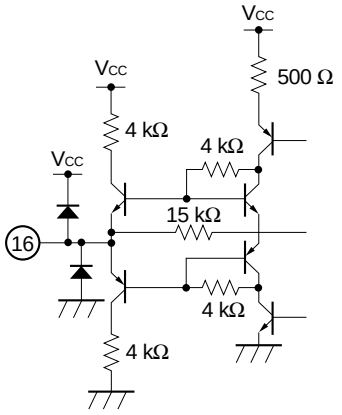
| Pin Number | Pin Name | Equivalent Circuit | Description |
|---|---|---|---|
| 13 | R1 OUT |  | R-channel signal output pin (for main output).<br>Pin voltage: approx. 6.0 V |
| 14 | L1 OUT |  | L-channel signal output pin (for main output).<br>Pin voltage: approx. 6.0 V |
| 15 | Vcc |  | Supply voltage.<br>Pin voltage: approx. 12.0 V |
| 16 | R2 OUT |  | R-channel signal output pin for external audio processor and so on.<br>Pin voltage: approx. 6.0 V |

**Table 1-1 Explanation of Pins (5/8)**

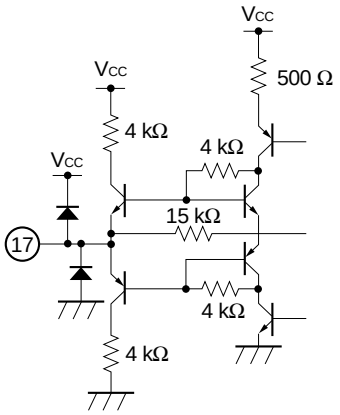
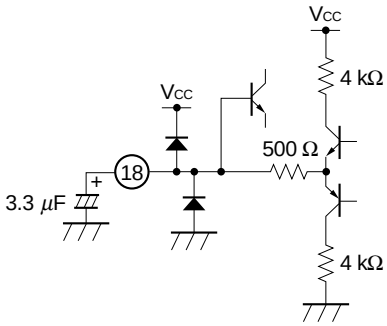
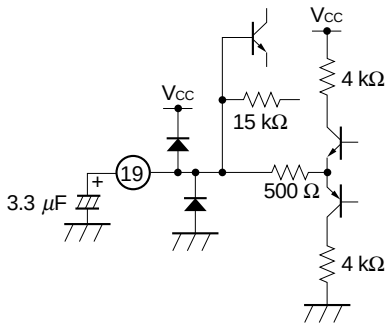
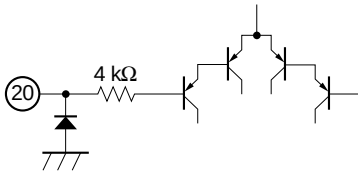
| Pin Number | Pin Name | Equivalent Circuit | Description |
|---|---|---|---|
| 17 | L2 OUT |  | L-channel signal output pin for external audio processor and so on.<br>Pin voltage: approx. 6.0 V |
| 18 | VOL-C (μPC1853-01) |  | Capacitor connection pin which absorbs shock noise of D/A converter for volume control.<br>Pin voltage: approx. 6.0 V |
| | LVC (μPC1853-02) | | Capacitor connection pin which absorbs shock noise of D/A converter for L-channel volume control.<br>Pin voltage: approx. 6.0 V |
| 19 | BAL-C (μPC1853-01) |  | Capacitor connection pin which absorbs shock noise of D/A converter for balance control.<br>Pin voltage: approx. 4.8 V |
| | RVC (μPC1853-02) | | Capacitor connection pin which absorbs shock noise of D/A converter for R-channel volume control.<br>Pin voltage: approx. 4.8 V |
| 20 | SCL |  | Serial clock line pin (clock input for $I^2C$ bus).<br>Pin voltage: approx. 0.0 V |

**Table 1-1 Explanation of Pins (6/8)**

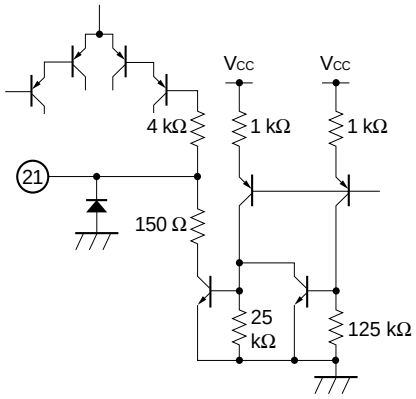
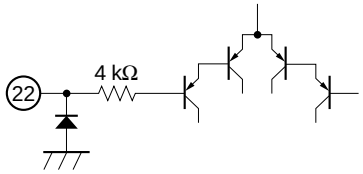
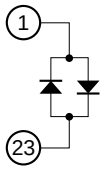
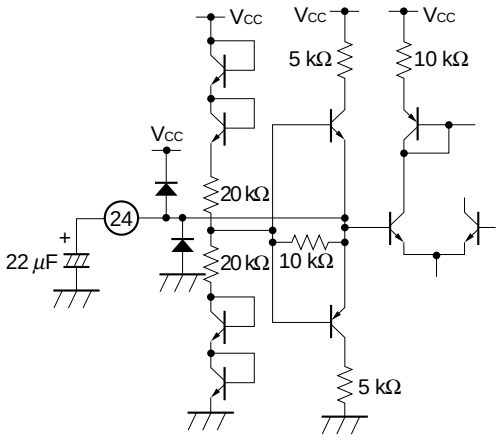
| Pin Number | Pin Name | Equivalent Circuit | Description |
|---|---|---|---|
| 21 | SDA |  | Serial data line pin (data input for I²C bus).<br>Pin voltage: approx. 0.0 V |
| 22 | ADS |  | Slave address selection pin.<br>Pin voltage: approx. 0.0 V |
| 23 | DGND |  | Ground for I²C bus signal.<br>Pin voltage: approx. 0.0 V |
| 24 | $\frac{1}{2}$ Vcc |  | Filter pin for middle point of supply voltage.<br>Pin voltage: approx. 6.0 V |

**Table 1-1 Explanation of Pins (7/8)**

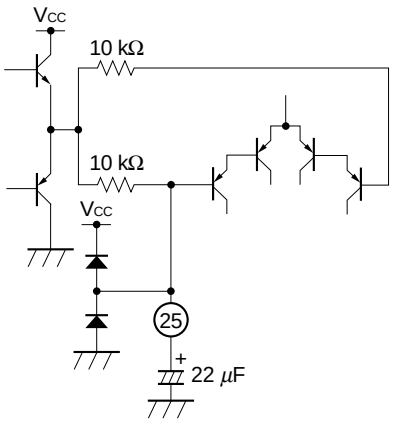
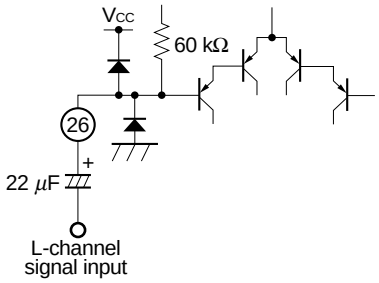
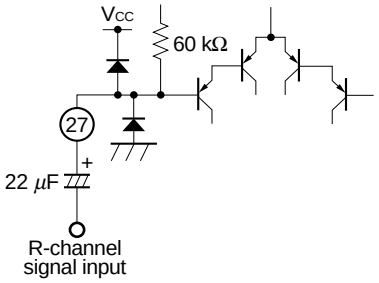
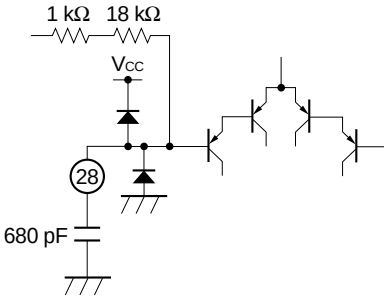
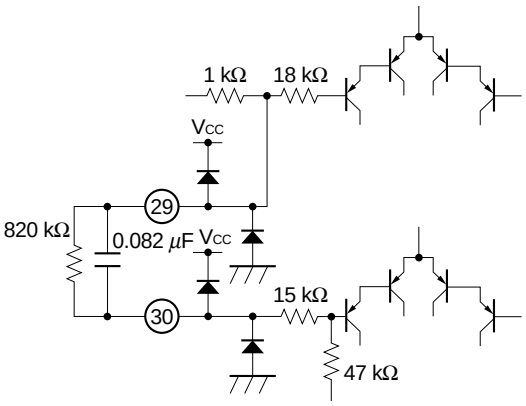
| Pin Number | Pin Name | Equivalent Circuit | Description |
|---|---|---|---|
| 25 | OFC |  | Capacitor connection pin which absorbs offset voltage generated by phase shifter.<br>Pin voltage: approx. 6.0 V |
| 26 | Lin |  | L-channel signal input pin.<br>Input impedance: 60 kΩ<br>Pin voltage: approx. 6.0 V |
| 27 | Rin |  | R-channel signal input pin.<br>Input impedance: 60 kΩ<br>Pin voltage: approx. 6.0 V |
| 28 | LF1 |  | Low-pass filter.<br>Pin voltage: approx. 6.0 V |

**Table 1-1 Explanation of Pins (8/8)**

| Pin Number | Pin Name | Equivalent Circuit | Description |
|---|---|---|---|
| 29 | MFO |  | High-pass filter output pin for surround function (Simulated mode) (see **4.3 Surround Function**). Pin voltage: approx. 6.0 V |
| 30 | MFI | | High-pass filter input pin for surround function (Simulated mode) (see **4.3 Surround Function**). Pin voltage: approx. 6.0 V |

## 2. ATTENTIONS

**<1> Attention on Pop Noise Reduction**

When changing the surround mode and switching power, use the mute function (approx. 200 ms) for pop noise reduction (see **4.4.1(2) Mute** for the μPC1853-01 or **4.4.2(1) Mute** for the μPC1853-02).

**<2> Attention on Supply Voltage**

Drive data on the $I^2C$ bus after supply voltage of total application system becomes stable.

## 3. I²C BUS INTERFACE

The μPC1853 has serial bus function. This serial bus (I²C bus) is a double wired bus developed by Philips. It is composed of 2 wires: serial clock line (SCL) and serial data line (SDA).

The μPC1853 has built-in I²C bus interface circuit, 9 rewritable registers (8 bits).

**SCL (Serial Clock Line)**

The master CPU outputs serial clock to synchronize with the data. According to this clock, the μPC1853 takes in the serial data.

Input level is compatible with CMOS.

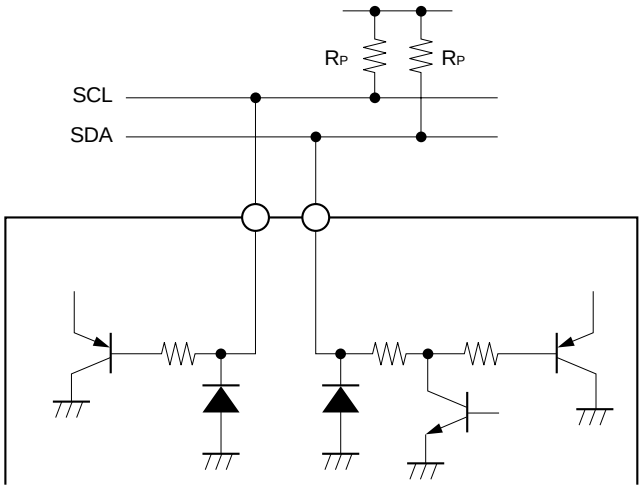
Clock frequency is 0 to 100 kHz.

**SDA (Serial Data Line)**

The master CPU outputs the data which is synchronized with serial clock. The μPC1853 takes in this data according to the clock.

Input level is compatible with CMOS.

**Fig. 3-1 Internal Equivalent Circuits of Interface Pin**




μPC1853

### 3.1 Data Transfer

#### 3.1.1 Start condition

Start condition is made by falling of SDA from “High” to “Low” during SCL is “High” as shown in **Fig. 3-2**.

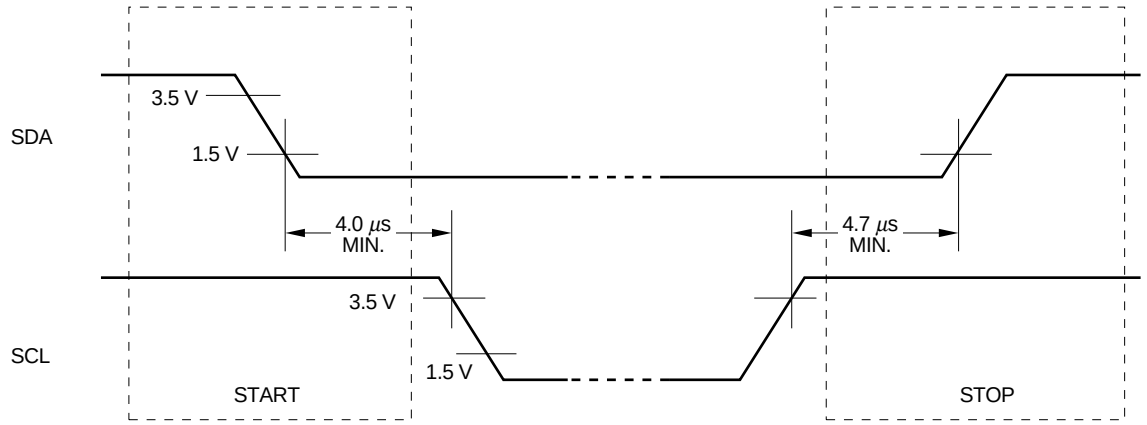
When this start condition is received, the μPC1853 takes in the data synchronizing with the clock after that.

### 3.1.2 Stop condition

Stop condition is made by rising of SDA from “Low” to “High” during SCL is “High” as shown in **Fig. 3-2**.

When this stop condition is received, the μPC1853 stops to take in or output the data.

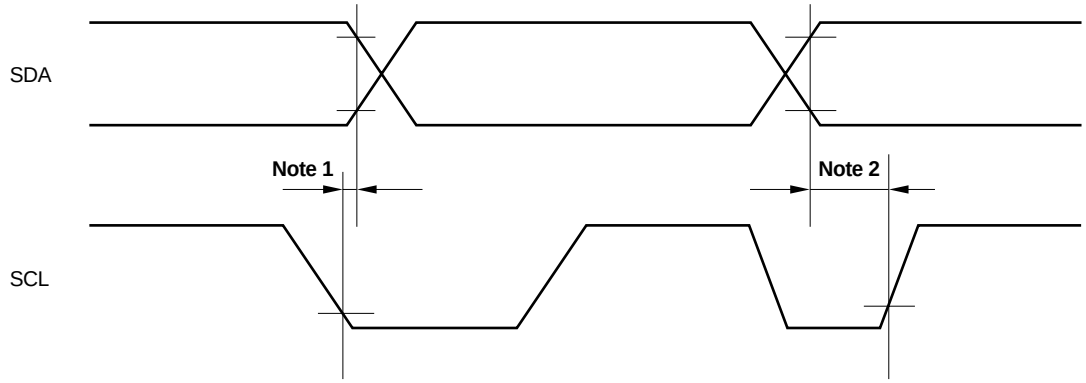
**Fig. 3-2 Start/Stop Condition of Data Transfer**




### 3.1.3 Data transfer

In the case of data transfer, data changing should be executed while SCL is “Low” like Fig. **3-3**. When SCL is “High”, be sure not to change the data.

**Fig. 3-3 Data Transfer**




**Note 1.** Data hold time for $I^2C$ device: 300 ns MIN., Data hold time for CPU: 5 μs MIN.

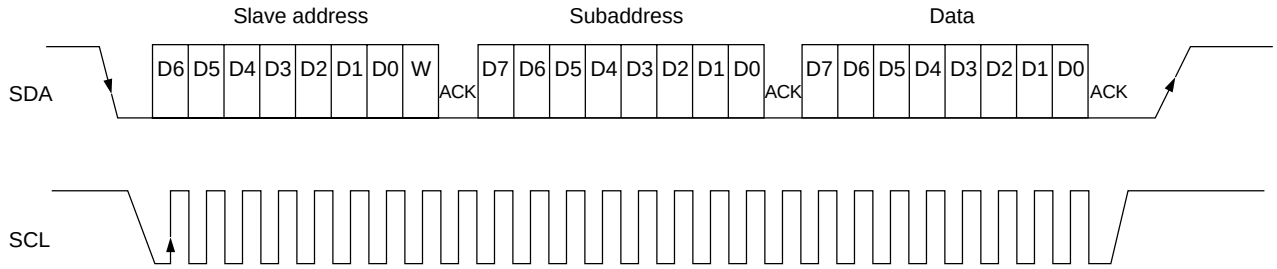
**2.** Data set-up time: 250 ns MIN.

**Remark** Clock frequency: 0 to 100 kHz

### 3.2 Data Transfer Format

**Fig. 3-4** is an example of data transfer in write mode.

**Fig. 3-4 Example of Data Transfer in Write Mode**




**Remark** W: Write mode, ACK: Acknowledge bit

Data is composed of 8 bits. Acknowledge bit is always added after this 8 bits data. Data should be transferred from MSB first.

The 1 byte immediately after start condition specifies the slave address (chip address). This slave address is composed of 7 bits.

**Table 3-1** is the slave address of the μPC1853. This slave address is registered by Phillips.

**Table 3-1 Slave Address of μPC1853**

| Bias Voltage of ADS (Pin 22) | Slave address | | | | | | |
|---|---|---|---|---|---|---|---|
| | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 5V | 1 | 0 | 0 | 0 | 1 | 1 | 0 |
| GND | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

User can set bit D1 freely.

0: Bias voltage of ADS (pin 22) is GND.

1: Bias voltage of ADS (pin 22) is 5 V.

The remaining 1 bit is the read/write bit which specifies the direction of the data transferred after that. Set “0” because the μPC1853 has write mode only.

The byte following the slave address is subaddress byte of the μPC1853.

The μPC1853 has 9 subaddresses from $SA_0$ to $SA_8$, and each of them is composed of 8 bits. The data to be set to the subaddress follows this subaddress byte.

The μPC1853 has automatic increment function. This function increments subaddress automatically in write mode.

By using automatic increment function, once slave address and subaddress are set, data can be transferred continuously to the next subaddress. Use this function for initializing and so on. In the case of changing the data continuously of one subaddress (adjustment and so on), set the automatic increment function OFF (see **4.4.1(8) Automatic increment function**).

### 3.2.1 1 byte data transfer

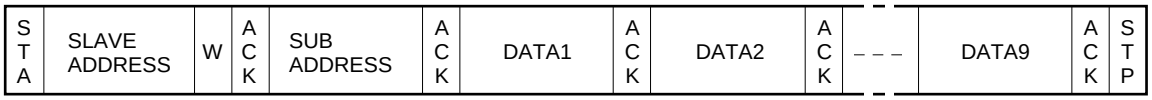
The following is the format in the case of transferring 1 byte data.

| STA | SLAVE ADDRESS | W | ACK | SUB ADDRESS | ACK | DATA | ACK | STP |
|---|---|---|---|---|---|---|---|---|

**Remark** STA: Start, W: Write mode, ACK: Acknowledge bit, STP: Stop

### 3.2.2 Serial data transfer

The following is the format in the case of transferring 8 bytes data at one time by using automatic increment function (the data of subaddress 01H to 08H, bit D6 is “1”).




**Remark** STA: Start, W: Write mode, ACK: Acknowledge, STP: Stop

The master CPU transfers “00H” as subaddress $SA_0$ after start and slave address like above figure. It transfers the data of $SA_0$ after subaddress, and then transfers the data of $SA_1$, $SA_2$..., $SA_8$ continuously without transferring stop condition. Finally, it transfers stop condition and terminates.

The increments of the subaddress of the μPC1853 stops automatically when the subaddress comes to “08H” inside of it.

### 3.2.3 Acknowledge

On $I^2C$ bus, acknowledge bit is added to the 9th bit after the data in order to judge whether data transfer has been succeeded or not. The master CPU judges it from “High” and “Low” of acknowledge condition.

When this acknowledge period is “Low”, it means success. And when the condition is “High”, it means failure of transfer or forced release of bus as NAK state.

The condition of being NAK state is when wrong slave address is transferred to slave IC or data transfer from slave side is finished in read state.

**(1) μPC1853-01**

| Bit / Sub-address | MSB D7 | D6 | D5 | D4 | D3 | D2 | D1 | LSB D0 |
|---|---|---|---|---|---|---|---|---|
| 00H | Rear output selection<br>0: φ(L-R)<br>1: L-R | Low boost<br>0: OFF<br>1: ON | Low boost gain<br>0: 6 dB<br>1: 3 dB | Rear output mute<br>0: OFF<br>1: ON | L+R signal output mute<br>0: OFF<br>1: ON | Audio output mute<br>0: OFF<br>1: ON | Main output mute<br>0: OFF<br>1: ON | Audio output control link<br>0: OFF<br>1: ON |
| 01H | 0 | Automatic increment<br>0: OFF<br>1: ON | Main output volume control<br>Attenuation volume : Flat to Low<br>Data : 111111 to 000000 | | | | | |
| 02H | 0 | Automatic increment<br>0: OFF<br>1: ON | Balance control<br>L-channel attenuation volume : Low to Flat to Flat<br>R-channel attenuation volume : Flat to Flat to Low<br>Data : 111111 to 100000 to 000000 | | | | | |
| 03H | 0 | Automatic increment<br>0: OFF<br>1: ON | Bass control<br>Gain : Boost to 0 dB to Cut<br>Data : 111111 to 100000 to 000000 | | | | | |
| 04H | 0 | Automatic increment<br>0: OFF<br>1: ON | Treble control<br>Gain : Boost to 0 dB to Cut<br>Data : 111111 to 100000 to 000000 | | | | | |
| 05H | 0 | Automatic increment<br>0: OFF<br>1: ON | L+R signal output volume control<br>Attenuation volume : Flat to Low<br>Data : 111111 to 000000 | | | | | |
| 06H | 0 | Automatic increment<br>0: OFF<br>1: ON | Audio output volume control<br>Attenuation volume : Flat to Low<br>Data : 111111 to 000000 | | | | | |
| 07H | 0 | Automatic increment<br>0: OFF<br>1: ON | Rear output volume control<br>Attenuation volume : Flat to Low<br>Data : 111111 to 000000 | | | | | |
| 08H | Surround ON/OFF<br>0: OFF<br>1: ON | Automatic increment<br>0: OFF<br>1: ON | Units of phase shifters<br>0: 4 units<br>1: 1 unit | Monaural/Stereo selection<br>0: Stereo<br>1: Monaural | Effect control<br>Effect : Large to Normal to Small<br>Data : 1111 to 1000 to 0000 | | | |

**Caution Be sure to write data “0” in the subaddress 01H to 07H, bit D7.**

## (2) μPC1853-02

| Bit / Sub-address | MSB D7 | D6 | D5 | D4 | D3 | D2 | D1 | LSB D0 |
|---|---|---|---|---|---|---|---|---|
| 00H | Rear output selection<br>0: φ(L-R)<br>1: L-R | 0 | 0 | Rear output mute<br>0: OFF<br>1: ON | L+R signal output mute<br>0: OFF<br>1: ON | Audio output mute<br>0: OFF<br>1: ON | 0 | 0 |
| 01H | 0 | Automatic increment<br>0: OFF<br>1: ON | R-channel signal output (R1 OUT pin) volume control<br>Attenuation volume : Flat to Low<br>Data : 111111 to 000000 | | | | | |
| 02H | 0 | Automatic increment<br>0: OFF<br>1: ON | L-channel signal output (L1 OUT pin) volume control<br>Attenuation volume : Flat to Low<br>Data : 111111 to 000000 | | | | | |
| 03H | 0 | Automatic increment<br>0: OFF<br>1: ON | Bass control<br>Gain : Boost to 0 dB to Cut<br>Data : 111111 to 100000 to 000000 | | | | | |
| 04H | 0 | Automatic increment<br>0: OFF<br>1: ON | Treble control<br>Gain : Boost to 0 dB to Cut<br>Data : 111111 to 100000 to 000000 | | | | | |
| 05H | 0 | Automatic increment<br>0: OFF<br>1: ON | L+R signal output volume control<br>Attenuation volume : Flat to Low<br>Data : 111111 to 000000 | | | | | |
| 06H | 0 | Automatic increment<br>0: OFF<br>1: ON | Audio output volume control<br>Attenuation volume : Flat to Low<br>Data : 111111 to 000000 | | | | | |
| 07H | 0 | Automatic increment<br>0: OFF<br>1: ON | Rear output volume control<br>Attenuation volume : Flat to Low<br>Data : 111111 to 000000 | | | | | |
| 08H | Surround ON/OFF<br>0: OFF<br>1: ON | Automatic increment<br>0: OFF<br>1: ON | Units of phase shifters<br>0: 4 units<br>1: 1 unit | Monaural/Stereo selection<br>0: Stereo<br>1: Monaural | Effect control<br>Effect : Large to Normal to Small<br>Data : 1111 to 1000 to 0000 | | | |

**Caution Be sure to fix data of the subaddress 00H, bit D6, D5, D1, D0 and subaddress 01H to 07H, bit D7 to "0".**

### 4.2 Initialization

After power-on, be sure to initialize the subaddress data to table below.

**Table 4-1 Initial Data of μPC1853-01**

| Bit / Subaddress | MSB D7 | D6 | D5 | D4 | D3 | D2 | D1 | LSB D0 |
|---|---|---|---|---|---|---|---|---|
| 00H | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 01H | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 02H | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 03H | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 04H | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 05H | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 06H | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 07H | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 08H | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |

**Table 4-2 Initial Data of μPC1853-02**

| Bit / Subaddress | MSB D7 | D6 | D5 | D4 | D3 | D2 | D1 | LSB D0 |
|---|---|---|---|---|---|---|---|---|
| 00H | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 01H | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 02H | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 03H | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 04H | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 05H | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 06H | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 07H | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 08H | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |

**Caution Until initializing completely, mute by the external units.**

### 4.3 Surround Function

About the setting of surround mode, see table below.

**Table 4-3 Setting of Surround Mode**

| Setting / Surround mode | Subaddress: 08H | | | Description | | |
|---|---|---|---|---|---|---|
| | D7 | D5 | D4 | Surround ON/OFF | Units of phase shifter | Monaural/Stereo selection |
| OFF | 0 | – | – | OFF | – | – |
| Movie | 1 | 0 | 0 | ON | 4 units | Stereo |
| Music | 1 | 1 | 0 | | 1 unit | |
| Simulated | 1 | 0 | 1 | | 4 units | Monaural |

–: Don't care.

**Caution When changing the surround mode, use the mute function (approx. 200 ms) for pop noise reduction (see 4.4.1(2) Mute for the μPC1853-01 or 4.4.2(1) Mute for the μPC1853-02).**

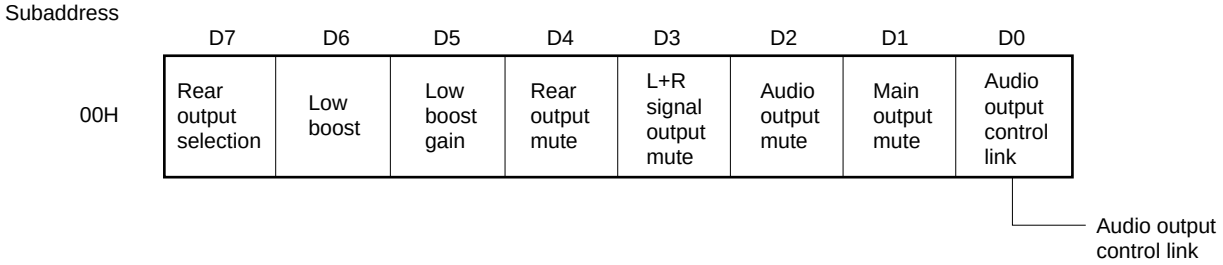
## 4.4 Explanation of Each Command

### 4.4.1 μPC1853-01

**(1) Audio Output Control Link**

By the data of subaddress 00H, bit D0, audio output volume link can be controlled (linked with main output control or not).

**Fig. 4-1 Audio Output Control Link**



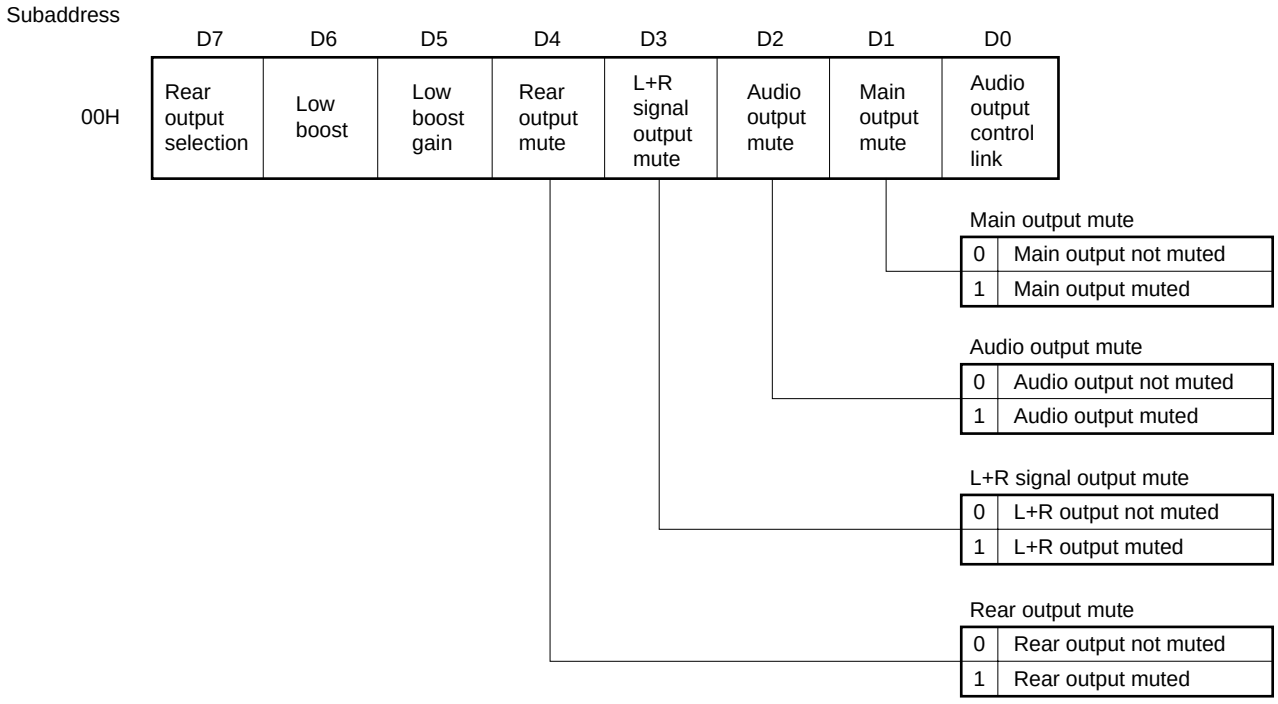

Audio output control link

| | |
|---|---|
| 0 | Audio output volume controlled independently. |
| | Main output volume control (Subaddress: 01H, Bit: D5 to D0)<br>Audio output volume control (Subaddress: 06H, Bit: D5 to D0) |
| 1 | Audio output volume control can be linked with main output volume control. |
| | Main output volume and audio output volume control (Subaddress: 01H, Bit: D5 to D0) |

**(2) Mute**

By the data of subaddress 00H, bit D1 to D4, ON/OFF of mute function can be controlled.

**Fig. 4-2 Mute (μPC1853-01)**

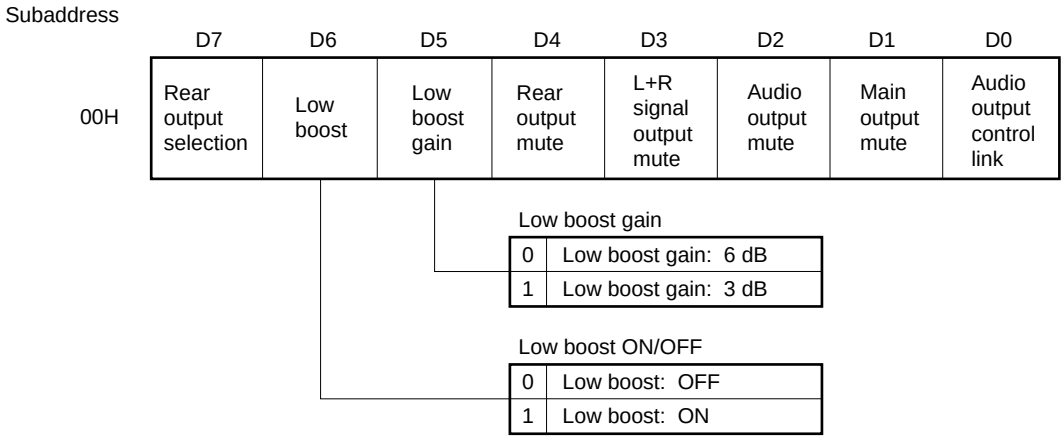



**Caution Use the mute function (approx. 200 ms) for pop noise reduction when changing the surround mode and switching power.**

**(3) Low boost function**

By the data of subaddress 00H, bit D5, the low boost gain can be selected (3 dB or 6 dB). And, by the data of subaddress 00H, bit D6 ON/OFF of the low boost can be controlled.

**Fig. 4-3 Low Boost Function**



### (4) Rear output selection

By the data of subaddress 00H, bit D7, output signal of the rear output pin can be selected (ϕ (L-R) signal or (L-R) signal).

**Fig. 4-4 Rear Output Selection (μPC1853-01)**

| Subaddress | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 00H | Rear output selection | Low boost | Low boost gain | Rear output mute | L+R signal output mute | Audio output mute | Main output mute | Audio output control link |

Rear output selection

| | |
|---|---|
| 0 | ϕ (L-R) signal: Phase-shifted |
| 1 | (L-R) signal: Not phase-shifted |

### (5) Volume control

By the data of subaddress 01H, 05H, 06H and 07H, bit D5 to D0, the volume control can be adjusted in 64 levels.

**Fig. 4-5 Volume Control (μPC1853-01) (1/2)**

- **Main output volume control**

| Subaddress | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 01H | 0 | Automatic increment | Main output volume control | | | | | |

Main output volume control

| Data D5 ⋯ D0 | Attenuation volume |
|---|---|
| 111111 | Flat |
| ⋮ | ⋮ |
| 000000 | Low |

- **L+R signal output volume control**

| Subaddress | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 05H | 0 | Automatic increment | L+R signal output volume control | | | | | |

L+R signal output volume control

| Data D5 ⋯ D0 | Attenuation volume |
|---|---|
| 111111 | Flat |
| ⋮ | ⋮ |
| 000000 | Low |

**Fig. 4-5 Volume Control (μPC1853-01) (2/2)**

- **Audio output volume control[Note]**

Subaddress 06H

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| 0 | Automatic increment | Audio output volume control | | | | | |

Audio output volume control

| Data D5 ⋯ D0 | Attenuation volume |
|---|---|
| 111111 | Flat |
| ⋮ | ⋮ |
| 000000 | Low |

**Note** When selecting the mode linking main output volume control to audio output volume control, the audio output volume can be controlled by the data of main output volume control (see **(1) Audio Output Control Link**). In that case, fix the audio output volume control data to "111111".

- **Rear output volume control**

Subaddress 07H

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| 0 | Automatic increment | Rear output volume control | | | | | |

Rear output volume control

| Data D5 ⋯ D0 | Attenuation volume |
|---|---|
| 111111 | Flat |
| ⋮ | ⋮ |
| 000000 | Low |

### (6) Balance control

By the data of subaddress 02H, bit D5 to D0, the balance level of L1 OUT and R1 OUT pin can be adjusted in 64 levels.

**Fig. 4-6 Balance Control**

Subaddress 02H

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| 0 | Automatic increment | Balance control | | | | | |

Balance control

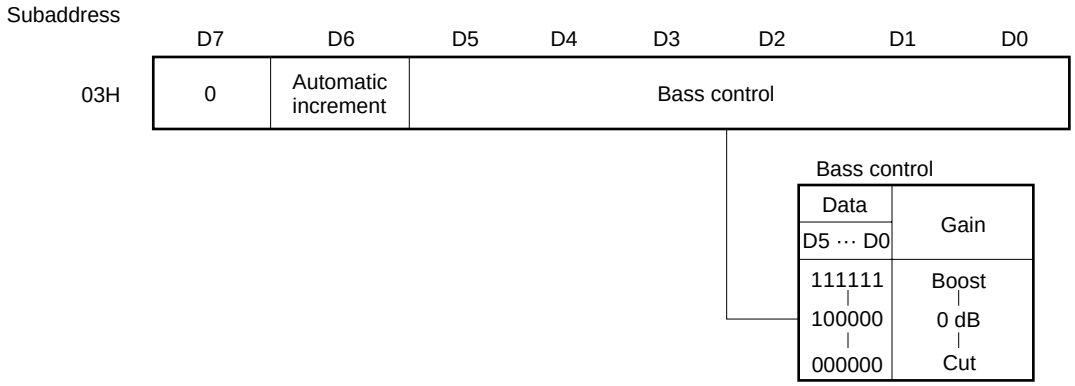
| Data D5 ⋯ D0 | L-channel attenuation volume | R-channel attenuation volume |
|---|---|---|
| 111111 | Low | Flat |
| ⋮ | ⋮ | ⋮ |
| 100000 | Flat | Flat |
| ⋮ | ⋮ | ⋮ |
| 000000 | Flat | Low |

### (7) Bass and treble control

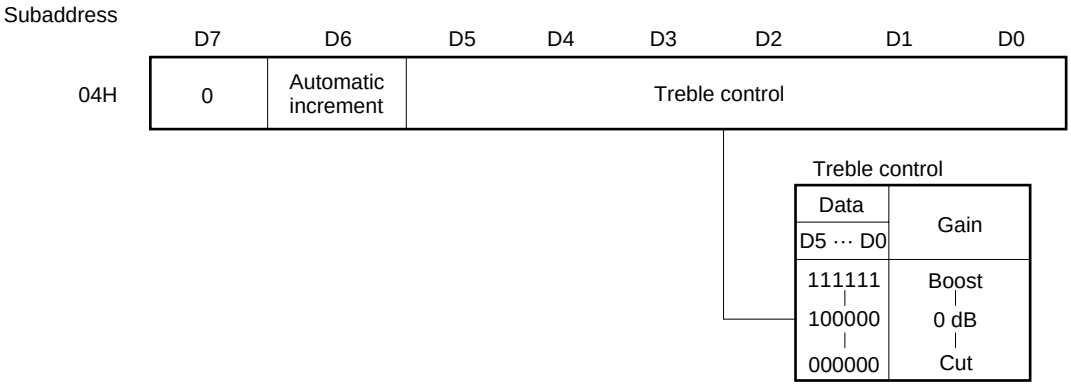
By the data of subaddress 03H and 04H, bit D5 to D0, the bass and treble tone for main output (L1 OUT and R1 OUT pin) can be adjusted in 64 levels.

**Fig. 4-7 Bass and Treble Control**

- **Bass control**



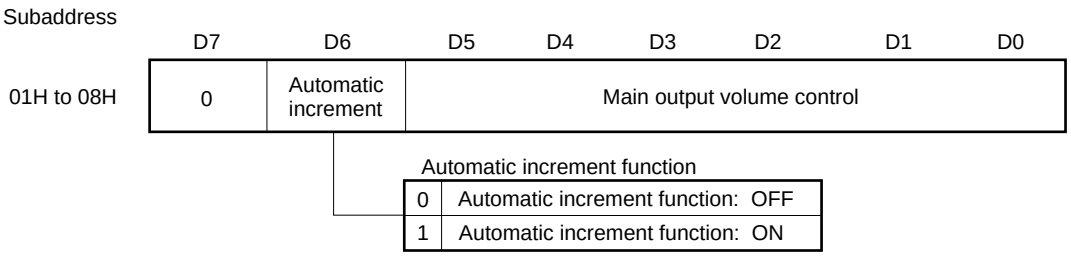

- **Treble control**




### (8) Automatic increment function

By the data of subaddress 01H to 08H, bit D6, ON/OFF of the automatic increment function can be controlled.

**Fig. 4-8 Automatic Increment Function**



**Caution After power-on, be sure to initialize the subaddress data (see 4.2 Initialization).**

The automatic increment function increments subaddress automatically.

Automatic increment function is ON : Subaddress is incremented automatically.
If once slave address and subaddress are set, without setting the next subaddress, data of the next subaddress can be transferred.

Automatic increment function is OFF: Subaddress is fixed.
Data of the fixed subaddress can be set repeatedly.

The automatic increment ON/OFF bit is in the subaddress 01H to 08H. The increment of subaddress is controlled individually by each automatic increment ON/OFF bit. As for 00H, subaddress is not incremented automatically (see **4.1 Subaddress List**).

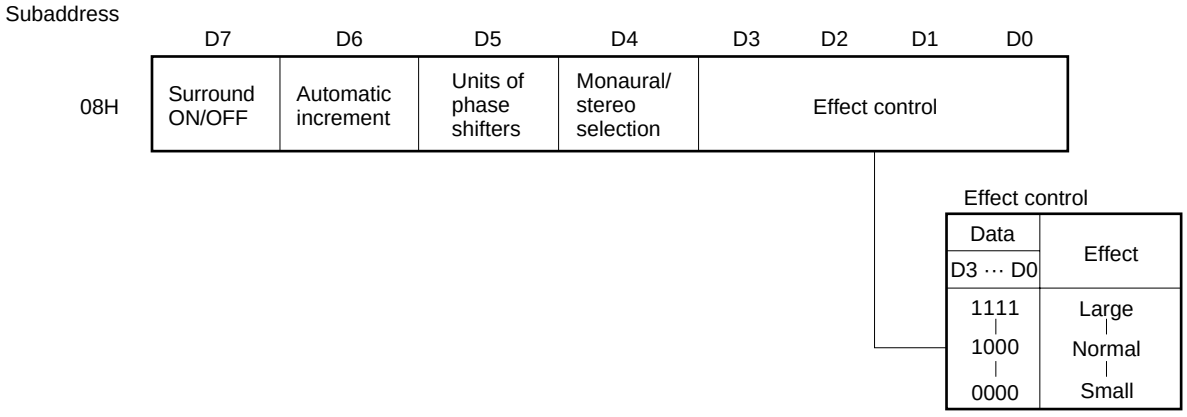
For example, when the automatic increment function of subaddress 01H is ON and that of 02H is OFF, subaddress is incremented from 01H to 02H automatically and is fixed on 02H.

In case of the automatic increment function of 08H is ON, subaddress is not incremented. If next data is transferred after setting data of 08H (acknowledge bit: L), the acknowledge condition is changed into NAK state (acknowledge bit: H). And the data transfer from the master CPU is stopped.

**(9) Effect control**

By the data of subaddress 08H, bit D3 to D0, the level of indirect sound signal (surround signal) added to the original signal can be adjusted in 16 levels.

**Fig. 4-9 Effect Control**



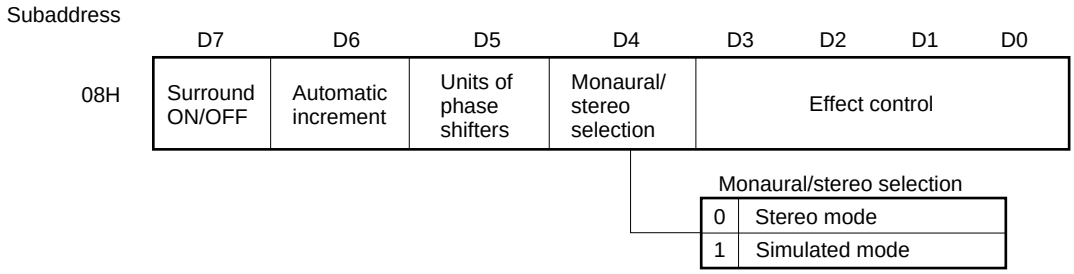

**(10) Monaural/Stereo selection**

By the data of subaddress 08H, bit D4, the surround mode can be selected (stereo mode or simulated mode).

Stereo mode : Surround signal processing for stereo source.
The phase of the difference between L-channel and R-channel signals is shifted and added to the original signal.

Simulated mode : Stereo sound simulation for monaural source.
The phase of the difference between the signal through HPF and the signal through LPF is shifted, and the signals are added to the original signal. When the output frequency characteristics of L-channel and R-channel signals become the form of comb, stereo sound simulation can be realized.

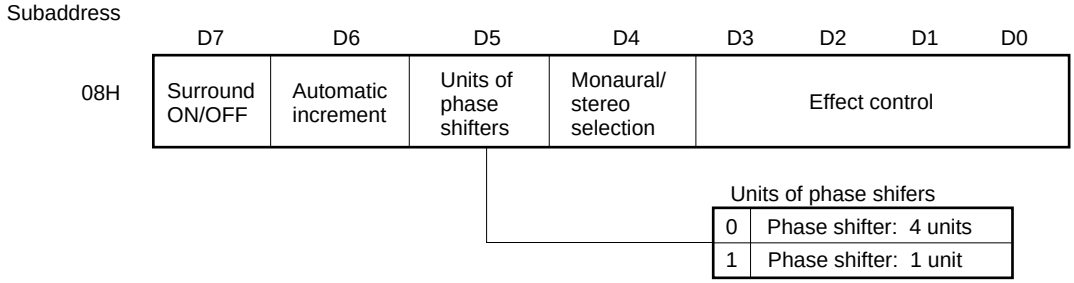
**Fig. 4-10 Monaural/Stereo Selection**




**(11) Units of phase shifters**

By the data of subaddress 08H, bit D5, the number of phase shifter's units (1 or 4 units) can be selected for the indirect sound signal (surround signal).

**Fig. 4-11 Units of Phase Shifters**



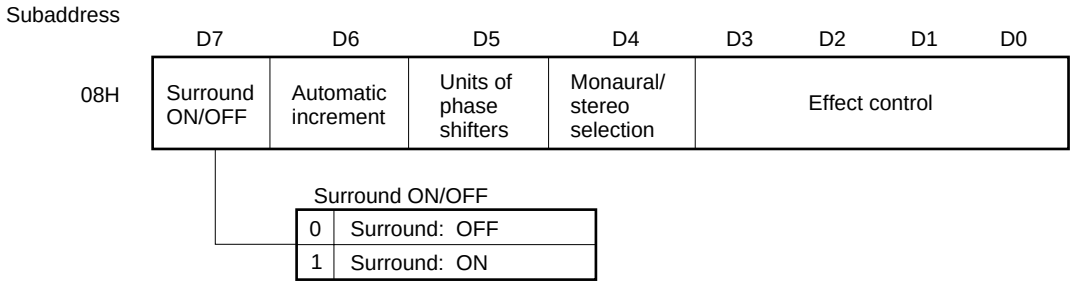

**(12) Surround ON/OFF**

By the data of subaddress 08H, bit D7, ON/OFF of surround (indirect sound signal) mode can be selected.

Surround OFF: Original signal is taken out directly (OFF mode).

Surround ON : The signal passed through the phase shifter (indirect sound) is added to the original signal (Movie, Music and Simulated mode).

**Fig. 4-12 Surround ON/OFF**

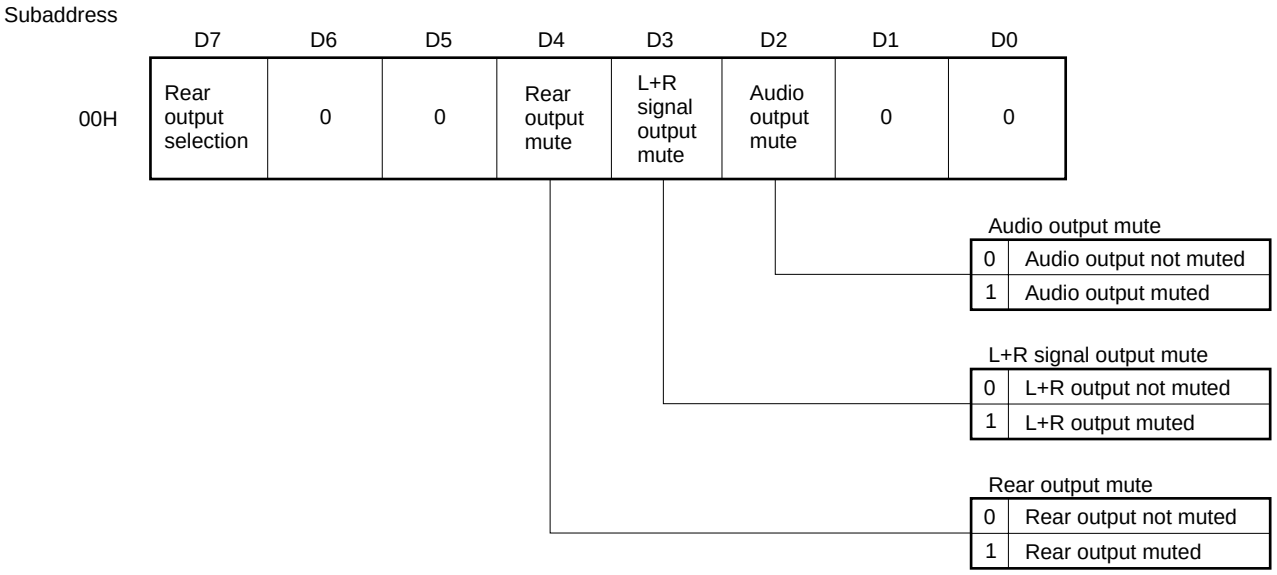


### 4.4.2 μPC1853-02

**(1) Mute**

By the data of subaddress 00H, bit D2 to D4, ON/OFF of mute function can be controlled.

**Fig. 4-13 Mute (μPC1853-02)**

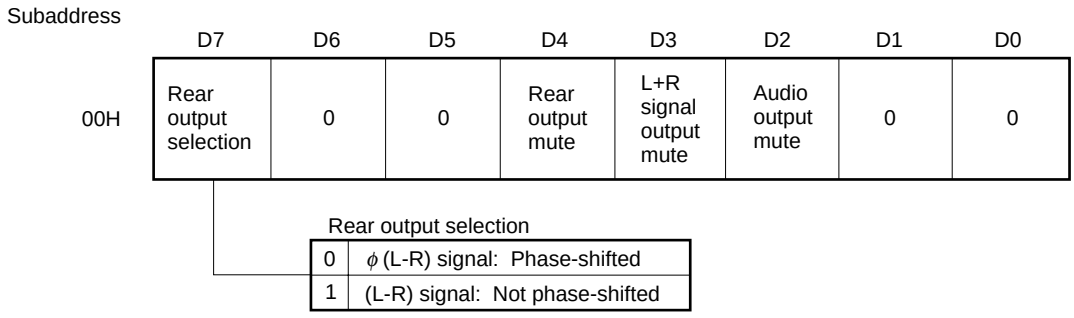



**Caution Use the mute function (approx. 200 ms) for pop noise reduction when changing the surround mode and switching power.**

**(2) Rear output selection**

By the data of subaddress 00H, bit D7, output signal of the rear output pin can be selected (ϕ (L-R) signal or (L-R) signal).

**Fig. 4-14 Rear Output Selection (μPC1853-02)**

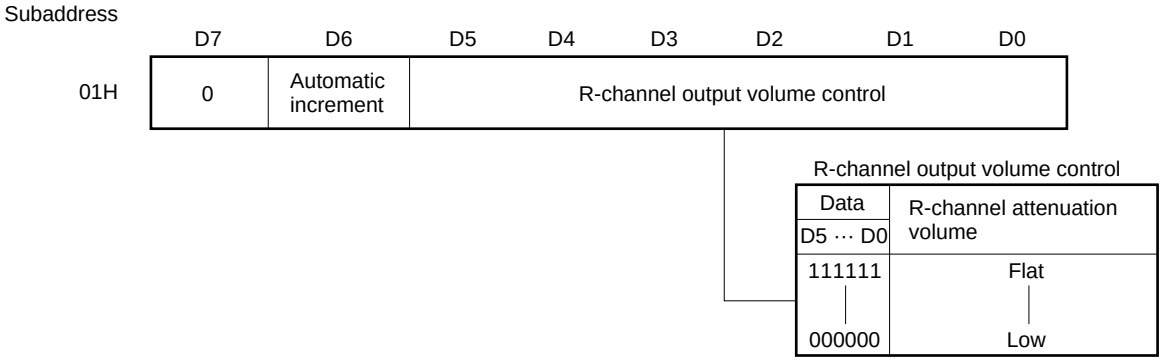


**(3) Volume control**

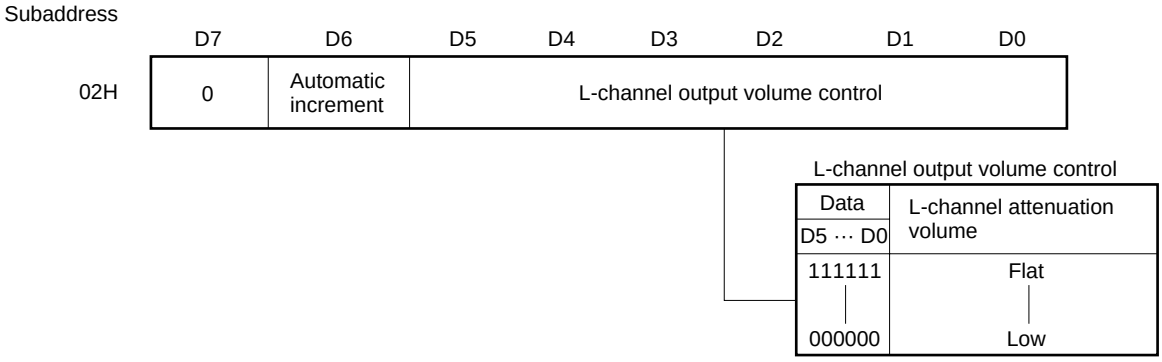
By the data of subaddress 01H, 02H, 05H, 06H and 07H, bit D5 to D0, the volume control can be adjusted in 64 levels.

**Fig. 4-15 Volume Control (μPC1853-02) (1/2)**

- **R-channel output volume control**




- **L-channel output volume control**




- **L+R signal output volume control**

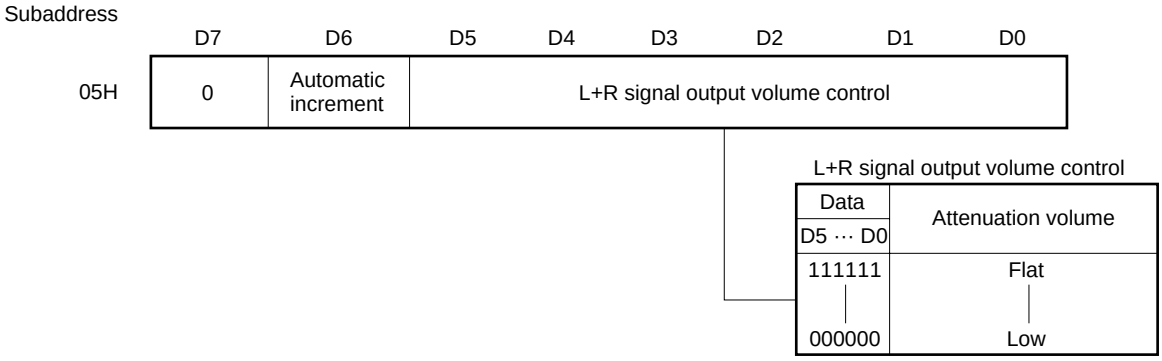


**Fig. 4-15 Volume Control (μPC1853-02) (2/2)**

- **Audio output volume control**

Subaddress

| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 06H | 0 | Automatic increment | Audio output volume control | | | | | |

Audio output volume control

| Data D5 ⋯ D0 | Attenuation volume |
|---|---|
| 111111 | Flat |
| ⋮ | ⋮ |
| 000000 | Low |

- **Rear output volume control**

Subaddress

| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 07H | 0 | Automatic increment | Rear output volume control | | | | | |

Rear output volume control

| Data D5 ⋯ D0 | Attenuation volume |
|---|---|
| 111111 | Flat |
| ⋮ | ⋮ |
| 000000 | Low |

**(4) Bass and treble control**

See **4.4.1 (7) Bass and treble control.**

**(5) Automatic increment function**

See **4.4.1 (8) Automatic increment function.**

**(6) Effect control**

See **4.4.1 (9) Effect control.**

**(7) Monaural/Stereo selection**

See **4.4.1 (10) Monaural/Stereo selection.**

**(8) Units of phase shifters**

See **4.4.1 (11) Units of phase shifters.**

**(9) Surround ON/OFF**

See **4.4.1 (12) Surround ON/OFF.**

## 5. ELECTRICAL CHARACTERISTICS

**Absolute Maximum Ratings** (Unless otherwise specified, $T_A$ = 25 ˚C)

| Parameter | Symbol | Test conditions | Ratings | Unit |
|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | No signal | 14.0 | V |
| Input signal voltage | $V_{IN}$ | | $V_{CC}$ | V |
| $I^2C$ bus input pin voltage | $V_{cont}$ | | $V_{CC}$ + 0.2 | V |
| Power dissipation | $P_D$ | $T_A$ = 75 ˚C | 500 | mW |
| Operating temperature | $T_A$ | $V_{CC}$ = 12 V | –20 to +75 | ˚C |
| Storage temperature | $T_{stg}$ | | –40 to +125 | ˚C |

**Recommended Operating Conditions** (Unless otherwise specified, $T_A$ = 25 ˚C)

| Parameter | Symbol | Test conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | | 10.8 | 12.0 | 13.2 | V |
| Input signal voltage | $V_{IN}$ | $V_{CC}$ = 12 V,<br>Gain of input-output: 0 dB | 0.0 | 1.4 | 7.9 | $V_{p-p}$ |
| $I^2C$ bus input pin voltage (H) | $V_{contH}$ | Pins SDA and SCL | 3.5 | 5.0 | 6.0 | V |
| $I^2C$ bus input pin voltage (L) | $V_{contL}$ | | 0.0 | 0.0 | 1.5 | V |

## Electrical Characteristics

($V_{CC}$ = 12 V, $T_A$ = 25 ˚C, RH ≤ 70 %, f = 1 kHz, $V_{IN}$ = 0.5 $V_{rms}$, No load impedance, unless otherwise specified)

**General** (1/1)

| Parameter | Symbol | Test conditions | Switch mode[Note] | | | Subaddress data | | | | | | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | S1 | S2 | S3 | 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | | | | |
| Supply current | $I_{CC}$ | No signal | b | b | – | 80 | 7F | 60 | 60 | 60 | 7F | 7F | 7F | 48 | 16 | 24 | 32 | mA |
| Maximum input voltage 1 | $V_{OM1}$ | Lin, Rin ≥ 2.8 $V_{rms}$, THD = 1 %, L1 OUT, R1 OUT, L2 OUT, R2 OUT, L+R OUT | a | a | – | 80 | 7F | 60 | 60 | 60 | 7F | 7F | 7F | 48 | 7.9 | 8.8 | 9.3 | $V_{p-p}$ |
| Maximum input voltage 2 | $V_{OM2}$ | Lin ≥ 2.8 $V_{rms}$, Rin = GND, THD = 1 %, Rear OUT | a | b | – | | | | | | | | | | 2.5 | 2.8 | 3.3 | $V_{p-p}$ |
| Distortion rate (L-ch) | $THD_L$ | f = 1 kHz, Lin = 0.5 $V_{rms}$, Rin = GND, L1 OUT, L2 OUT | a | b | – | 80 | 7F | 60 | 60 | 60 | 7F | 7F | 7F | 48 | – | 0.1 | 0.5 | % |
| Distortion rate (R-ch) | $THD_R$ | f = 1 kHz, Lin = GND, Rin = 0.5 $V_{rms}$, R1 OUT, R2 OUT | b | a | – | | | | | | | | | | – | 0.1 | 0.5 | % |

–: Don't care.

**Note** See **7. MEASURING CIRCUIT**.

**Remark** The values are common to both the μPC1853CT-01 and μPC1853CT-02.

### (1) μPC1853CT-01 Volume control, tone control block (1/3)

| Parameter | Symbol | Test conditions | Switch mode[Note] | | | Subaddress data | | | | | | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | S1 | S2 | S3 | 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | | | | |
| Volume attenuation 1 (1) | $ATT_{VL11}$ | Lin = 0.5 $V_{rms}$, Rin = GND, | a | b | – | 80 | 7F | 60 | 60 | 60 | 7F | 7F | 7F | 48 | –1.5 | 0.0 | +1.5 | dB |
| Volume attenuation 1 (2) | $ATT_{VL12}$ | L1 OUT | | | | | 60 | | | | | | | | –25.0 | –19.0 | –13.0 | dB |
| Volume attenuation 1 (3) | $ATT_{VL13}$ | | | | | | 40 | | | | | | | | –80.0 | – | – | dB |
| Volume attenuation 2 (1) | $ATT_{VL21}$ | Lin = 0.5 $V_{rms}$, Rin = GND, | a | b | – | 80 | 7F | 60 | 60 | 60 | 7F | 7F | 7F | 48 | –1.5 | 0.0 | +1.5 | dB |
| Volume attenuation 2 (2) | $ATT_{VL22}$ | L2 OUT | | | | | | | | | | 60 | | | –25.0 | –19.0 | –13.0 | dB |
| Volume attenuation 2 (3) | $ATT_{VL23}$ | | | | | | | | | | | 40 | | | –80.0 | – | – | dB |
| L+R volume attenuation 1 | $ATT_{VLR1}$ | Lin = 0.5 $V_{rms}$, Rin = 0.5 $V_{rms}$, | a | a | – | 80 | 7F | 60 | 60 | 60 | 7F | 7F | 7F | 48 | –1.5 | 0.0 | +1.5 | dB |
| L+R volume attenuation 2 | $ATT_{VLR2}$ | L+R OUT | | | | | | | | | 60 | | | | –25.0 | –19.0 | –13.0 | dB |
| L+R volume attenuation 3 | $ATT_{VLR3}$ | | | | | | | | | | 40 | | | | –80.0 | – | – | dB |
| Rear volume attenuation 1 | $ATT_{VRE1}$ | Lin = 0.5 $V_{rms}$, Rin = GND, | a | b | – | 80 | 7F | 60 | 60 | 60 | 7F | 7F | 7F | 48 | 8.5 | 10.0 | 11.5 | dB |
| Rear volume attenuation 2 | $ATT_{VRE2}$ | Rear OUT | | | | | | | | | | | 60 | | –15.0 | –9.0 | –3.0 | dB |
| Balance attenuation (L-ch) 1 (1) | $ATT_{BL11}$ | Lin = 0.5 $V_{rms}$, Rin = GND, | a | b | – | 80 | 7F | 41 | 60 | 60 | 7F | 7F | 7F | 48 | –1.5 | 0.0 | +1.5 | dB |
| Balance attenuation (L-ch) 1 (2) | $ATT_{BL12}$ | L1 OUT | | | | | | 60 | | | | | | | –1.5 | 0.0 | +1.5 | dB |
| Balance attenuation (L-ch) 1 (3) | $ATT_{BL13}$ | | | | | | | 7F | | | | | | | –80.0 | – | – | dB |
| Balance attenuation (R-ch) 1 (1) | $ATT_{BR11}$ | Lin = GND, Rin = 0.5 $V_{rms}$, | b | a | – | 80 | 7F | 41 | 60 | 60 | 7F | 7F | 7F | 48 | –80.0 | – | – | dB |
| Balance attenuation (R-ch) 1 (2) | $ATT_{BR12}$ | R1 OUT | | | | | | 60 | | | | | | | –1.5 | 0.0 | +1.5 | dB |
| Balance attenuation (R-ch) 1 (3) | $ATT_{BR13}$ | | | | | | | 7F | | | | | | | –1.5 | 0.0 | +1.5 | dB |
| Low-band boost control | $V_{BB}$ | f = 100 Hz, Lin = 0.5 $V_{rms}$, | a | b | – | 80 | 7F | 60 | 7F | 60 | 7F | 7F | 7F | 48 | 7.0 | 10.0 | 13.0 | dB |
| Low-band flat control | $V_{BF}$ | Rin = GND, L1 OUT | | | | | | | 60 | | | | | | –3.0 | 0.0 | +3.0 | dB |
| Low-band cut control | $V_{BC}$ | | | | | | | | 41 | | | | | | –13.0 | –10.0 | –7.0 | dB |
| Low-band boost control (6 dB) 1 | $V_{B6dB1}$ | f = 100 Hz, Lin = 0.5 $V_{rms}$, | a | b | – | 80 | 7F | 60 | 60 | 60 | 7F | 7F | 7F | 48 | 2.0 | 3.0 | 4.0 | dB |
| Low-band boost control (6 dB) 2 | $V_{B6dB2}$ | Rin = GND, L1 OUT | | | | ↓ | 60 | | | | | | | | 3.0 | 4.0 | 5.0 | dB |
| Low-band boost control (6 dB) 3 | $V_{B6dB3}$ | | | | | C0 | 50 | | | | | | | | 4.0 | 6.0 | 8.0 | dB |

–: Don't care.

**Note** See **7. MEASURING CIRCUIT**.

## (1) μPC1853CT-01 Volume control, tone control block (2/3)

| Parameter | Symbol | Test conditions | Switch mode[Note] | | | Subaddress data | | | | | | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | S1 | S2 | S3 | 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | | | | |
| Low-band boost control (3 dB) 1 | $V_{B3dB1}$ | f = 100 Hz, Lin = 0.5 $V_{rms}$, | a | b | – | A0 | 7F | 60 | 60 | 60 | 7F | 7F | 7F | 48 | 0.5 | 1.5 | 2.5 | dB |
| Low-band boost control (3 dB) 2 | $V_{B3dB2}$ | Rin = GND, L1 OUT | | | | ↓ | 60 | | | | | | | | 1.0 | 2.0 | 3.0 | dB |
| Low-band boost control (3 dB) 3 | $V_{B3dB3}$ | | | | | E0 | 50 | | | | | | | | 2.0 | 3.0 | 4.0 | dB |
| High-band boost control | $V_{TB}$ | f = 10 kHz, Lin = 0.5 $V_{rms}$, | a | b | – | 80 | 7F | 60 | 60 | 7F | 7F | 7F | 7F | 48 | 7.0 | 10.0 | 13.0 | dB |
| High-band flat control | $V_{TF}$ | Rin = GND, L1 OUT | | | | | | | | 60 | | | | | –3.0 | 0.0 | +3.0 | dB |
| High-band cut control | $V_{TC}$ | | | | | | | | | 41 | | | | | –13.0 | –10.0 | –7.0 | dB |
| L, R in-phase gain difference 1 (1) | $DG_{11}$ | Lin = GND, Rin = 0.5 $V_{rms}$, | b | a | – | 80 | 7F | 60 | 60 | 60 | 7F | 7F | 7F | 48 | –1.0 | 0.0 | +1.0 | dB |
| L, R in-phase gain difference 1 (2) | $DG_{12}$ | L1 OUT, R1 OUT | | | | | 60 | | | | | | | | –1.0 | 0.0 | +1.0 | dB |
| L, R in-phase gain difference 2 (1) | $DG_{21}$ | Lin = GND, Rin = 0.5 $V_{rms}$, | b | a | – | 80 | 7F | 60 | 60 | 60 | 7F | 7F | 7F | 48 | –1.0 | 0.0 | +1.0 | dB |
| L, R in-phase gain difference 2 (2) | $DG_{22}$ | L2 OUT, R2 OUT | | | | | | | | | | 60 | | | –1.0 | 0.0 | +1.0 | dB |
| L, R in-phase gain difference 3 (1) | $DG_{31}$ | f = 100 Hz, Lin = 0.5 $V_{rms}$, | a | a | – | 80 | 7F | 60 | 7F | 60 | 7F | 7F | 7F | 48 | –1.0 | 0.0 | +1.0 | dB |
| L, R in-phase gain difference 3 (2) | $DG_{32}$ | Rin = 0.5 $V_{rms}$, | | | | | | | 60 | | | | | | –1.0 | 0.0 | +1.0 | dB |
| L, R in-phase gain difference 3 (3) | $DG_{33}$ | L1 OUT, R1 OUT | | | | | | | 41 | | | | | | –1.0 | 0.0 | +1.0 | dB |
| L, R in-phase gain difference 4 (1) | $DG_{41}$ | f = 10 kHz, Lin = 0.5 $V_{rms}$, | a | a | – | 80 | 7F | 60 | 60 | 7F | 7F | 7F | 7F | 48 | –1.0 | 0.0 | +1.0 | dB |
| L, R in-phase gain difference 4 (2) | $DG_{42}$ | Rin = 0.5 $V_{rms}$, | | | | | | | | 60 | | | | | –1.0 | 0.0 | +1.0 | dB |
| L, R in-phase gain difference 4 (3) | $DG_{43}$ | L1 OUT, R1 OUT | | | | | | | | 41 | | | | | –1.0 | 0.0 | +1.0 | dB |
| L, R in-phase gain difference 5 (1) | $DG_{51}$ | f = 100 Hz, Lin = 0.5 $V_{rms}$, | a | a | – | 80 | 7F | 60 | 60 | 60 | 7F | 7F | 7F | 48 | –1.0 | 0.0 | +1.0 | dB |
| L, R in-phase gain difference 5 (2) | $DG_{52}$ | Rin = 0.5 $V_{rms}$, | | | | ↓ | 60 | | | | | | | | –1.0 | 0.0 | +1.0 | dB |
| L, R in-phase gain difference 5 (3) | $DG_{53}$ | L1 OUT, R1 OUT | | | | C0 | 48 | | | | | | | | –1.0 | 0.0 | +1.0 | dB |
| L, R in-phase gain difference 6 (1) | $DG_{61}$ | f = 100 Hz, Lin = 0.5 $V_{rms}$, | a | a | – | A0 | 7F | 60 | 60 | 60 | 7F | 7F | 7F | 48 | –1.0 | 0.0 | +1.0 | dB |
| L, R in-phase gain difference 6 (2) | $DG_{62}$ | Rin = 0.5 $V_{rms}$, | | | | ↓ | 60 | | | | | | | | –1.0 | 0.0 | +1.0 | dB |
| L, R in-phase gain difference 6 (3) | $DG_{63}$ | L1 OUT, R1 OUT | | | | E0 | 48 | | | | | | | | –1.0 | 0.0 | +1.0 | dB |

–: Don't care.

**Note** See **7. MEASURING CIRCUIT**.

### (1) μPC1853CT-01 Volume control, tone control block (3/3)

| Parameter | Symbol | Test conditions | Switch mode[Note] | | | Subaddress data | | | | | | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | S1 | S2 | S3 | 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | | | | |
| Muting attenuation 1 | Mute 1 | Lin = 0.5 $V_{rms}$, Rin = GND, L1 OUT | a | b | – | 82 | 7F | 60 | 60 | 60 | 7F | 7F | 7F | 48 | –80.0 | – | – | dB |
| Muting attenuation 2 | Mute 2 | Lin = GND, Rin = 0.5 $V_{rms}$, R1 OUT | b | a | – | | | | | | | | | | –80.0 | – | – | dB |
| Muting attenuation 3 | Mute 3 | Lin = 0.5 $V_{rms}$, Rin = GND, L2 OUT | a | b | – | 84 | | | | | | | | | –80.0 | – | – | dB |
| Muting attenuation 4 | Mute 4 | Lin = GND, Rin = 0.5 $V_{rms}$, R2 OUT | b | a | – | | | | | | | | | | –80.0 | – | – | dB |
| Muting attenuation 5 | Mute 5 | Lin = 0.5 $V_{rms}$, Rin = 0.5 $V_{rms}$, L+R OUT | a | a | – | 88 | | | | | | | | | –80.0 | – | – | dB |
| Muting attenuation 6 | Mute 6 (Rear) | Lin = 0.5 $V_{rms}$, Rin = GND, Rear OUT | a | b | – | 90 | | | | | | | | | –70.0 | – | – | dB |
| DC offset at muting mode (L1 OUT, R1 OUT) | $V_{OS1}$ | No signal | b | b | – | 80 ↓ 82 | 7F | 60 | 60 | 60 | 7F | 7F | 7F | 48 | –50 | 0 | +50 | mV |
| DC offset at muting mode (L2 OUT, R2 OUT) | $V_{OS2}$ | | | | | 80 ↓ 84 | | | | | | | | | –50 | 0 | +50 | mV |
| DC offset at muting mode (L+R OUT) | $V_{OS3}$ | | | | | 80 ↓ 88 | | | | | | | | | –50 | 0 | +50 | mV |
| DC offset at muting mode (Rear OUT) | $V_{OS4}$ | | | | | 80 ↓ 90 | | | | | | | | | –50 | 0 | +50 | mV |

–: Don't care.

**Note** See **7. MEASURING CIRCUIT**.

## (2) μPC1853CT-02 Volume control, tone control block (1/2)

| Parameter | Symbol | Test conditions | Switch mode[Note] | | | Subaddress data | | | | | | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | S1 | S2 | S3 | 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | | | | |
| Volume attenuation 1 (1) L-ch | $ATT_{VL11}$ | Lin = 0.5 $V_{rms}$, | a | b | – | 80 | 7F | 7F | 60 | 60 | 7F | 7F | 7F | 48 | –1.5 | 0.0 | +1.5 | dB |
| Volume attenuation 1 (2) L-ch | $ATT_{VL12}$ | Rin = GND, | | | | | | 60 | | | | | | | –25.0 | –19.0 | –13.0 | dB |
| Volume attenuation 1 (3) L-ch | $ATT_{VL13}$ | L1 OUT | | | | | | 40 | | | | | | | –80.0 | – | – | dB |
| Volume attenuation 1 (4) R-ch | $ATT_{VR14}$ | Lin = GND, | a | b | – | 80 | 7F | 7F | 60 | 60 | 7F | 7F | 7F | 48 | –1.5 | 0.0 | +1.5 | dB |
| Volume attenuation 1 (5) R-ch | $ATT_{VR15}$ | Rin = 0.5 $V_{rms}$, R1 OUT | | | | | 60 | | | | | | | | –25.0 | –19.0 | –13.0 | dB |
| Volume attenuation 1 (6) R-ch | $ATT_{VR16}$ | | | | | | 40 | | | | | | | | –80.0 | – | – | dB |
| Volume attenuation 2 (1) | $ATT_{VL21}$ | Lin = 0.5 $V_{rms}$, Rin = GND, | a | b | – | 80 | 7F | 7F | 60 | 60 | 7F | 7F | 7F | 48 | –1.5 | 0.0 | +1.5 | dB |
| Volume attenuation 2 (2) | $ATT_{VL22}$ | L2 OUT | | | | | | | | | | 60 | | | –25.0 | –19.0 | –13.0 | dB |
| Volume attenuation 2 (3) | $ATT_{VL23}$ | | | | | | | | | | | 40 | | | –80.0 | – | – | dB |
| L+R volume attenuation 1 | $ATT_{VLR1}$ | Lin = 0.5 $V_{rms}$, Rin = 0.5 $V_{rms}$, | a | a | – | 80 | 7F | 7F | 60 | 60 | 7F | 7F | 7F | 48 | –1.5 | 0.0 | +1.5 | dB |
| L+R volume attenuation 2 | $ATT_{VLR2}$ | L+R OUT | | | | | | | | | 60 | | | | –25.0 | –19.5 | –13.0 | dB |
| L+R volume attenuation 3 | $ATT_{VLR3}$ | | | | | | | | | | 40 | | | | –80.0 | – | – | dB |
| Rear volume attenuation 1 | $ATT_{VRE1}$ | Lin = 0.5 $V_{rms}$, Rin = GND, | a | b | – | 80 | 7F | 7F | 60 | 60 | 7F | 7F | 7F | 48 | 8.5 | 10.0 | 11.5 | dB |
| Rear volume attenuation 2 | $ATT_{VRE2}$ | Rear OUT | | | | | | | | | | | 60 | | –15.0 | –9.0 | –3.0 | dB |
| Low-band boost control | $V_{BB}$ | f = 100 Hz, Lin = 0.5 $V_{rms}$, | a | b | – | 80 | 7F | 7F | 7F | 60 | 7F | 7F | 7F | 48 | 7.0 | 10.0 | 13.0 | dB |
| Low-band flat control | $V_{BF}$ | Rin = GND, L1 OUT | | | | | | | 60 | | | | | | –3.0 | 0.0 | +3.0 | dB |
| Low-band cut control | $V_{BC}$ | | | | | | | | 41 | | | | | | –13.0 | –10.0 | –7.0 | dB |
| High-band boost control | $V_{TB}$ | f = 100 kHz, Lin = 0.5 $V_{rms}$, | a | b | – | 80 | 7F | 7F | 60 | 7F | 7F | 7F | 7F | 48 | 7.0 | 10.0 | 13.0 | dB |
| High-band flat control | $V_{TF}$ | Rin = GND, L1 OUT | | | | | | | | 60 | | | | | –3.0 | 0.0 | +3.0 | dB |
| High-band cut control | $V_{TC}$ | | | | | | | | | 41 | | | | | –13.0 | –10.0 | –7.0 | dB |
| L, R in-phase gain difference 1 (1) | $DG_{11}$ | Lin = GND, Rin = 0.5 $V_{rms}$, | b | a | – | 80 | 7F | 7F | 60 | 60 | 7F | 7F | 7F | 48 | –1.0 | 0.0 | +1.0 | dB |
| L, R in-phase gain difference 1 (2) | $DG_{12}$ | L1 OUT, R1 OUT | | | | | 60 | 60 | | | | | | | –1.5 | 0.0 | +1.5 | dB |
| L, R in-phase gain difference 2 (1) | $DG_{21}$ | Lin = GND, Rin = 0.5 $V_{rms}$, | b | a | – | 80 | 7F | 7F | 60 | 60 | 7F | 7F | 7F | 48 | –1.0 | 0.0 | +1.0 | dB |
| L, R in-phase gain difference 2 (2) | $DG_{22}$ | L2 OUT, R2 OUT | | | | | | | | | | 60 | | | –1.0 | 0.0 | +1.0 | dB |

–: Don't care.

**Note** See **7. MEASURING CIRCUIT**.

### (2) μPC1853CT-02 Volume control, tone control block (2/2)

| Parameter | Symbol | Test conditions | Switch mode[Note] | | | Subaddress data | | | | | | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | S1 | S2 | S3 | 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | | | | |
| L, R in-phase gain difference 3 (1) | $DG_{31}$ | f = 100 Hz, Lin = 0.5 $V_{rms}$, | a | a | – | 80 | 7F | 7F | 7F | 60 | 7F | 7F | 7F | 48 | –1.0 | 0.0 | +1.0 | dB |
| L, R in-phase gain difference 3 (2) | $DG_{32}$ | Rin = 0.5 $V_{rms}$, | | | | | | | 60 | | | | | | –1.0 | 0.0 | +1.0 | dB |
| L, R in-phase gain difference 3 (3) | $DG_{33}$ | L1 OUT, R1 OUT | | | | | | | 41 | | | | | | –1.0 | 0.0 | +1.0 | dB |
| L, R in-phase gain difference 4 (1) | $DG_{41}$ | f = 10 kHz, Lin = 0.5 $V_{rms}$, | a | a | – | 80 | 7F | 7F | 60 | 7F | 7F | 7F | 7F | 48 | –1.0 | 0.0 | +1.0 | dB |
| L, R in-phase gain difference 4 (2) | $DG_{42}$ | Rin = 0.5 $V_{rms}$, | | | | | | | | 60 | | | | | –1.0 | 0.0 | +1.0 | dB |
| L, R in-phase gain difference 4 (3) | $DG_{43}$ | L1 OUT, R1 OUT | | | | | | | | 41 | | | | | –1.0 | 0.0 | +1.0 | dB |
| Muting attenuation 1 | Mute 1 | Lin = 0.5 $V_{rms}$, Rin = GND, L2 OUT | a | b | – | 84 | 7F | 7F | 60 | 60 | 7F | 7F | 7F | 48 | –80.0 | – | – | dB |
| Muting attenuation 2 | Mute 2 | Lin = GND, Rin = 0.5 $V_{rms}$, R2 OUT | b | a | – | | | | | | | | | | –80.0 | – | – | dB |
| Muting attenuation 3 | Mute 3 | Lin = 0.5 $V_{rms}$, Rin = 0.5 $V_{rms}$, L+R OUT | a | a | – | 88 | | | | | | | | | –80.0 | – | – | dB |
| Muting attenuation 4 | Mute 4 (Rear) | Lin = 0.5 $V_{rms}$, Rin = GND, Rear OUT | a | b | – | 90 | | | | | | | | | –70.0 | – | – | dB |
| DC offset at muting mode (L1 OUT, R1 OUT) | $V_{OS1}$ | No signal | b | b | – | 80 ↓ 82 | 7F | 7F | 60 | 60 | 7F | 7F | 7F | 48 | –50 | 0 | +50 | mV |
| DC offset at muting mode (L2 OUT, R2 OUT) | $V_{OS2}$ | | | | | 80 ↓ 84 | | | | | | | | | –50 | 0 | +50 | mV |
| DC offset at muting mode (L+R OUT) | $V_{OS3}$ | | | | | 80 ↓ 88 | | | | | | | | | –50 | 0 | +50 | mV |
| DC offset at muting mode (Rear OUT) | $V_{OS4}$ | | | | | 80 ↓ 90 | | | | | | | | | –50 | 0 | +50 | mV |

–: Don't care.

**Note** See **7. MEASURING CIRCUIT**.

**Matrix surround block (1/2)**

| Parameter | Symbol | Test conditions | Switch mode[Note1] | | | Subaddress data | | | | | | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | S1 | S2 | S3 | 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | | | | |
| In-phase gain<br>Movie mode 1 [Note2] | $G_{MOV1}$ | f = 1 kHz, Lin = 0.5 $V_{rms}$,<br>Rin = GND, L1 OUT | a | b | – | 80 | 7F | 60 | 60 | 60 | 7F | 7F | 7F | C8 | 3.0 | 7.0 | 11.0 | dB |
| In-phase gain<br>Movie mode 2 [Note2] | $G_{MOV2}$ | f = 1 kHz, Lin = 0.5 $V_{rms}$,<br>Rin = GND, R1 OUT | | | | | | | | | | | | | 0.0 | 4.0 | 8.0 | dB |
| In-phase gain<br>Music mode 1 [Note2] | $G_{MUS1}$ | f = 1 kHz, Lin = 0.5 $V_{rms}$,<br>Rin = GND, L1 OUT | | | | | | | | | | | | E8 | 3.5 | 5.5 | 7.5 | dB |
| In-phase gain<br>Music mode 2 [Note2] | $G_{MUS2}$ | f = 1 kHz, Lin = 0.5 $V_{rms}$,<br>Rin = GND, R1 OUT | | | | | | | | | | | | | –2.5 | –0.5 | +1.5 | dB |
| In-phase gain<br>Simulated mode (L-ch) 1 [Note2] | $G_{SIML1}$ | f = 250 Hz, Lin = 0.5 $V_{rms}$,<br>Rin = 0.5 $V_{rms}$, L1 OUT | a | a | – | | | | | | | | | D8 | –0.5 | +3.5 | +6.5 | dB |
| In-phase gain<br>Simulated mode (L-ch) 2 [Note2] | $G_{SIML2}$ | f = 1 kHz, Lin = 0.5 $V_{rms}$,<br>Rin = 0.5 $V_{rms}$, L1 OUT | | | | | | | | | | | | | – | –3.0 | +4.5 | dB |
| In-phase gain<br>Simulated mode (L-ch) 3 [Note2] | $G_{SIML3}$ | f = 4 kHz, Lin = 0.5 $V_{rms}$,<br>Rin = 0.5 $V_{rms}$, L1 OUT | | | | | | | | | | | | | 2.0 | 6.0 | 10.0 | dB |
| In-phase gain<br>Simulated mode (R-ch) 1 [Note2] | $G_{SIMR1}$ | f = 250 Hz, Lin = 0.5 $V_{rms}$,<br>Rin = 0.5 $V_{rms}$, R1 OUT | | | | | | | | | | | | D8 | – | –5.5 | –1.0 | dB |
| In-phase gain<br>Simulated mode (R-ch) 2 [Note2] | $G_{SIMR2}$ | f = 1 kHz, Lin = 0.5 $V_{rms}$,<br>Rin = 0.5 $V_{rms}$, R1 OUT | | | | | | | | | | | | | 0.0 | 3.0 | 6.0 | dB |
| In-phase gain<br>Simulated mode (R-ch) 3 [Note2] | $G_{SIMR3}$ | f = 4 kHz, Lin = 0.5 $V_{rms}$,<br>Rin = 0.5 $V_{rms}$, R1 OUT | | | | | | | | | | | | | – | –7.0 | +5.0 | dB |

–: Don't care.

**Note 1.** See **7. MEASURING CIRCUIT**.

**2.** See **4.3 Surround Function** about setting of surround mode.

**Remark** The values are common to both the $\mu$PC1853CT-01 and $\mu$PC1853CT-02.

**Matrix surround block (2/2)**

| Parameter | Symbol | Test conditions | Switch mode[Note] | | | Subaddress data | | | | | | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | S1 | S2 | S3 | 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | | | | |
| Output noise | NO1 | Lin = GND, Rin = GND,<br>Surround: OFF, DIN-AUDIO filter,<br>L1 OUT, R1 OUT, L2 OUT,<br>R2 OUT, L+R OUT, Rear OUT | b | b | – | 80 | 7F | 60 | 60 | 60 | 7F | 7F | 7F | 48 | – | 25 | 50 | $\mu V_{rms}$ |
| Crosstalk 1 | CT1 | Lin = 0.5 $V_{rms}$, Rin = GND,<br>0 dB: 0.5 $V_{rms}$ | a | b | – | 80 | 7F | 60 | 60 | 60 | 7F | 7F | 7F | 48 | – | –80 | –70 | dB |
| Crosstalk 2 | CT2 | Lin = GND, Rin = 0.5 $V_{rms}$,<br>0 dB: 0.5 $V_{rms}$ | b | a | – | | | | | | | | | | – | –80 | –70 | dB |
| Inter-mode offset | $V_{OSM}$ | No signal.<br>At surround mode switching. | b | b | – | 80 | 7F | 60 | 60 | 60 | 7F | 7F | 7F | ×F | –50 | 0 | +50 | mV |

–: Don't care.

**Note** See **7. MEASURING CIRCUIT**.

**Remark** The values are common to both the $\mu$PC1853CT-01 and $\mu$PC1853CT-02.

## ELECTRICAL CHARACTERISTICS MEASUREMENT LIST

Set subaddress data as shown in **4.2 Initialization** unless otherwise specified.

**General (1/1)**

| Parameter | Symbol | Test conditions | Subaddress | Data | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Supply current | $I_{CC}$ | Current flowing to pin 15.<br>No signal | | | | | | | | | |
| Maximum input voltage 1 | $V_{OM1}$ | Input signal level of pins 13, 14, 16 and 17.<br>Distortion rate of pins 13, 14, 16 and 17: 1 %<br>Pins 26 and 27: Input SIN wave (1 kHz, 2.8 $V_{rms}$). | | | | | | | | | |
| Maximum input voltage 2 | $V_{OM2}$ | Input signal level of pin 11.<br>Distortion rate of pin 11: 1 %<br>Pin 26: Input SIN wave (1 kHz, 2.8 $V_{rms}$).<br>Pin 27: No signal | | | | | | | | | |
| Distortion rate (L-ch) | $THD_L$ | Distortion rate of pins 14 and 17.<br>Pin 26: Input SIN wave (1 kHz, 0.5 $V_{rms}$).<br>Pin 27: No signal (Connect to GND with an input coupling capacitor). | | | | | | | | | |
| Distortion rate (R-ch) | $THD_R$ | Distortion rate of pins 13 and 16.<br>Pin 26: No signal (Connect to GND with an input coupling capacitor).<br>Pin 27: Input SIN wave (1 kHz, 0.5 $V_{rms}$). | | | | | | | | | |

**Remark** The methods are common to both the $\mu$PC1853CT-01 and $\mu$PC1853CT-02.

**(1) $\mu$PC1853CT-01 Volume control, tone control block** (1/9)

| Parameter | Symbol | Test conditions | Subaddress | Data | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Volume attenuation 1 (1) | $ATT_{VL11}$ | Volume attenuation = 20 log $\frac{\text{L1 output}}{\text{L input}}$ | 01 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Volume attenuation 1 (2) | $ATT_{VL12}$ | L1 output: Output signal level of pin 14. | | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| Volume attenuation 1 (3) | $ATT_{VL13}$ | L input: Input signal level of pin 26.<br>Pin 26: Input SIN wave (1 kHz, 0.5 $V_{rms}$).<br>Pin 27: No signal (Connect to GND with an input coupling capacitor). | | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| Volume attenuation 2 (1) | $ATT_{VL21}$ | Volume attenuation = 20 log $\frac{\text{L2 output}}{\text{L input}}$ | 06 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Volume attenuation 2 (2) | $ATT_{VL22}$ | L2 output: Output signal level of pin 17. | | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| Volume attenuation 2 (3) | $ATT_{VL23}$ | L input: Input signal level of pin 26.<br>Pin 26: Input SIN wave (1 kHz, 0.5 $V_{rms}$).<br>Pin 27: No signal (Connect to GND with an input coupling capacitor). | | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| L+R volume attenuation 1 | $ATT_{VLR1}$ | L+R volume attenuation = 20 log $\frac{\text{L+R output}}{\text{L, R input}}$ | 05 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| L+R volume attenuation 2 | $ATT_{VLR2}$ | L+R output: Output signal level of pin 12. | | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| L+R volume attenuation 3 | $ATT_{VLR3}$ | L, R input: Input signal level of pin 26 or 27.<br>Pin 26, 27: Input SIN wave (1 kHz, 0.5 $V_{rms}$). | | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| Rear volume attenuation 1 | $ATT_{VRE1}$ | Rear volume attenuation = 20 log $\frac{\text{Rear output}}{\text{L input}}$ | 07 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Rear volume attenuation 2 | $ATT_{VRE2}$ | Rear output: Output signal level of pin 11.<br>L input: Input signal level of pin 26.<br>Pin 26: Input SIN wave (1 kHz, 0.5 $V_{rms}$).<br>Pin 27: No signal (Connect to GND with an input coupling capacitor). | | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

## (1) μPC1853CT-01 Volume control, tone control block (2/9)

| Parameter | Symbol | Test conditions | Subaddress | Data | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Balance attenuation (L-ch) 1 (1) | $ATT_{BL11}$ | Balance attenuation = 20 log $\frac{\text{L1 output}}{\text{L input}}$ | 02 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| Balance attenuation (L-ch) 1 (2) | $ATT_{BL12}$ | L1 output: Output signal level of pin 14. | | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| | | L input: Input signal level of pin 26. | | | | | | | | | |
| Balance attenuation (L-ch) 1 (3) | $ATT_{BL13}$ | Pin 26: Input SIN wave (1 kHz, 0.5 $V_{rms}$). | | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | Pin 27: No signal (Connect to GND with an input coupling capacitor). | | | | | | | | | |
| Balance attenuation (R-ch) 1 (1) | $ATT_{BR11}$ | Balance attenuation = 20 log $\frac{\text{R1 output}}{\text{R input}}$ | 02 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| Balance attenuation (R-ch) 1 (2) | $ATT_{BR12}$ | R1 output: Output signal level of pin 13. | | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| | | R input: Input signal level of pin 27. | | | | | | | | | |
| Balance attenuation (R-ch) 1 (3) | $ATT_{BR13}$ | Pin 26: No signal (Connect to GND with an input coupling capacitor). | | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | Pin 27: Input SIN wave (1 kHz, 0.5 $V_{rms}$). | | | | | | | | | |
| Low-band boost control | $V_{BB}$ | Bass response = 20 log $\frac{\text{L1 output}}{\text{L input}}$ | 03 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Low-band flat control | $V_{BF}$ | L1 output: Output signal level of pin 14. | | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| | | L input: Input signal level of pin 26. | | | | | | | | | |
| Low-band cut control | $V_{BC}$ | Pin 26: Input SIN wave (100 Hz, 0.5 $V_{rms}$). | | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| | | Pin 27: No signal (Connect to GND with an input coupling capacitor). | | | | | | | | | |
| Low-band boost control (6 dB) 1 | $V_{B6dB1}$ | Bass response = 20 log $\frac{V_{BON}}{V_{BOFF}}$ | 00 | 1 | 0 ↓ 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | $V_{BON}$: Output signal level of pin 14 (Low boost: ON). | 01 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Low-band boost control (6 dB) 2 | $V_{B6dB2}$ | $V_{BOFF}$: Output signal level of pin 14 (Low boost: OFF). | 00 | 1 | 0 ↓ 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Pin 26: Input SIN wave (100 Hz, 0.5 $V_{rms}$). | | | | | | | | | |
| | | Pin 27: No signal (Connect to GND with an input coupling capacitor). | 01 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

**(1) $\mu$PC1853CT-01 Volume control, tone control block** (3/9)

| Parameter | Symbol | Test conditions | Subaddress | Data | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Low-band boost control (6 dB) 3 | $V_{B6dB3}$ | Bass response = 20 log $\frac{V_{BON}}{V_{BOFF}}$<br>$V_{BON}$ : Output signal level of pin 14 (Low boost: ON).<br>$V_{BOFF}$: Output signal level of pin 14 (Low boost: OFF).<br>Pin 26: Input SIN wave (100 Hz, 0.5 $V_{rms}$).<br>Pin 27: No signal (Connect to GND with an input coupling capacitor). | 00 | 1 | 0 ↓ 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | 01 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| Low-band boost control (3 dB) 1 | $V_{B3dB1}$ | | 00 | 1 | 0 ↓ 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| | | | 01 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Low-band boost control (3 dB) 2 | $V_{B3dB2}$ | | 00 | 1 | 0 ↓ 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| | | | 01 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| Low-band boost control (3 dB) 3 | $V_{B3dB3}$ | | 00 | 1 | 0 ↓ 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| | | | 01 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| High-band boost control | $V_{TB}$ | Treble response = 20 log $\frac{\text{L1 output}}{\text{L input}}$<br>L1 output: Output signal level of pin 14.<br>L input: Input signal level of pin 26.<br>Pin 26: Input SIN wave (10 kHz, 0.5 $V_{rms}$).<br>Pin 27: No signal (Connect to GND with an input coupling capacitor). | 04 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| High-band flat control | $V_{TF}$ | | | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| High-band cut control | $V_{TC}$ | | | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |

**(1) $\mu$PC1853CT-01 Volume control, tone control block** (4/9)

| Parameter | Symbol | Test conditions | Subaddress | Data | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| L, R in-phase gain difference 1 (1) | $DG_{11}$ | Channel to channel error = 20 log $\frac{\text{R1 output}}{\text{R input}}$ – $ATT_{VL11}$<br>R1 output: Output signal level of pin 13.<br>R input: Input signal level of pin 27.<br>$ATT_{VL11}$: Gain of the Volume attenuation 1 (1).<br>Pin 26: No signal (Connect to GND with an input coupling capacitor).<br>Pin 27: Input SIN wave (1 kHz, 0.5 $V_{rms}$). | 01 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| L, R in-phase gain difference 1 (2) | $DG_{12}$ | Channel to channel error = 20 log $\frac{\text{R1 output}}{\text{R input}}$ – $ATT_{VL12}$<br>R1 output: Output signal level of pin 13.<br>R input: Input signal level of pin 27.<br>$ATT_{VL12}$: Gain of the Volume attenuation 1 (2).<br>Pin 26: No signal (Connect to GND with an input coupling capacitor).<br>Pin 27: Input SIN wave (1 kHz, 0.5 $V_{rms}$). | | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| L, R in-phase gain difference 2 (1) | $DG_{21}$ | Channel to channel error = 20 log $\frac{\text{R2 output}}{\text{R input}}$ – $ATT_{VL21}$<br>R2 output: Output signal level of pin 16.<br>R input: Input signal level of pin 27.<br>$ATT_{VL21}$: Gain of the Volume attenuation 2 (1).<br>Pin 26: No signal (Connect to GND with an input coupling capacitor).<br>Pin 27: Input SIN wave (1 kHz, 0.5 $V_{rms}$). | 06 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| L, R in-phase gain difference 2 (2) | $DG_{22}$ | Channel to channel error = 20 log $\frac{\text{R2 output}}{\text{R input}}$ – $ATT_{VL22}$<br>R2 output: Output signal level of pin 16.<br>R input: Input signal level of pin 27.<br>$ATT_{VL22}$: Gain of the Volume attenuation 2 (2).<br>Pin 26: No signal (Connect to GND with an input coupling capacitor).<br>Pin 27: Input SIN wave (1 kHz, 0.5 $V_{rms}$). | | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

**(1) $\mu$PC1853CT-01 Volume control, tone control block** (5/9)

| Parameter | Symbol | Test conditions | Subaddress | Data | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| L, R in-phase gain difference 3 (1) | $DG_{31}$ | Channel to channel error = 20 log $\frac{\text{R1 output}}{\text{R input}} - V_{BB}$<br>R1 output: Output signal level of pin 13.<br>R input: Input signal level of pin 27.<br>$V_{BB}$: Gain of the Low-band boost control.<br>Pin 26: No signal (Connect to GND with an input coupling capacitor).<br>Pin 27: Input SIN wave (100 Hz, 0.5 $V_{rms}$). | 03 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| L, R in-phase gain difference 3 (2) | $DG_{32}$ | Channel to channel error = 20 log $\frac{\text{R1 output}}{\text{R input}} - V_{BF}$<br>R1 output: Output signal level of pin 13.<br>R input: Input signal level of pin 27.<br>$V_{BF}$: Gain of the Low-band flat control.<br>Pin 26: No signal (Connect to GND with an input coupling capacitor).<br>Pin 27: Input SIN wave (100 Hz, 0.5 $V_{rms}$). | | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| L, R in-phase gain difference 3 (3) | $DG_{33}$ | Channel to channel error = 20 log $\frac{\text{R1 output}}{\text{R input}} - V_{BC}$<br>R1 output: Output signal level of pin 13.<br>R input: Input signal level of pin 27.<br>$V_{BC}$: Gain of the Low-band cut control.<br>Pin 26: No signal (Connect to GND with an input coupling capacitor).<br>Pin 27: Input SIN wave (100 Hz, 0.5 $V_{rms}$). | | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| L, R in-phase gain difference 4 (1) | $DG_{41}$ | Channel to channel error = 20 log $\frac{\text{R1 output}}{\text{R input}} - V_{TB}$<br>R1 output: Output signal level of pin 13.<br>R input: Input signal level of pin 27.<br>$V_{TB}$: Gain of the High-band boost control.<br>Pin 26: No signal (Connect to GND with an input coupling capacitor).<br>Pin 27: Input SIN wave (10 kHz, 0.5 $V_{rms}$). | 05 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

**(1) $\mu$PC1853CT-01 Volume control, tone control block** (6/9)

| Parameter | Symbol | Test conditions | Subaddress | Data | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| L, R in-phase gain difference 4 (2) | $DG_{42}$ | Channel to channel error = 20 log $\frac{\text{R1 output}}{\text{R input}} - V_{TF}$<br>R1 output: Output signal level of pin 13.<br>R input: Input signal level of pin 27.<br>$V_{TF}$: Gain of the High-band flat control.<br>Pin 26: No signal (Connect to GND with an input coupling capacitor).<br>Pin 27: Input SIN wave (10 kHz, 0.5 $V_{rms}$). | 05 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| L, R in-phase gain difference 4 (3) | $DG_{43}$ | Channel to channel error = 20 log $\frac{\text{R1 output}}{\text{R input}} - V_{TC}$<br>R1 output: Output signal level of pin 13.<br>R input: Input signal level of pin 27.<br>$V_{TC}$: Gain of the High-band cut control.<br>Pin 26: No signal (Connect to GND with an input coupling capacitor).<br>Pin 27: Input SIN wave (10 kHz, 0.5 $V_{rms}$). | | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| L, R in-phase gain difference 5 (1) | $DG_{51}$ | Channel to channel error = 20 log $\frac{V_{BON}}{V_{BOFF}} - V_{B6dB1}$<br>$V_{BON}$ : Output signal level of pin 13 (Low boost: ON).<br>$V_{BOFF}$ : Output signal level of pin 13 (Low boost: OFF).<br>$V_{B6dB1}$: Gain of the Low-band boost control (6 dB) 1.<br>Pin 26: No signal (Connect to GND with an input coupling capacitor).<br>Pin 27: Input SIN wave (100 Hz, 0.5 $V_{rms}$). | 00 | 1 | 0 ↓ 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | 01 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| L, R in-phase gain difference 5 (2) | $DG_{52}$ | Channel to channel error = 20 log $\frac{V_{BON}}{V_{BOFF}} - V_{B6dB2}$<br>$V_{BON}$ : Output signal level of pin 13 (Low boost: ON).<br>$V_{BOFF}$ : Output signal level of pin 13 (Low boost: OFF).<br>$V_{B6dB2}$: Gain of the Low-band boost control (6 dB) 2.<br>Pin 26: No signal (Connect to GND with an input coupling capacitor).<br>Pin 27: Input SIN wave (100 Hz, 0.5 $V_{rms}$). | 00 | 1 | 0 ↓ 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | 01 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

**(1) $\mu$PC1853CT-01 Volume control, tone control block** (7/9)

| Parameter | Symbol | Test conditions | Subaddress | Data | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| L, R in-phase gain difference 5 (3) | $DG_{53}$ | Channel to channel error = 20 log $\frac{V_{BON}}{V_{BOFF}} - V_{B6dB3}$<br>$V_{BON}$ : Output signal level of pin 13 (Low boost: ON).<br>$V_{BOFF}$ : Output signal level of pin 13 (Low boost: OFF).<br>$V_{B6dB3}$: Gain of the Low-band boost control (6 dB) 3.<br>Pin 26: No signal (Connect to GND with an input coupling capacitor).<br>Pin 27: Input SIN wave (100 Hz, 0.5 $V_{rms}$). | 00 | 1 | 0 ↓ 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | 01 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| L, R in-phase gain difference 6 (1) | $DG_{61}$ | Channel to channel error = 20 log $\frac{V_{BON}}{V_{BOFF}} - V_{B3dB1}$<br>$V_{BON}$ : Output signal level of pin 13 (Low boost: ON).<br>$V_{BOFF}$: Output signal level of pin 13 (Low boost: OFF).<br>$V_{B3dB1}$: Gain of the Low-band boost control (3 dB) 1.<br>Pin 26: No signal (Connect to GND with an input coupling capacitor).<br>Pin 27: Input SIN wave (100 Hz, 0.5 $V_{rms}$). | 00 | 1 | 0 ↓ 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| | | | 01 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| L, R in-phase gain difference 6 (2) | $DG_{62}$ | Channel to channel error = 20 log $\frac{V_{BON}}{V_{BOFF}} - V_{B3dB2}$<br>$V_{BON}$ : Output signal level of pin 13 (Low boost: ON).<br>$V_{BOFF}$: Output signal level of pin 13 (Low boost: OFF).<br>$V_{B3dB2}$: Gain of the Low-band boost control (3 dB) 2.<br>Pin 26: No signal (Connect to GND with an input coupling capacitor).<br>Pin 27: Input SIN wave (100 Hz, 0.5 $V_{rms}$). | 00 | 1 | 0 ↓ 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| | | | 01 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| L, R in-phase gain difference 6 (3) | $DG_{63}$ | Channel to channel error = 20 log $\frac{V_{BON}}{V_{BOFF}} - V_{B3dB3}$<br>$V_{BON}$ : Output signal level of pin 13 (Low boost: ON).<br>$V_{BOFF}$ : Output signal level of pin 13 (Low boost: OFF).<br>$V_{B3dB3}$: Gain of the Low-band boost control (3 dB) 3.<br>Pin 26: No signal (Connect to GND with an input coupling capacitor).<br>Pin 27: Input SIN wave (100 Hz, 0.5 $V_{rms}$). | 00 | 1 | 0 ↓ 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| | | | 01 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |

**(1) $\mu$PC1853CT-01 Volume control, tone control block** (8/9)

| Parameter | Symbol | Test conditions | Subaddress | Data | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Muting attenuation 1 | Mute 1 | Mute 1 = 20 log $\frac{\text{L1 output}}{\text{L input}}$<br>L1 output : Output signal level of pin 14.<br>L input: Input signal level of pin 26.<br>Pin 26: Input SIN wave (1 kHz, 0.5 $V_{rms}$).<br>Pin 27: No signal (Connect to GND with an input coupling capacitor). | 00 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| Muting attenuation 2 | Mute 2 | Mute 2 = 20 log $\frac{\text{R1 output}}{\text{R input}}$<br>R1 output : Output signal level of pin 13.<br>R input: Input signal level of pin 27.<br>Pin 26: No signal (Connect to GND with an input coupling capacitor).<br>Pin 27: Input SIN wave (1 kHz, 0.5 $V_{rms}$). | | | | | | | | | |
| Muting attenuation 3 | Mute 3 | Mute 3 = 20 log $\frac{\text{L2 output}}{\text{L input}}$<br>L2 output : Output signal level of pin 17.<br>L input: Input signal level of pin 26.<br>Pin 26: Input SIN wave (1 kHz, 0.5 $V_{rms}$).<br>Pin 27: No signal (Connect to GND with an input coupling capacitor). | | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| Muting attenuation 4 | Mute 4 | Mute 4 = 20 log $\frac{\text{R2 output}}{\text{R input}}$<br>R2 output : Output signal level of pin 16.<br>R input: Input signal level of pin 27.<br>Pin 26: No signal (Connect to GND with an input coupling capacitor).<br>Pin 27: Input SIN wave (1 kHz, 0.5 $V_{rms}$). | | | | | | | | | |

**(1) $\mu$PC1853CT-01 Volume control, tone control block** (9/9)

| Parameter | Symbol | Test conditions | Subaddress | Data | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Muting attenuation 5 | Mute 5 | Mute 5 = 20 log $\frac{\text{L+R output}}{\text{L, R input}}$<br>L+R output : Output signal level of pin 12.<br>L, R input: Input signal level of pin 26 or 27.<br>Pins 26 and 27: Input SIN wave (1 kHz, 0.5 $V_{rms}$). | 00 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| Muting attenuation 6 | Mute 6<br>(Rear) | Mute 6 = 20 log $\frac{\text{Rear output}}{\text{L input}}$<br>Rear output : Output signal level of pin 11.<br>L input: Input signal level of pin 26.<br>Pin 26: Input SIN wave (1 kHz, 0.5 $V_{rms}$).<br>Pin 27: No signal (Connect to GND with an input coupling capacitor). | | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| DC offset at muting mode<br>(L1 OUT, R1 OUT) | $V_{OS1}$ | $V_{OS1} = V_1 - V_0$<br>$V_1$: DC voltage of pin 14 or 13 (Main output mute: ON).<br>$V_0$: DC voltage of pin 14 or 13 (Main output mute: OFF).<br>Pins 26 and 27: Connect to GND with an input coupling capacitor. | 00 | 1 | 0 | 0 | 0 | 0 | 0 | 0<br>↓<br>1 | 0 |
| DC offset at muting mode<br>(L2 OUT, R2 OUT) | $V_{OS2}$ | $V_{OS2} = V_1 - V_0$<br>$V_1$: DC voltage of pin 17 or 16 (Audio output mute: ON).<br>$V_0$: DC voltage of pin 17 or 16 (Audio output mute: OFF).<br>Pins 26 and 27: Connect to GND with an input coupling capacitor. | | 1 | 0 | 0 | 0 | 0 | 0<br>↓<br>1 | 0 | 0 |
| DC offset at muting mode<br>(L+R OUT) | $V_{OS3}$ | $V_{OS3} = V_1 - V_0$<br>$V_1$: DC voltage of pin 12 (L+R output mute: ON).<br>$V_0$: DC voltage of pin 12 (L+R output mute: OFF).<br>Pins 26 and 27: Connect to GND with an input coupling capacitor. | | 1 | 0 | 0 | 0 | 0<br>↓<br>1 | 0 | 0 | 0 |
| DC offset at muting mode<br>(Rear OUT) | $V_{OS4}$ | $V_{OS4} = V_1 - V_0$<br>$V_1$: DC voltage of pin 11 (Rear output mute: ON).<br>$V_0$: DC voltage of pin 11 (Rear output mute: OFF).<br>Pins 26 and 27: Connect to GND with an input coupling capacitor. | | 1 | 0 | 0 | 0<br>↓<br>1 | 0 | 0 | 0 | 0 |

## (2) μPC1853CT-02 Volume control, tone control block (1/6)

| Parameter | Symbol | Test conditions | Subaddress | Data | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Volume attenuation 1 (1) L-ch | $ATT_{VL11}$ | Volume attenuation = 20 log $\frac{\text{L1 output}}{\text{L input}}$<br>L1 output: Output signal level of pin 14.<br>L input: Input signal level of pin 26.<br>Pin 26: Input SIN wave (1 kHz, 0.5 $V_{rms}$).<br>Pin 27: No signal (Connect to GND with an input coupling capacitor). | 02 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Volume attenuation 1 (2) L-ch | $ATT_{VL12}$ | | | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| Volume attenuation 1 (3) L-ch | $ATT_{VL13}$ | | | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| Volume attenuation 1 (4) R-ch | $ATT_{VR14}$ | Volume attenuation = 20 log $\frac{\text{R1 output}}{\text{R input}}$<br>R1 output: Output signal level of pin 13.<br>R input: Input signal level of pin 27.<br>Pin 26: No signal (Connect to GND with an input coupling capacitor).<br>Pin 27: Input SIN wave (1 kHz, 0.5 $V_{rms}$). | 01 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Volume attenuation 1 (5) R-ch | $ATT_{VR15}$ | | | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| Volume attenuation 1 (6) R-ch | $ATT_{VR16}$ | | | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| Volume attenuation 2 (1) | $ATT_{VL21}$ | Volume attenuation = 20 log $\frac{\text{L2 output}}{\text{L input}}$<br>L2 output: Output signal level of pin 17.<br>L input: Input signal level of pin 26.<br>Pin 26: Input SIN wave (1 kHz, 0.5 $V_{rms}$).<br>Pin 27: No signal (Connect to GND with an input coupling capacitor). | 06 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Volume attenuation 2 (2) | $ATT_{VL22}$ | | | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| Volume attenuation 2 (3) | $ATT_{VL23}$ | | | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| L+R volume attenuation 1 | $ATT_{VLR1}$ | L+R volume attenuation = 20 log $\frac{\text{L+R output}}{\text{L, R input}}$<br>L+R output: Output signal level of pin 12.<br>L, R input: Input signal level of pin 26 or 27.<br>Pin 26, 27: Input SIN wave (1 kHz, 0.5 $V_{rms}$). | 05 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| L+R volume attenuation 2 | $ATT_{VLR2}$ | | | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| L+R volume attenuation 3 | $ATT_{VLR3}$ | | | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

**(2) $\mu$PC1853CT-02 Volume control, tone control block** (2/6)

| Parameter | Symbol | Test conditions | Subaddress | Data | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Rear volume attenuation 1 | $ATT_{VRE1}$ | Rear volume attenuation = 20 log $\frac{\text{Rear output}}{\text{L input}}$<br>Rear output: Output signal level of pin 11. | 07 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Rear volume attenuation 2 | $ATT_{VRE2}$ | L input: Input signal level of pin 26.<br>Pin 26: Input SIN wave (1 kHz, 0.5 $V_{rms}$).<br>Pin 27: No signal (Connect to GND with an input coupling capacitor). | | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| Low-band boost control | $V_{BB}$ | Bass response = 20 log $\frac{\text{L1 output}}{\text{L input}}$<br>L1 output: Output signal level of pin 14.<br>L input: Input signal level of pin 26.<br>Pin 26: Input SIN wave (100 Hz, 0.5 $V_{rms}$).<br>Pin 27: No signal (Connect to GND with an input coupling capacitor). | 03 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Low-band flat control | $V_{BF}$ | | | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| Low-band cut control | $V_{BC}$ | | | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| High-band boost control | $V_{TB}$ | Treble response = 20 log $\frac{\text{L1 output}}{\text{L input}}$<br>L1 output: Output signal level of pin 14.<br>L input: Input signal level of pin 26.<br>Pin 26: Input SIN wave (10 kHz, 0.5 $V_{rms}$).<br>Pin 27: No signal (Connect to GND with an input coupling capacitor). | 04 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| High-band flat control | $V_{TF}$ | | | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| High-band cut control | $V_{TC}$ | | | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| L, R in-phase gain difference 1 (1) | $DG_{11}$ | Channel to channel error = 20 log $\frac{\text{R1 output}}{\text{R input}}$ – $ATT_{VL11}$<br>R1 output : Output signal level of pin 13.<br>R input: Input signal level of pin 27.<br>$ATT_{VL11}$: Gain of the Volume attenuation 1 (1).<br>Pin 26: No signal (Connect to GND with an input coupling capacitor).<br>Pin 27: Input SIN wave (1 kHz, 0.5 $V_{rms}$).<br>Same method about L-ch input/output signal | 01<br>02 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

**(2) $\mu$PC1853CT-02 Volume control, tone control block** (3/6)

| Parameter | Symbol | Test conditions | Subaddress | Data | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| L, R in-phase gain difference 1 (2) | $DG_{12}$ | Channel to channel error = 20 log $\frac{\text{R1 output}}{\text{R input}}$ – $ATT_{VL12}$<br>R1 output : Output signal level of pin 13.<br>R input: Input signal level of pin 27.<br>$ATT_{VL12}$: Gain of the Volume attenuation 1 (2).<br>Pin 26: No signal (Connect to GND with an input coupling capacitor).<br>Pin 27: Input SIN wave (1 kHz, 0.5 $V_{rms}$).<br>Same method about L-ch input/output signal | 01<br>02 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| L, R in-phase gain difference 2 (1) | $DG_{21}$ | Channel to channel error = 20 log $\frac{\text{R2 output}}{\text{R input}}$ – $ATT_{VL21}$<br>R2 output : Output signal level of pin 16.<br>R input: Input signal level of pin 27.<br>$ATT_{VL21}$: Gain of the Volume attenuation 2 (1).<br>Pin 26: No signal (Connect to GND with an input coupling capacitor).<br>Pin 27: Input SIN wave (1 kHz, 0.5 $V_{rms}$). | 06 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| L, R in-phase gain difference 2 (2) | $DG_{22}$ | Channel to channel error = 20 log $\frac{\text{R2 output}}{\text{R input}}$ – $ATT_{VL22}$<br>R2 output : Output signal level of pin 16.<br>R input: Input signal level of pin 27.<br>$ATT_{VL22}$: Gain of the Volume attenuation 2 (2).<br>Pin 26: No signal (Connect to GND with an input coupling capacitor).<br>Pin 27: Input SIN wave (1 kHz, 0.5 $V_{rms}$). | | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| L, R in-phase gain difference 3 (1) | $DG_{31}$ | Channel to channel error = 20 log $\frac{\text{R1 output}}{\text{R input}}$ – $V_{BB}$<br>R1 output : Output signal level of pin 13.<br>R input: Input signal level of pin 27.<br>$V_{BB}$: Gain of the Low-band boost control.<br>Pin 26: No signal (Connect to GND with an input coupling capacitor).<br>Pin 27: Input SIN wave (100 Hz, 0.5 $V_{rms}$). | 03 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

**(2) $\mu$PC1853CT-02 Volume control, tone control block** (4/6)

| Parameter | Symbol | Test conditions | Subaddress | Data | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| L, R in-phase gain difference 3 (2) | $DG_{32}$ | Channel to channel error = 20 log $\frac{\text{R1 output}}{\text{R input}} - V_{BF}$<br>R1 output : Output signal level of pin 13.<br>R input: Input signal level of pin 27.<br>$V_{BF}$: Gain of the Low-band flat control.<br>Pin 26: No signal (Connect to GND with an input coupling capacitor).<br>Pin 27: Input SIN wave (100 Hz, 0.5 $V_{rms}$). | 03 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| L, R in-phase gain difference 3 (3) | $DG_{33}$ | Channel to channel error = 20 log $\frac{\text{R1 output}}{\text{R input}} - V_{BC}$<br>R1 output : Output signal level of pin 13.<br>R input: Input signal level of pin 27.<br>$V_{BC}$: Gain of the Low-band cut control.<br>Pin 26: No signal (Connect to GND with an input coupling capacitor).<br>Pin 27: Input SIN wave (100 Hz, 0.5 $V_{rms}$). | | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| L, R in-phase gain difference 4 (1) | $DG_{41}$ | Channel to channel error = 20 log $\frac{\text{R1 output}}{\text{R input}} - V_{TB}$<br>R1 output : Output signal level of pin 13.<br>R input: Input signal level of pin 27.<br>$V_{TB}$: Gain of the High-band boost control.<br>Pin 26: No signal (Connect to GND with an input coupling capacitor).<br>Pin 27: Input SIN wave (10 kHz, 0.5 $V_{rms}$). | 05 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| L, R in-phase gain difference 4 (2) | $DG_{42}$ | Channel to channel error = 20 log $\frac{\text{R1 output}}{\text{R input}} - V_{TF}$<br>R1 output : Output signal level of pin 13.<br>R input: Input signal level of pin 27.<br>$V_{TF}$: Gain of the High-band flat control.<br>Pin 26: No signal (Connect to GND with an input coupling capacitor).<br>Pin 27: Input SIN wave (10 kHz, 0.5 $V_{rms}$). | | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

**(2) $\mu$PC1853CT-02 Volume control, tone control block** (5/6)

| Parameter | Symbol | Test conditions | Subaddress | Data | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| L, R in-phase gain difference 4 (3) | $DG_{43}$ | Channel to channel error = 20 log $\frac{\text{R1 output}}{\text{R input}} - V_{TC}$<br>R1 output : Output signal level of pin 13.<br>R input: Input signal level of pin 27.<br>$V_{TC}$: Gain of the High-band cut control.<br>Pin 26: No signal (Connect to GND with an input coupling capacitor).<br>Pin 27: Input SIN wave (10 kHz, 0.5 $V_{rms}$). | 05 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| Muting attenuation 1 | Mute 1 | Mute 1 = 20 log $\frac{\text{L2 output}}{\text{L input}}$<br>L2 output : Output signal level of pin 17.<br>L input: Input signal level of pin 26.<br>Pin 26: Input SIN wave (1 kHz, 0.5 $V_{rms}$).<br>Pin 27: No signal (Connect to GND with an input coupling capacitor). | 00 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| Muting attenuation 2 | Mute 2 | Mute 2 = 20 log $\frac{\text{R2 output}}{\text{R input}}$<br>R2 output : Output signal level of pin 16.<br>R input: Input signal level of pin 27.<br>Pin 26: No signal (Connect to GND with an input coupling capacitor).<br>Pin 27: Input SIN wave (1 kHz, 0.5 $V_{rms}$). | | | | | | | | | |
| Muting attenuation 3 | Mute 3 | Mute 3 = 20 log $\frac{\text{L+R output}}{\text{L, R input}}$<br>L+R output : Output signal level of pin 12.<br>L, R input: Input signal level of pin 26 or 27.<br>Pins 26 and 27: Input SIN wave (1 kHz, 0.5 $V_{rms}$). | | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

**(2) $\mu$PC1853CT-02 Volume control, tone control block** (6/6)

| Parameter | Symbol | Test conditions | Subaddress | Data | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Muting attenuation 4 | Mute 4 (Rear) | Mute 4 = 20 log $\frac{\text{Rear output}}{\text{L input}}$<br>Rear output : Output signal level of pin 11.<br>L input: Input signal level of pin 26.<br>Pin 26: Input SIN wave (1 kHz, 0.5 $V_{rms}$).<br>Pin 27: No signal (Connect to GND with an input coupling capacitor). | 00 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| DC offset at muting mode (L1OUT, R1 OUT) | $V_{OS1}$ | $V_{OS1} = V_1 - V_0$<br>$V_1$: DC voltage of pin 14 or 13 (Main output mute: ON).<br>$V_0$: DC voltage of pin 14 or 13 (Main output mute: OFF).<br>Pins 26 and 27: Connect to GND with an input coupling capacitor. | 00 | 1 | 0 | 0 | 0 | 0 | 0 | 0 ↓ 1 | 0 |
| DC offset at muting mode (L2 OUT, R2 OUT) | $V_{OS2}$ | $V_{OS2} = V_1 - V_0$<br>$V_1$: DC voltage of pin 17 or 16 (Audio output mute: ON).<br>$V_0$: DC voltage of pin 17 or 16 (Audio output mute: OFF).<br>Pins 26 and 27: Connect to GND with an input coupling capacitor. | | 1 | 0 | 0 | 0 | 0 | 0 ↓ 1 | 0 | 0 |
| DC offset at muting mode (L+R OUT) | $V_{OS3}$ | $V_{OS3} = V_1 - V_0$<br>$V_1$: DC voltage of pin 12 (L+R output mute: ON).<br>$V_0$: DC voltage of pin 12 (L+R output mute: OFF).<br>Pins 26 and 27: Connect to GND with an input coupling capacitor. | | 1 | 0 | 0 | 0 | 0 ↓ 1 | 0 | 0 | 0 |
| DC offset at muting mode (Rear OUT) | $V_{OS4}$ | $V_{OS4} = V_1 - V_0$<br>$V_1$: DC voltage of pin 11 (Rear output mute: ON).<br>$V_0$: DC voltage of pin 11 (Rear output mute: OFF).<br>Pins 26 and 27: Connect to GND with an input coupling capacitor. | | 1 | 0 | 0 | 0 ↓ 1 | 0 | 0 | 0 | 0 |

**Matrix surround block** (1/3)

| Parameter | Symbol | Test conditions | Subaddress | Data | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| In-phase gain<br>Movie mode 1 | $G_{MOV1}$ | Response = 20 log $\frac{\text{L1, R1 output}}{\text{L input}}$<br>L1, R1 output: Output signal level of pin 14 or 13.<br>L input: Input signal level of pin 26.<br>Pin 26: Input SIN wave (1 kHz, 0.5 $V_{rms}$).<br>Pin 27: No signal (Connect to GND with an input coupling capacitor). | 08 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| In-phase gain<br>Movie mode 2 | $G_{MOV2}$ | | | | | | | | | | |
| In-phase gain<br>Music mode 1 | $G_{MUS1}$ | Response = 20 log $\frac{\text{L1, R1 output}}{\text{L input}}$<br>L1, R1 output: Output signal level of pin 14 or 13.<br>L input: Input signal level of pin 26.<br>Pin 26: Input SIN wave (1 kHz, 0.5 $V_{rms}$).<br>Pin 27: No signal (Connect to GND with an input coupling capacitor). | 08 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 |
| In-phase gain<br>Music mode 2 | $G_{MUS2}$ | | | | | | | | | | |
| In-phase gain<br>Simulated mode<br>(L-ch) 1 | $G_{SIML1}$ | Response = 20 log $\frac{\text{L1 output}}{\text{L, R input}}$<br>L1 output : Output signal level of pin 14.<br>L, R input: Input signal level of pin 26 or 27.<br>Pins 26 and 27: Input SIN wave (250 Hz, 0.5 $V_{rms}$). | 08 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| In-phase gain<br>Simulated mode<br>(L-ch) 2 | $G_{SIML2}$ | Response = 20 log $\frac{\text{L1 output}}{\text{L, R input}}$<br>L1 output : Output signal level of pin 14.<br>L, R input: Input signal level of pin 26 or 27.<br>Pins 26 and 27: Input SIN wave (1 kHz, 0.5 $V_{rms}$). | | | | | | | | | |
| In-phase gain<br>Simulated mode<br>(L-ch) 3 | $G_{SIML3}$ | Response = 20 log $\frac{\text{L1 output}}{\text{L, R input}}$<br>L1 output : Output signal level of pin 14.<br>L, R input: Input signal level of pin 26 or 27.<br>Pins 26 and 27: Input SIN wave (4 kHz, 0.5 $V_{rms}$). | | | | | | | | | |

**Remark** The methods are common to both the $\mu$PC1853CT-01 and $\mu$PC1853CT-02.

**Matrix surround block** (2/3)

| Parameter | Symbol | Test conditions | Subaddress | Data | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| In-phase gain<br>Simulated mode<br>(R-ch) 1 | $G_{SIMR1}$ | Response = 20 log $\frac{\text{R1 output}}{\text{L, R input}}$<br>R1 output: Output signal level of pin 13.<br>L, R input: Input signal level of pin 26 or 27.<br>Pins 26 and 27: Input SIN wave (250 Hz, 0.5 $V_{rms}$). | 08 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| In-phase gain<br>Simulated mode<br>(R-ch) 2 | $G_{SIMR2}$ | Response = 20 log $\frac{\text{R1 output}}{\text{L, R input}}$<br>R1 output: Output signal level of pin 13.<br>L, R input: Input signal level of pin 26 or 27.<br>Pins 26 and 27: Input SIN wave (1 kHz, 0.5 $V_{rms}$). | | | | | | | | | |
| In-phase gain<br>Simulated mode<br>(R-ch) 3 | $G_{SIMR3}$ | Response = 20 log $\frac{\text{R1 output}}{\text{L, R input}}$<br>R1 output : Output signal level of pin 13.<br>L, R input: Input signal level of pin 26 or 27.<br>Pins 26 and 27: Input SIN wave (4 kHz, 0.5 $V_{rms}$). | | | | | | | | | |
| Output noise | NO1 | NO1: Output noise voltage of pins 11, 12, 13, 14, 16 and 17.<br>Pins 26 and 27: Connect to GND with an input coupling capacitor.<br>Filter of noise meter: DIN-AUDIO filter | | | | | | | | | |
| Crosstalk 1 | CT1 | Crosstalk = 20 log $\frac{\text{R output}}{\text{L input}}$<br>R output: Output signal level of pin 13 or 16.<br>L input: Input signal level of pin 26.<br>Pin 26: Input SIN wave (1 kHz. 0.5 $V_{rms}$).<br>Pin 27: No signal (Connect to GND with an input coupling capacitor). | | | | | | | | | |

**Remark** The methods are common to both the $\mu$PC1853CT-01 and $\mu$PC1853CT-02.

**Matrix surround block** (3/3)

| Parameter | Symbol | Test conditions | Subaddress | Data | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Crosstalk 2 | CT2 | $\text{Crosstalk} = 20 \log \frac{\text{L output}}{\text{R input}}$<br>L output : Output signal level of pin 14 or 17.<br>R input: Input signal level of pin 27.<br>Pin 26: No signal (Connect to GND with an input coupling capacitor).<br>Pin 27: Input SIN wave (1 kHz. 0.5 $V_{rms}$). | | | | | | | | | |
| Inter-mode offset | $V_{OSM}$ | No signal.<br>At surround mode switching.**Note** | 08 | × | 1 | × | × | 1 | 1 | 1 | 1 |

**Note** See **4.3 Surround Function.**

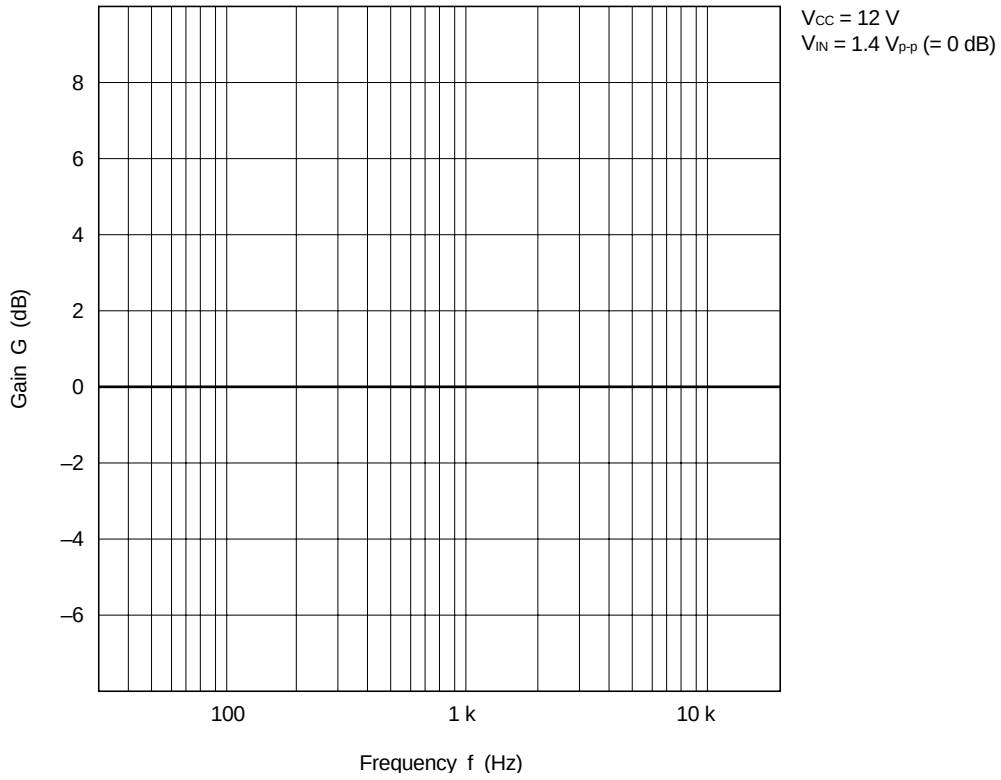
**Remark** The methods are common to both the μPC1853CT-01 and μPC1853CT-02.

## 6. CHARACTERISTIC CURVES

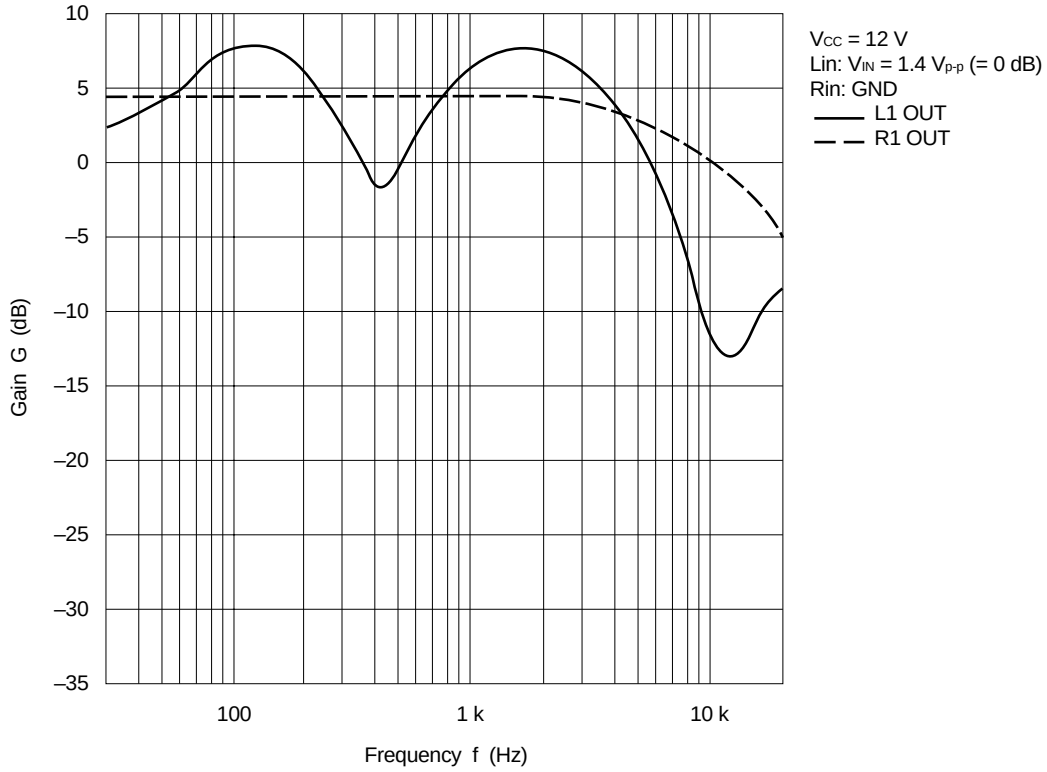
About surround mode, see **4.3 Surround Function.**

### 6.1 Frequency Response Characteristics in Each Mode

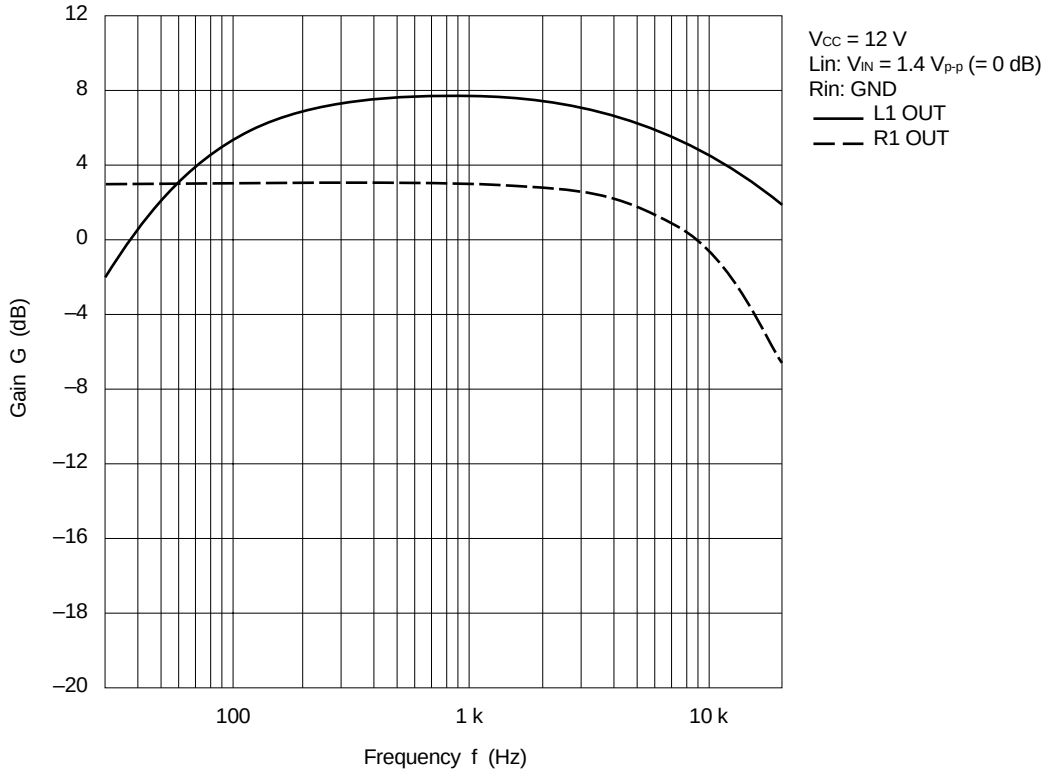
**(1) OFF mode (L-channel, R-channel)**



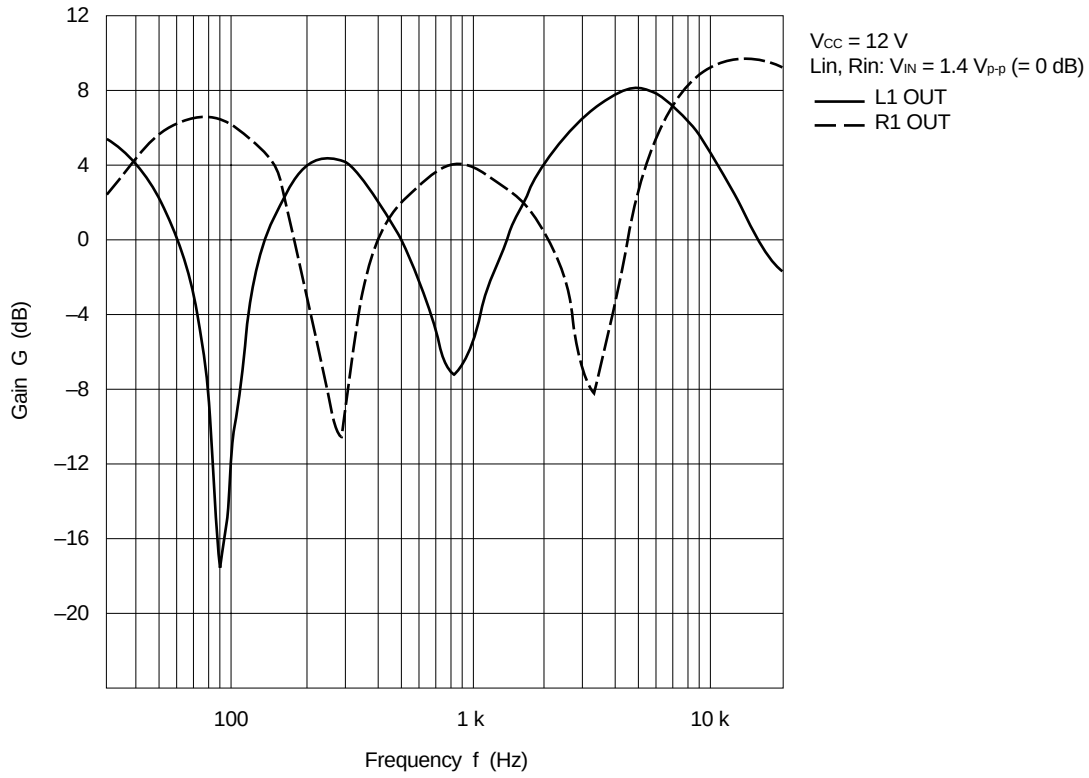
**(2) Movie Mode**




**(3) Music Mode**

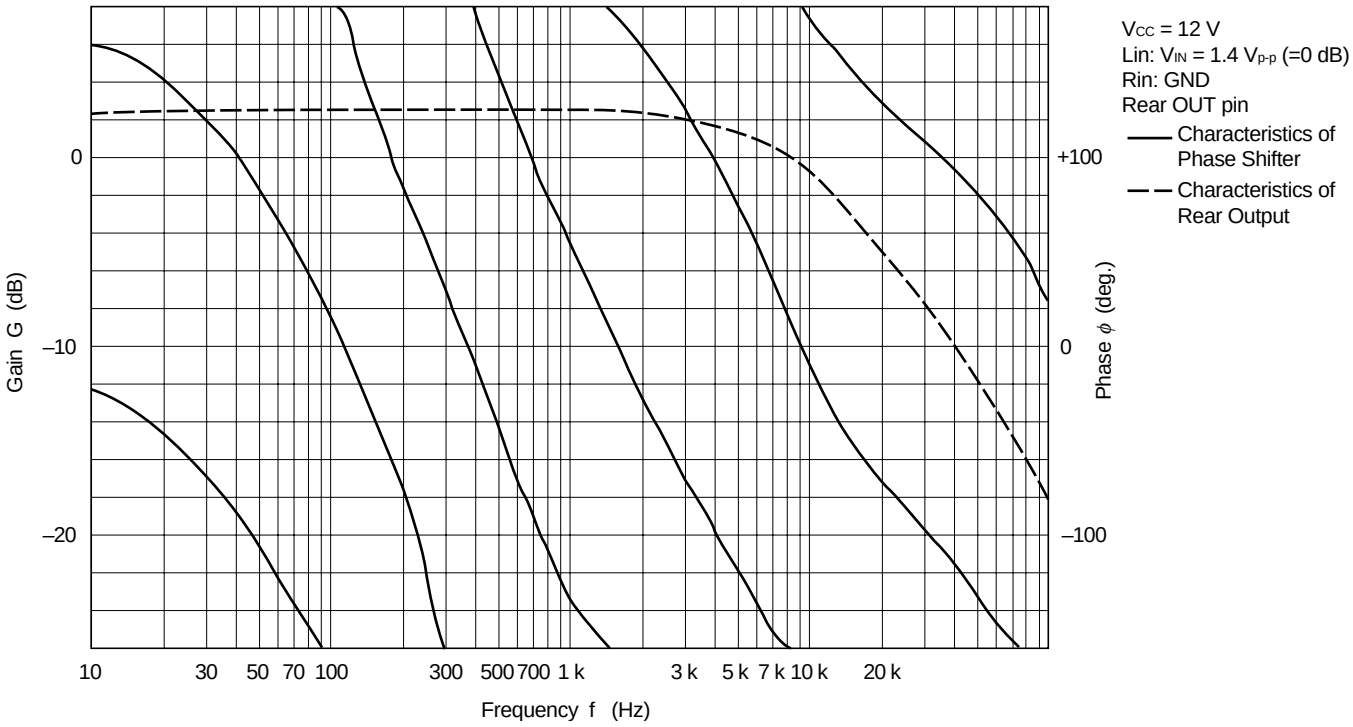


**(4) Simulated Mode**

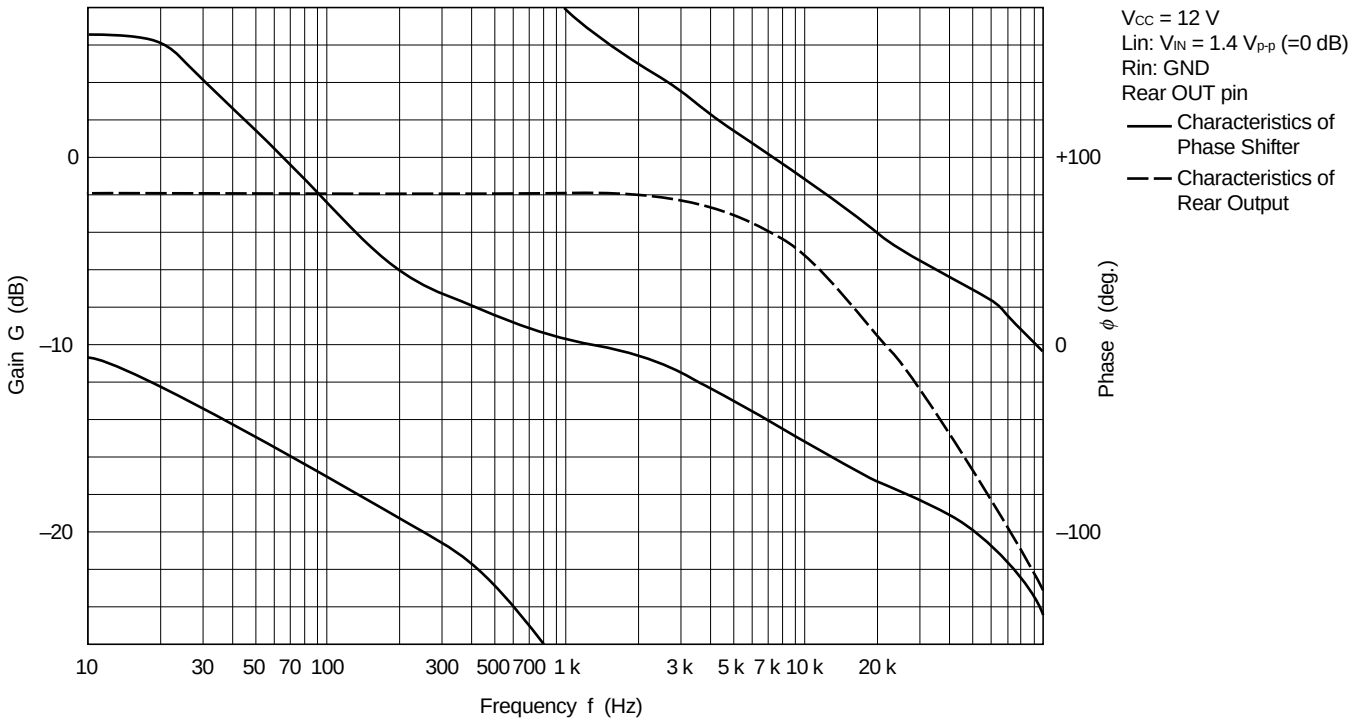


### 6.2 Characteristics of Phase Shifter and Rear Output

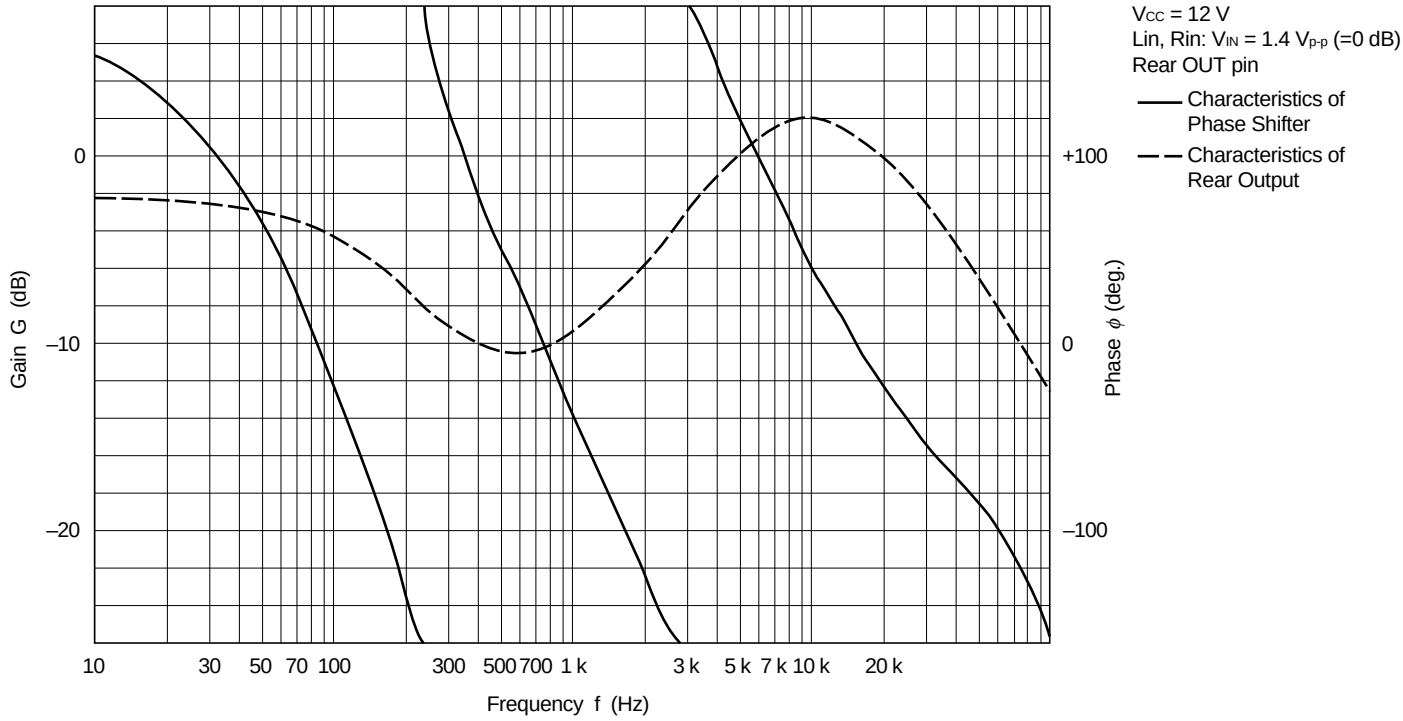
#### (1) Movie Mode




#### (2) Music Mode

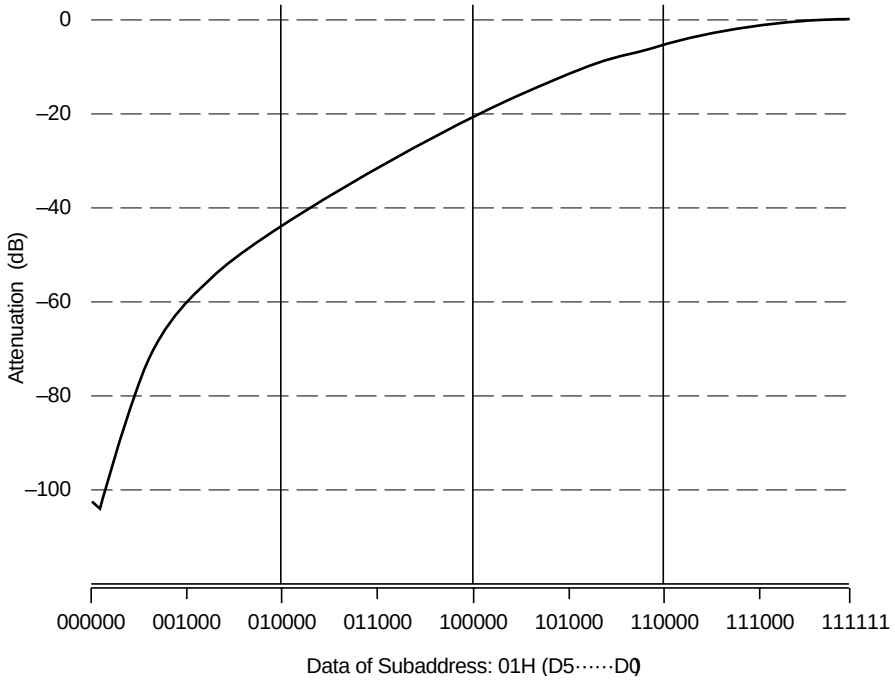


**(3) Simulated Mode**



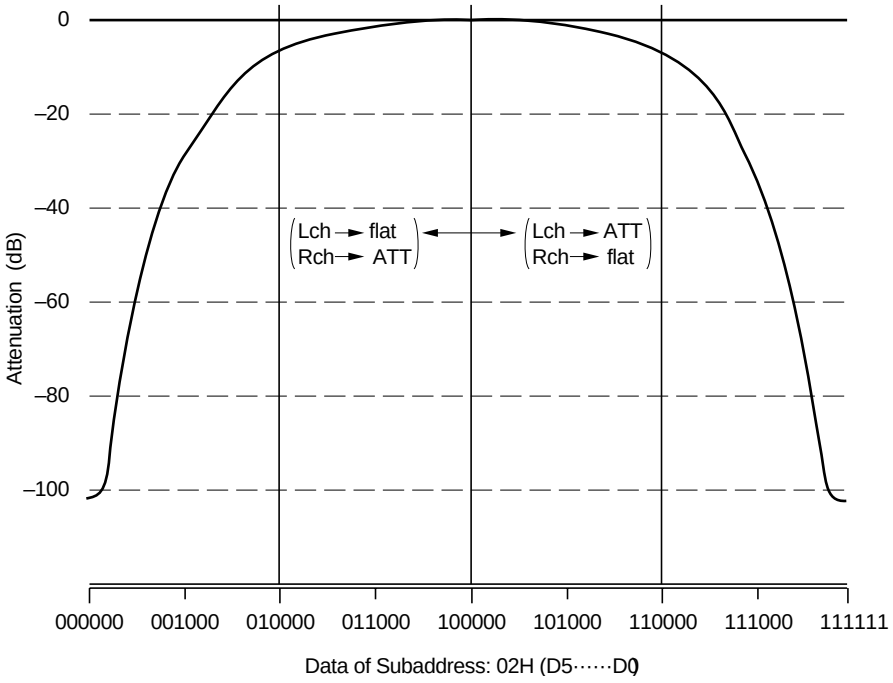
### 6.3 Control Characteristics

#### (1) Volume Control Characteristics



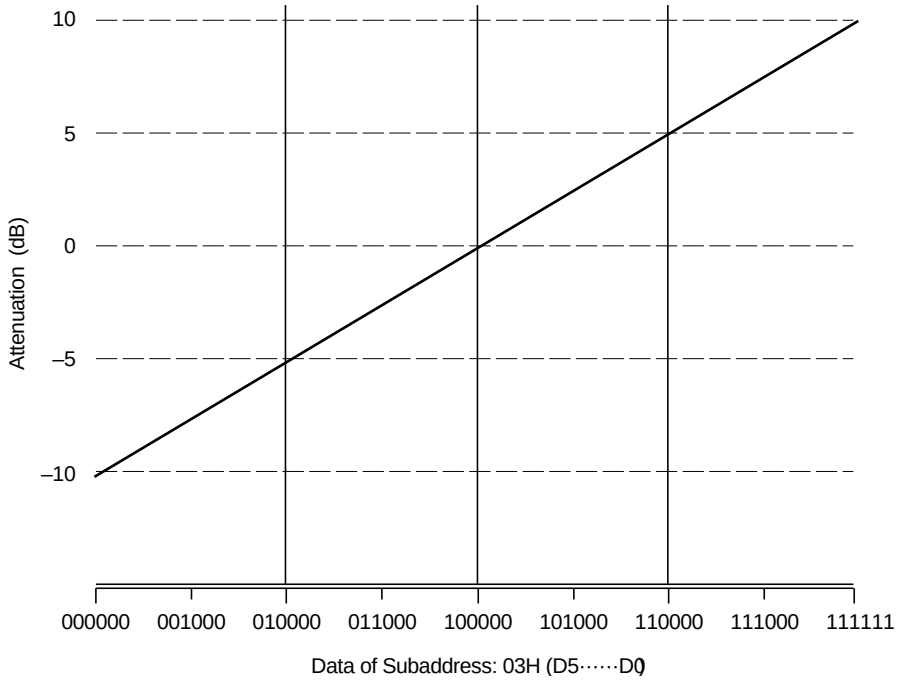

OFF mode
f = 1 kHz
Lin or Rin: $V_{IN}$ = 1.4 $V_{p-p}$ (=0 dB)
Lin or Rin: GND

#### (2) Balance Control Characteristics



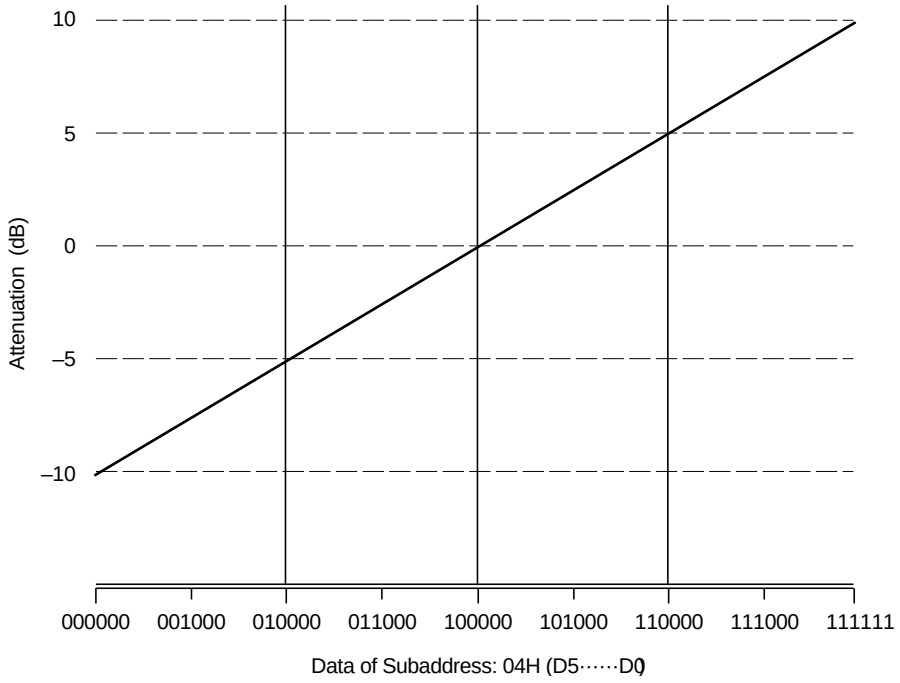

OFF mode
f = 1 kHz
L1 OUT
Lin: $V_{IN}$ = 1.4 $V_{p-p}$ (=0 dB)
Rin: GND
R1 OUT
Lin: GND
Rin: $V_{IN}$ = 1.4 $V_{p-p}$ (=0 dB)

### (3) Tone Control Characteristics (Bass)



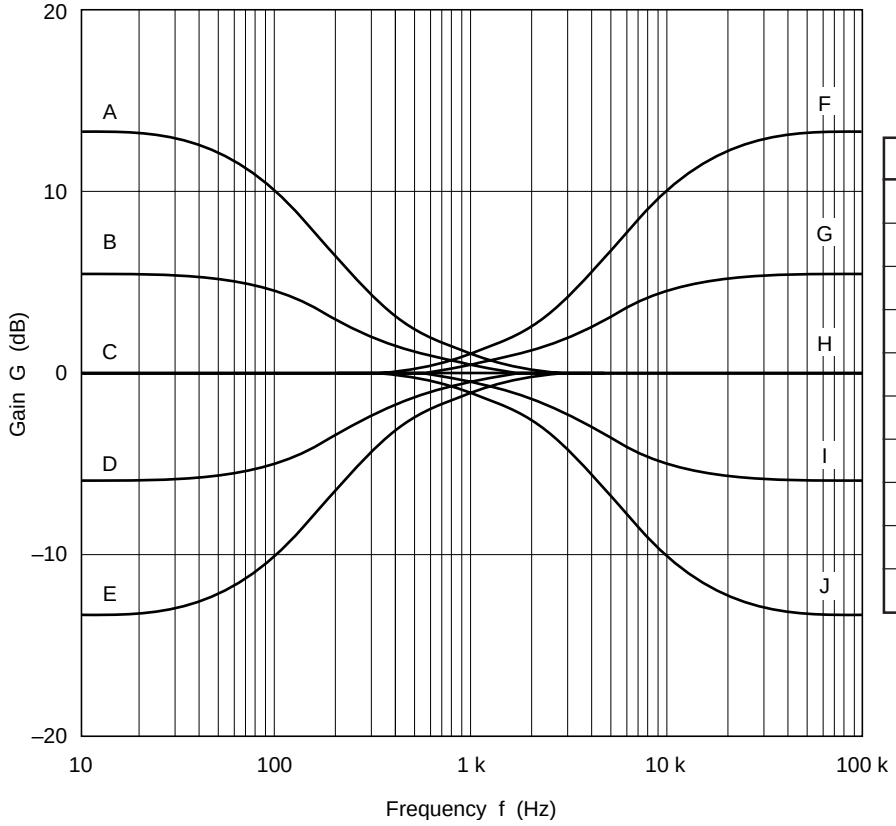

OFF mode
Bass: f = 100 Hz
Lin: $V_{IN}$ = 1.4 $V_{p-p}$ (=0 dB)
Rin: GND
L1 OUT

### (4) Tone Control Characteristics (Treble)




OFF mode
Treble: f = 10 kHz
Lin: $V_{IN}$ = 1.4 $V_{p-p}$ (=0 dB)
Rin: GND
L1 OUT

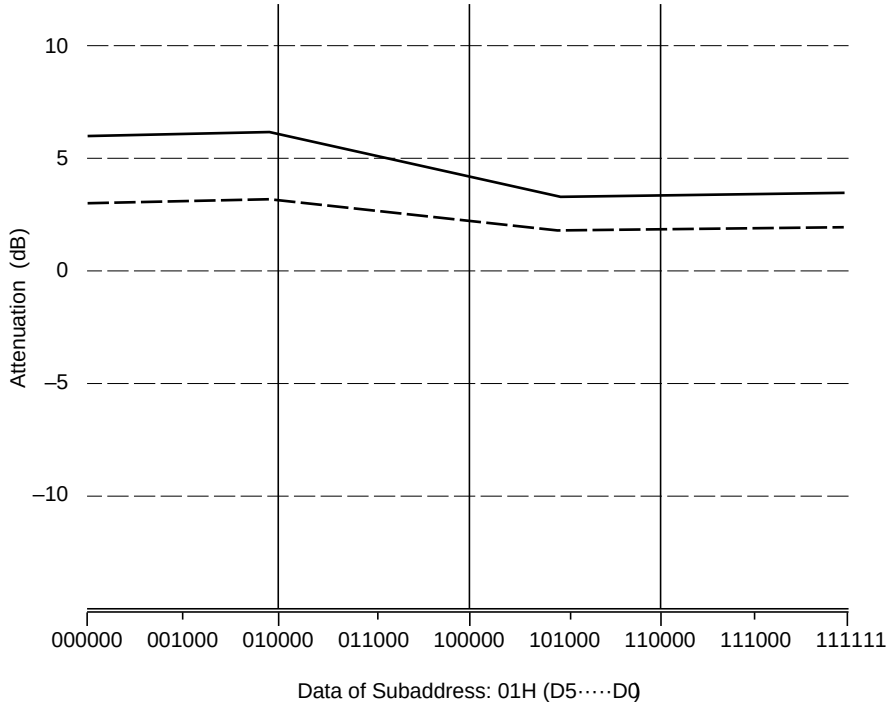
### (5) Tone Frequency Characteristics




OFF mode
Lin: $V_{IN}$ = 1.4 $V_{p-p}$ (=0 dB)
Rin: GND
L1 OUT

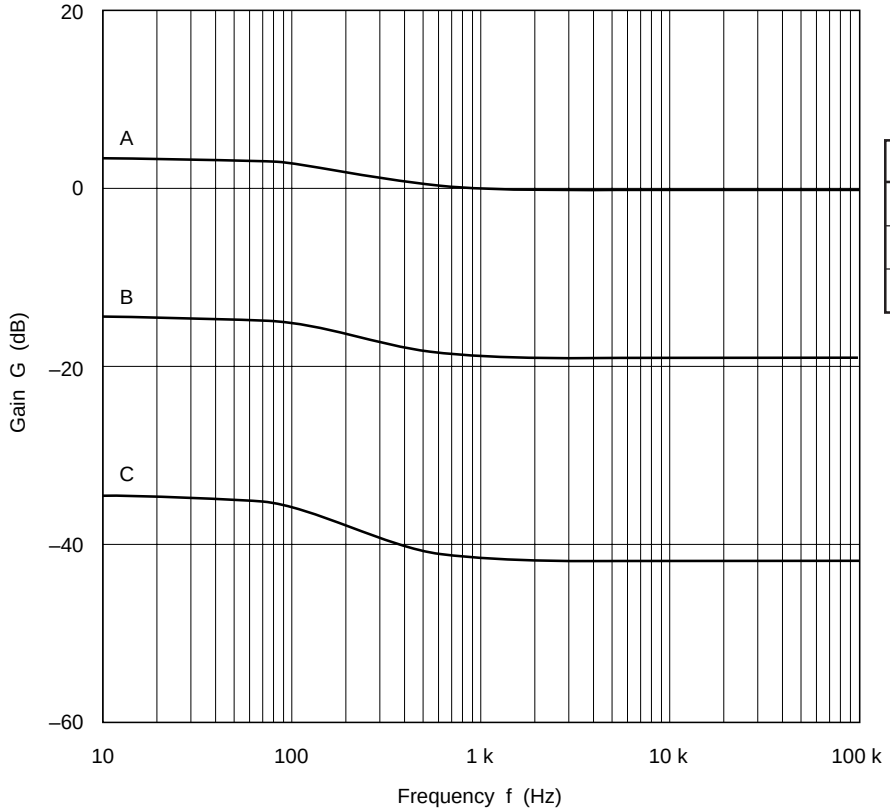
| Curve | Subaddress | Data (D5 ·····D0) |
|---|---|---|
| A | 03H | 111111 |
| B | | 110000 |
| C | | 100000 |
| D | | 010000 |
| E | | 000001 |
| F | 04H | 111111 |
| G | | 110000 |
| H | | 100000 |
| I | | 010000 |
| J | | 000001 |

### (6) Low Boost Control Characteristics




OFF mode
f = 100 Hz
Lin: $V_{IN}$ = 1.4 $V_{p-p}$ (= 0 dB)
Rin : GND
L1 OUT
—— Low Boost 1 (6 dB)
– – Low Boost 2 (3 dB)

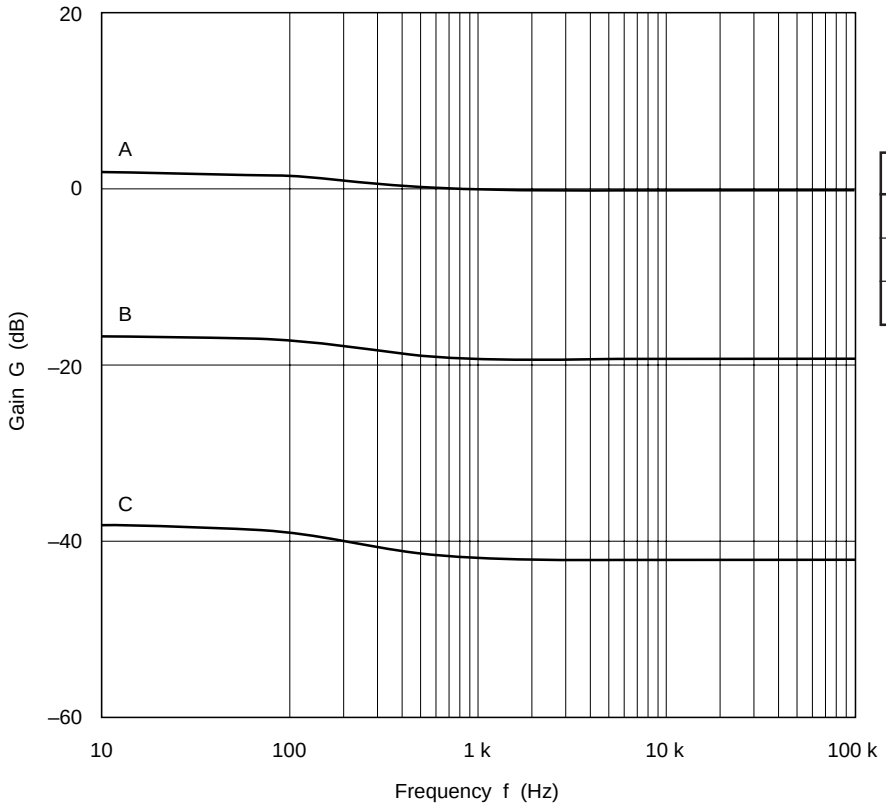
### (7) Low Boost 1 (6 dB)




$V_{CC}$ = 12 V
Lin: $V_{IN}$ = 1.4 $V_{p-p}$ (= 0 dB)
Rin: GND
L1 OUT

| Curve | Subaddress | Data (D5 ·····D0) |
|---|---|---|
| A | 01H | 111111 |
| B | | 100000 |
| C | | 010000 |

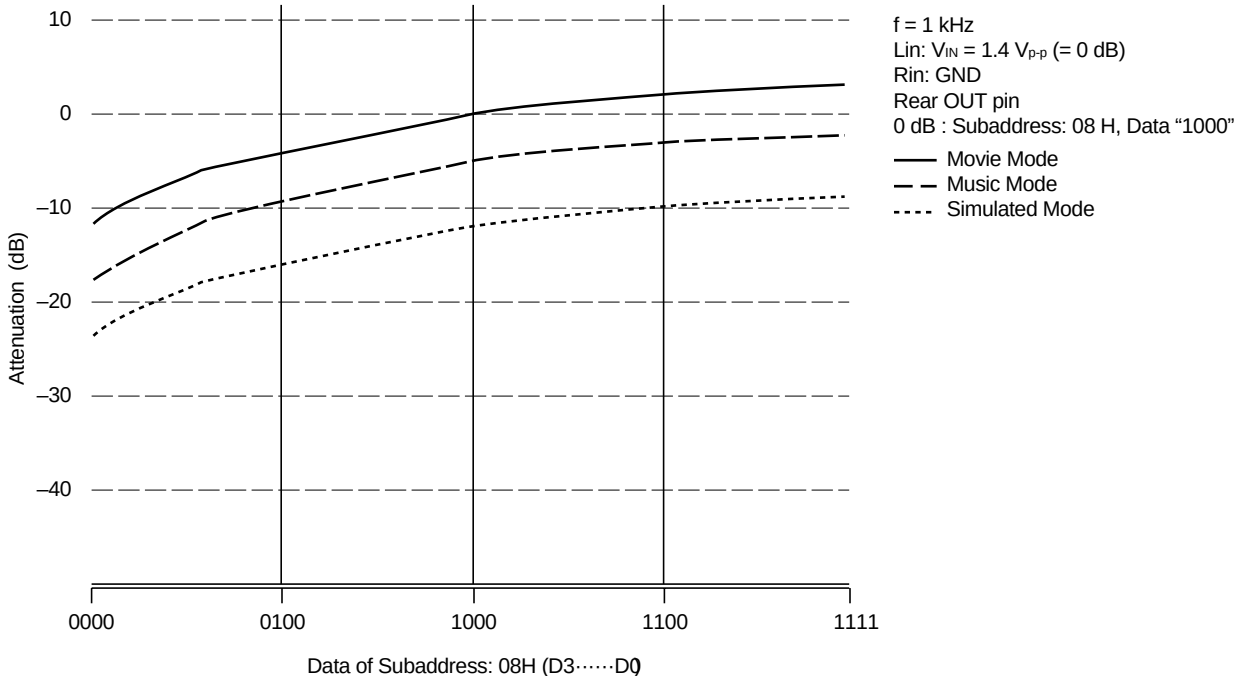
### (8) Low Boost 2 (3 dB)



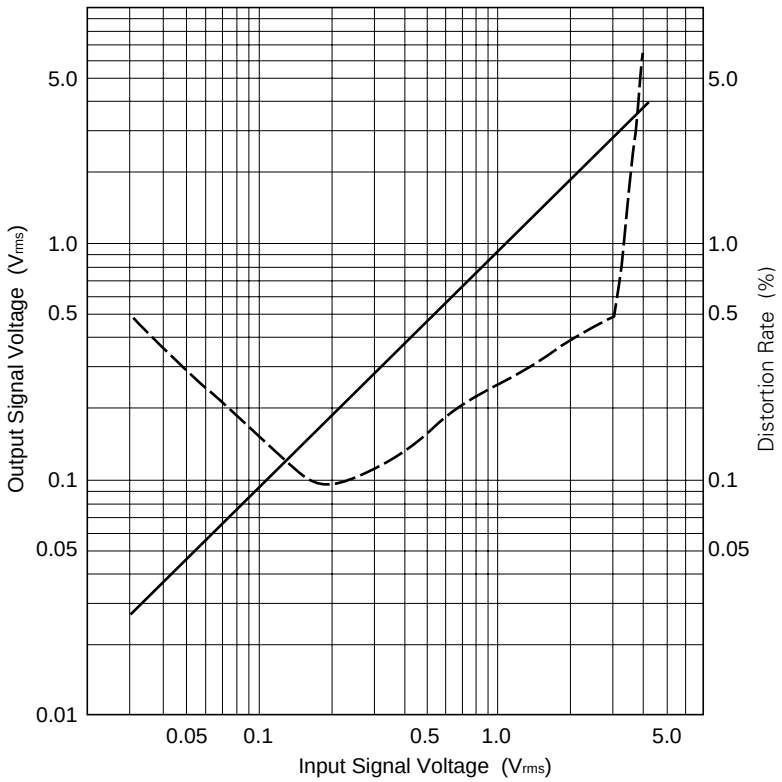

$V_{CC}$ = 12 V
Lin: $V_{IN}$ = 1.4 $V_{p-p}$ (= 0 dB)
Rin: GND
L1 OUT

| Curve | Subaddress | Data (D5 ·····D0) |
|---|---|---|
| A | 01H | 111111 |
| B | | 100000 |
| C | | 010000 |

**(9) Effect Control Characteristics**

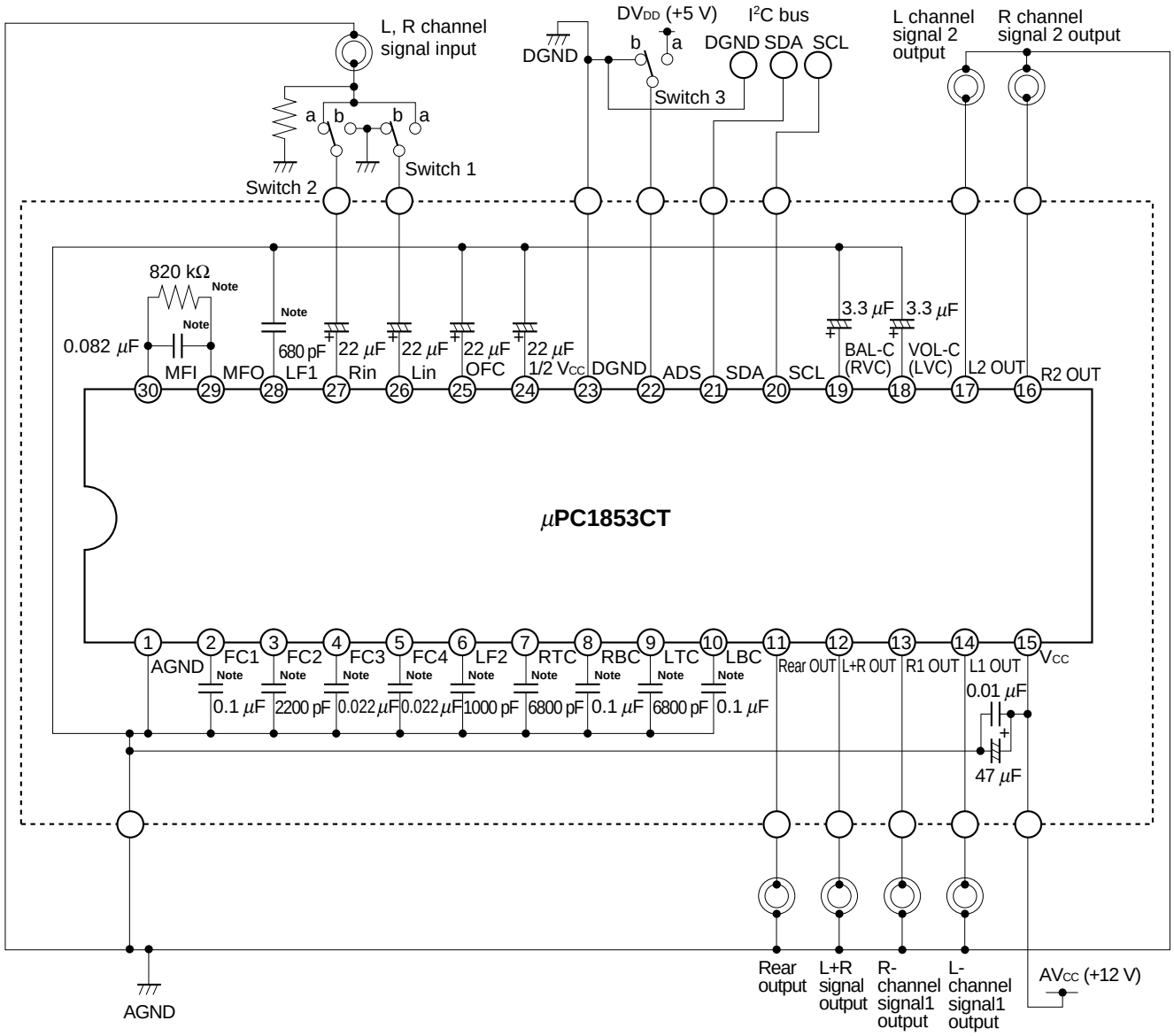


### 6.4 Input/Output Characteristics, Distortion Rate




f = 1 kHz
Lin or Rin: $V_{IN}$ = 1.4 $V_{p-p}$ (= 0 dB)
Lin or Rin: GND
μPC1853-01
Subaddress: 01H, Data "111111"
Subaddress: 02H, Data "100000"
μPC1853-02
Subaddress: 01H, 02H,
Data "111111"
—— Output Signal Voltage
— — Distortion Rate

## 7. MEASURING CIRCUIT




**Note** Recommended external parts.

Carbon-film resistor : ±1 %
Film capacitor : ±1 %
Ceramic capacitor : ±1 %

Use external parts as follows unless otherwise specified.

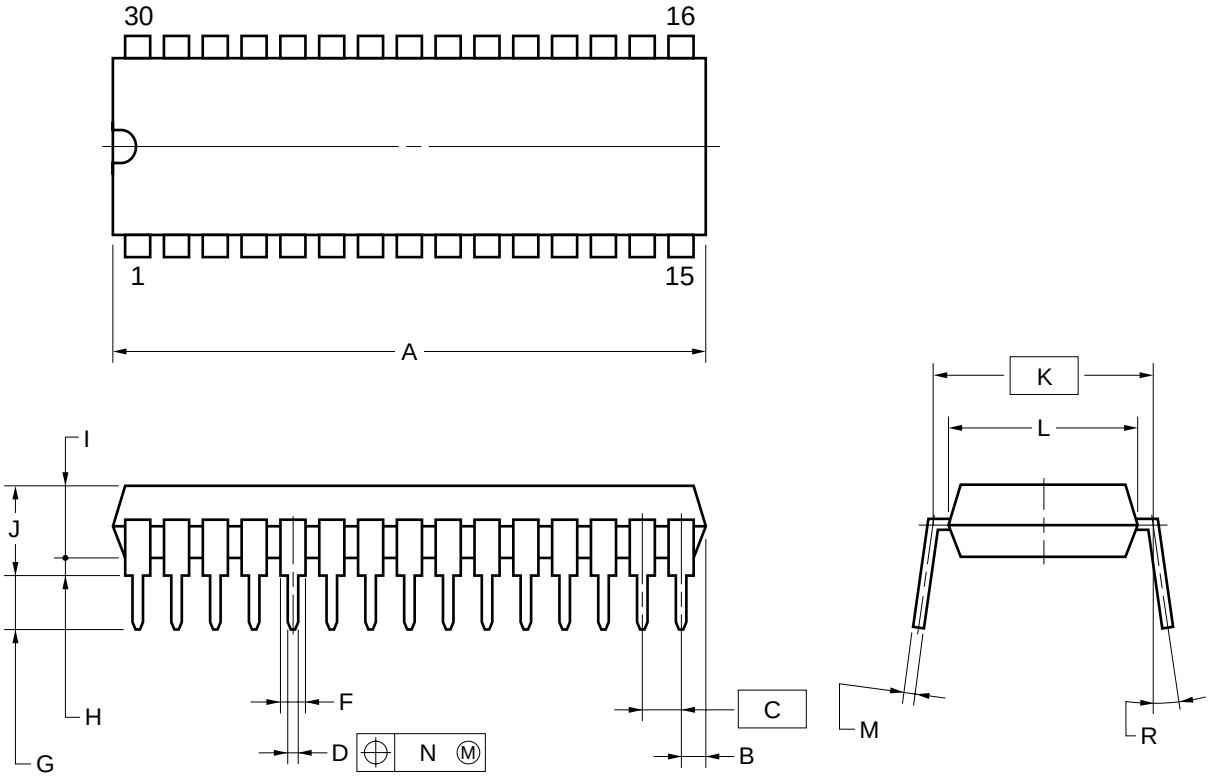
Carbon-film resistor : ±5 %
Film capacitor : ±20 %
Electrolytic capacitor : ±20 %

**Attention on Printed Wiring**

1. AGND: Wide area grounding.
2. Connect terminating resistors as near pins 26 and 27 as possible.
3. Make the wiring of $I^2C$ bus block distant from the wiring of analog block.
4. Connect by-pass capacitor near pin 15 ($V_{CC}$ pin).

## 8. PACKAGE DIMENSIONS

### 30PIN PLASTIC SHRINK DIP (400 mil)




**NOTES**

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

| ITEM | MILLIMETERS | INCHES |
|---|---|---|
| A | 28.46 MAX. | 1.121 MAX. |
| B | 1.78 MAX. | 0.070 MAX. |
| C | 1.778 (T.P.) | 0.070 (T.P.) |
| D | $0.50\pm0.10$ | $0.020^{+0.004}_{-0.005}$ |
| F | 0.85 MIN. | 0.033 MIN. |
| G | $3.2\pm0.3$ | $0.126\pm0.012$ |
| H | 0.51 MIN. | 0.020 MIN. |
| I | 4.31 MAX. | 0.170 MAX. |
| J | 5.08 MAX. | 0.200 MAX. |
| K | 10.16 (T.P.) | 0.400 (T.P.) |
| L | 8.6 | 0.339 |
| M | $0.25^{+0.10}_{-0.05}$ | $0.010^{+0.004}_{-0.003}$ |
| N | 0.17 | 0.007 |
| R | 0~15° | 0~15° |

**S30C-70-400B-1**

**[MEMO]**

**Caution: Purchase of NEC $I^2C$ components conveys a license under the Philips $I^2C$ Patent Rights to use these components in an $I^2C$ system, provided that the system conforms to the $I^2C$ Standard Specification as defined by Philips.**

The application circuits and their parameters are for references only and are not intended for use in actual design-in's.



M4 94.11