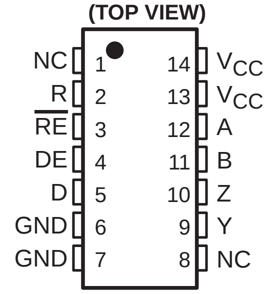
- **High-Speed Low-Power LinBICMOS™ Circuitry Designed for Signaling Rates† of up to 30 Mbps**
- **Bus-Pin ESD Protection Exceeds 12 kV HBM**
- **Very Low Disabled Supply-Current Requirements . . . 700 µA Maximum**
- **Designed for High-Speed Multipoint Data Transmission Over Long Cables**
- **Common-Mode Voltage Range of −7 V to 12 V**
- **Low Supply Current . . . 15 mA Max**
- **Compatible With ANSI Standard TIA/EIA-485-A and ISO 8482:1987(E)**
- **Positive and Negative Output Current Limiting**
- **Driver Thermal Shutdown Protection**

SN65LBC180AD (Marked as BL180A)
SN65LBC180AN (Marked as 65LBC180A)
SN75LBC180AD (Marked as LB180A)
SN75LBC180AN (Marked as 75LBC180A)
(TOP VIEW)



NC − No internal connection

Function Tables

DRIVER

INPUT D	ENABLE DE	OUTPUTS Y	OUTPUTS Z
H	H	H	L
L	H	L	H
X	L	Z	Z
Open	H	H	L

RECEIVER

DIFFERENTIAL INPUTS A − B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
$-0.2 \text{ V} < V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Open circuit	L	H

H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

description

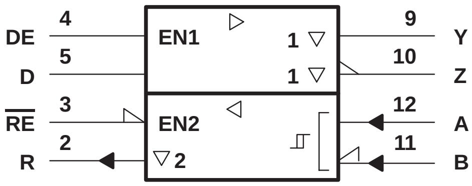
The SN65LBC180A and SN75LBC180A differential driver and receiver pairs are monolithic integrated circuits designed for bidirectional data communication over long cables that take on the characteristics of transmission lines. They are balanced, or differential, voltage mode devices that are compatible with ANSI standard TIA/EIA-485-A and ISO 8482:1987(E). The A version offers improved switching performance over its predecessors without sacrificing significantly more power.

These devices combine a differential line driver and differential input line receiver and operate from a single 5-V power supply. The driver differential outputs and the receiver differential inputs are connected to separate terminals for full-duplex operation and are designed to present minimum loading to the bus when powered off (V_{CC} = 0). These parts feature wide positive and negative common-mode voltage ranges, making them suitable for point-to-point or multipoint data bus applications. The devices also provide positive and negative current limiting for protection from line fault conditions. The SN65LBC180A is characterized for operation from −40°C to 85°C, and the SN75LBC180A is characterized for operation from 0°C to 70°C.

† Signaling rate by TIA/EIA-485-A definition restrict transition times to 30% of the bit duration, and much higher signaling rates may be achieved without this requirement as displayed in the *TYPICAL CHARACTERISTICS* of this device.

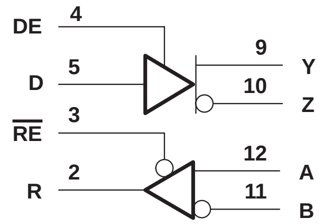
LinBiCMOS is a trademark of Texas Instruments.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



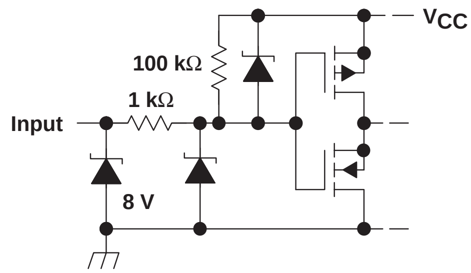
AVAILABLE OPTIONS

T_A	PACKAGE	
	SMALL OUTLINE† (D)	PLASTIC DUAL-IN-LINE (N)
0°C to 70°C	SN75LBC180AD	SN75LBC180AN
−40°C to 85°C	SN65LBC180AD	SN65LBC180AN

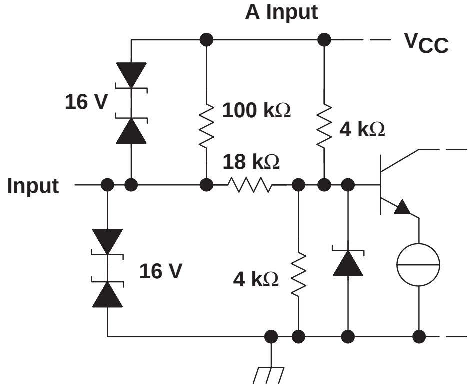
† The D package is available taped and reeled. Add an R suffix to the part number (i.e., SN65LBC180ADR).

schematics of inputs and outputs

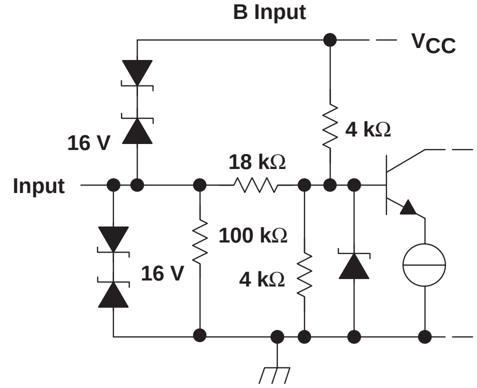
D, DE, and $\overline{RE}$ Inputs



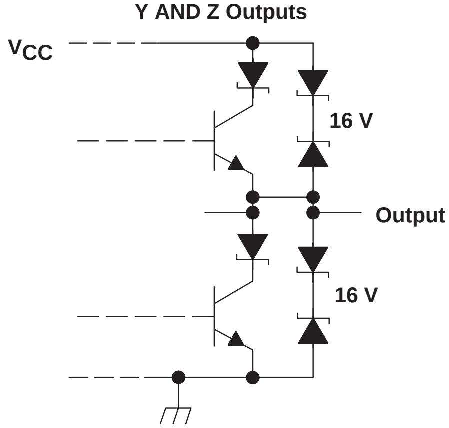
A Input



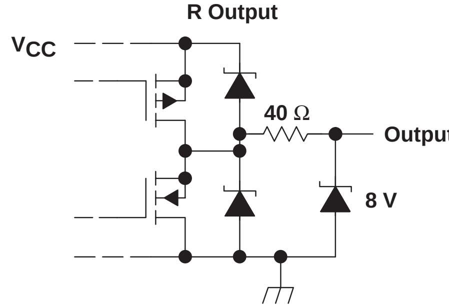
B Input



Y AND Z Outputs



R Output



absolute maximum ratings†

Supply voltage range, V_{CC} (see Note 1)	−0.3 V to 6 V
Input voltage range, V_I (A, B)	−10 V to 15 V
Voltage range at D, R, DE, $\overline{RE}$	−0.3 V to V_{CC} + 0.5 V
Continuous total power dissipation (see Note 2)	Internally limited
Total power dissipation	See Dissipation Rating Table
Electrostatic discharge: Bus terminals and GND, Class 3, A: (see Note 3)	12 kV
Bus terminals and GND, Class 3, B: (see Note 3)	400 V
All terminals, Class 3, A:	3 kV
All terminals, Class 3, B:	400 V
Storage temperature range, T_{stg}	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND except for differential input or output voltages.
2. The maximum operating junction temperature is internally limited. Use the dissipation rating table to operate below this temperature.
3. Tested in accordance with MIL−STD−883C, Method 3015.7

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR‡ ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

‡ This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}	D, DE, and $\overline{RE}$	2		V_{CC}	V
Low-level input voltage, V_{IL}	D, DE, and $\overline{RE}$	0		0.8	V
Differential input voltage, V_{ID} (see Note 4)		−12§		12	V
Voltage at any bus terminal (separately or common mode), V_O, V_I, or V_{IC}	A, B, Y, or Z	−7		12	V
High-level output current, I_{OH}	Y or Z	−60			mA
	R	−8			
Low-level output current, I_{OL}	Y or Z			60	mA
	R			8	
Operating free-air temperature, T_A	SN65LBC180A	−40		85	°C
	SN75LBC180A	0		70	

§ The algebraic convention where the least positive (more negative) limit is designated minimum, is used in this data sheet.

NOTE 4: Differential input/output bus voltage is measured at the noninverting terminal with respect to the inverting terminal.

driver electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18$ mA		−1.5	−0.8		V
$\lvert V_{OD} \rvert$	Differential output voltage magnitude	$R_L = 54\ \Omega$,, See Figure 1	SN65LBC180A	1	1.5	3	V
			SN75LBC180A	1.1	1.5	3	
		$R_L = 60\ \Omega$,, See Figure 2	SN65LBC180A	1	1.5	3	
			SN75LBC180A	1.1	1.5	3	
$\Delta\lvert V_{OD} \rvert$	Change in magnitude of differential output voltage (see Note 5)	See Figures 1 and 2		−0.2		0.2	V
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 1		1.8	2.4	2.8	V
ΔV_{OC}	Change in steady-state common-mode output voltage (see Note 5)			−0.1		0.1	V
I_O	Output current with power off	$V_{CC} = 0$,	$V_O = -7$ V to 12 V	−10		10	µA
I_{IH}	High-level input current	$V_I = 2$ V		−100			µA
I_{IL}	Low-level input current	$V_I = 0.8$ V		−100			µA
I_{OS}	Short-circuit output current	$-7\ V \le V_O \le 12$ V		−250	±70	250	mA
I_{CC}	Supply current	$V_I = 0$ or V_{CC}, No load	Receiver disabled and driver enabled		5.5	9	mA
			Receiver disabled and driver disabled		0.5	1	
			Receiver enabled and driver enabled		8.5	15	

† All typical values are at $V_{CC} = 5$ V and $T_A = 25°C$.

NOTE 5: $\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in the steady-state magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

driver switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	$R_L = 54\ \Omega$, $C_L = 50$ pF, See Figure 3	2	6	12	ns
t_{PHL}	Propagation delay time, high-to-low-level output		2	6	12	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{PLH} - t_{PHL}\rvert$)			0.3	1	ns
t_r	Differential output signal rise time		4	7.5	11	ns
t_f	Differential output signal fall time		4	7.5	11	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	$R_L = 110\ \Omega$, See Figure 4		12	22	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output	$R_L = 110\ \Omega$, See Figure 5		12	22	ns
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output	$R_L = 110\ \Omega$, See Figure 4		12	22	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output	$R_L = 110\ \Omega$, See Figure 5		12	22	ns

receiver electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	$I_O = -8$ mA				0.2	V
V_{IT-}	Negative-going input threshold voltage	$I_O = 8$ mA		−0.2			V
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)				50		mV
V_{IK}	Enable-input clamp voltage	$I_I = -18$ mA		−1.5	−0.8		V
V_{OH}	High-level output voltage	$V_{ID} = 200$ mV, $I_{OH} = -8$ mA		4	4.9		V
V_{OL}	Low-level output voltage	$V_{ID} = -200$ mV, $I_{OL} = 8$ mA			0.1	0.8	V
I_{OZ}	High-impedance-state output current	$V_O = 0$ V to V_{CC}		−1		1	μA
I_{IH}	High-level enable-input current	$V_{IH} = 2.4$ V		−100			μA
I_{IL}	Low-level enable-input current	$V_{IL} = 0.4$ V		−100			μA
I_I	Bus input current	$V_I = 12$ V, $V_{CC} = 5$ V	Other input at 0 V		0.4	1	mA
		$V_I = 12$ V, $V_{CC} = 0$ V			0.5	1	
		$V_I = -7$ V, $V_{CC} = 5$ V		−0.8	−0.4		
		$V_I = -7$ V, $V_{CC} = 0$ V		−0.8	−0.3		
I_{CC}	Supply current	$V_I = 0$ or V_{CC}, No load	Receiver enabled and driver disabled		4.5	7.5	mA
			Receiver disabled and driver disabled		0.5	1	
			Receiver enabled and driver enabled		8.5	15	

† All typical values are at $V_{CC} = 5$ V and $T_A = 25°C$.

receiver switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	$V_{ID} = -1.5$ V to 1.5 V, See Figure 7	7	13	20	ns
t_{PHL}	Propagation delay time, high- to low-level output		7	13	20	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)			0.5	1.5	ns
t_r	Output signal rise time	See Figure 7		2.1	3.3	ns
t_f	Output signal fall time			2.1	3.3	ns
t_{PZH}	Output enable time to high level	$C_L = 10$ pF, See Figure 8		30	45	ns
t_{PZL}	Output enable time to low level			30	45	ns
t_{PHZ}	Output disable time from high level			20	40	ns
t_{PLZ}	Output disable time from low level			20	40	ns

PARAMETER MEASUREMENT INFORMATION

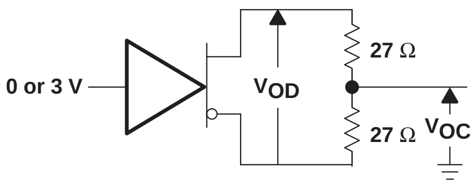


Figure 1. Driver V_{OD} and V_{OC}

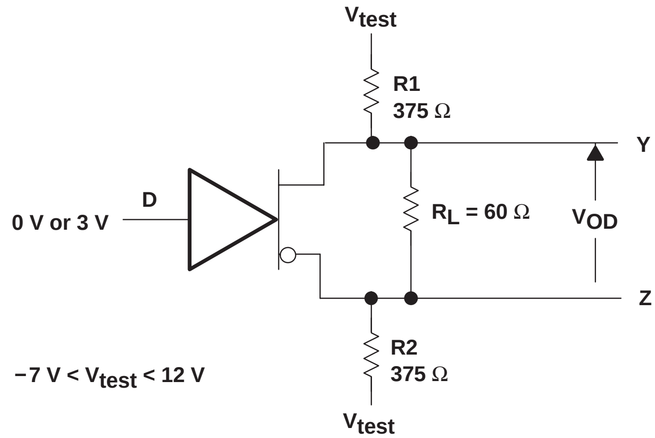
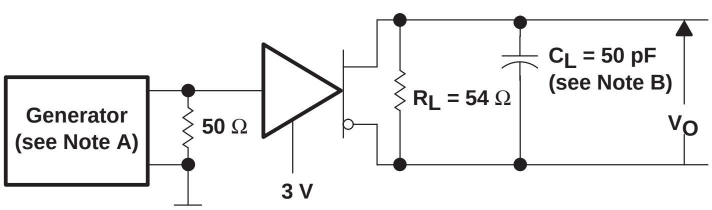
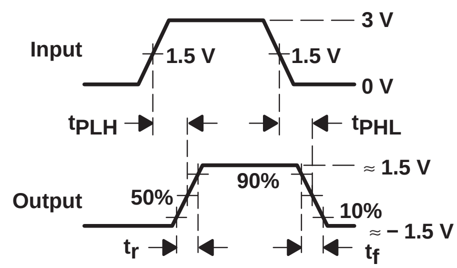


Figure 2. Driver V_{OD}



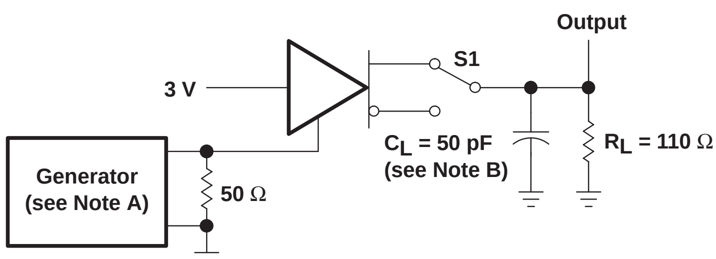
TEST CIRCUIT



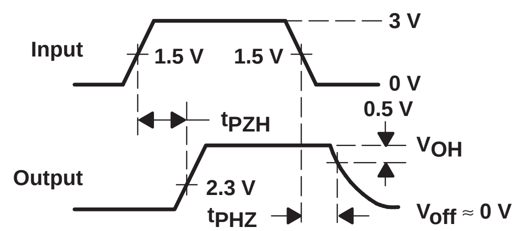
VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

Figure 3. Driver Test Circuit and Voltage Waveforms



TEST CIRCUIT

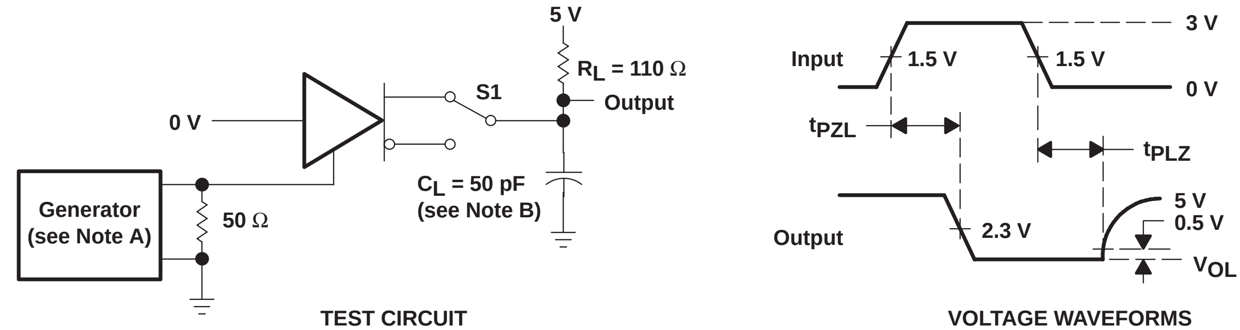


VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

Figure 4. Driver Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 5. Driver Test Circuit and Voltage Waveforms

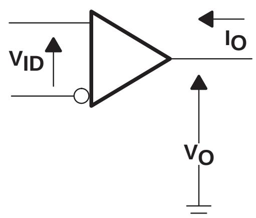
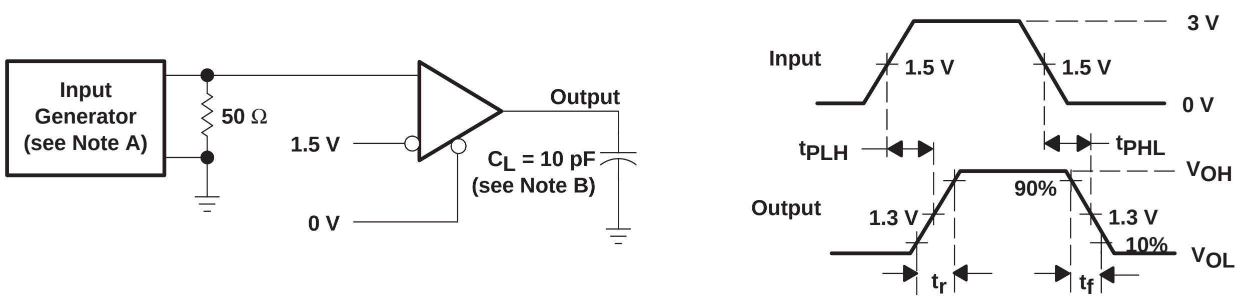


Figure 6. Receiver V_{OH} and V_{OL}



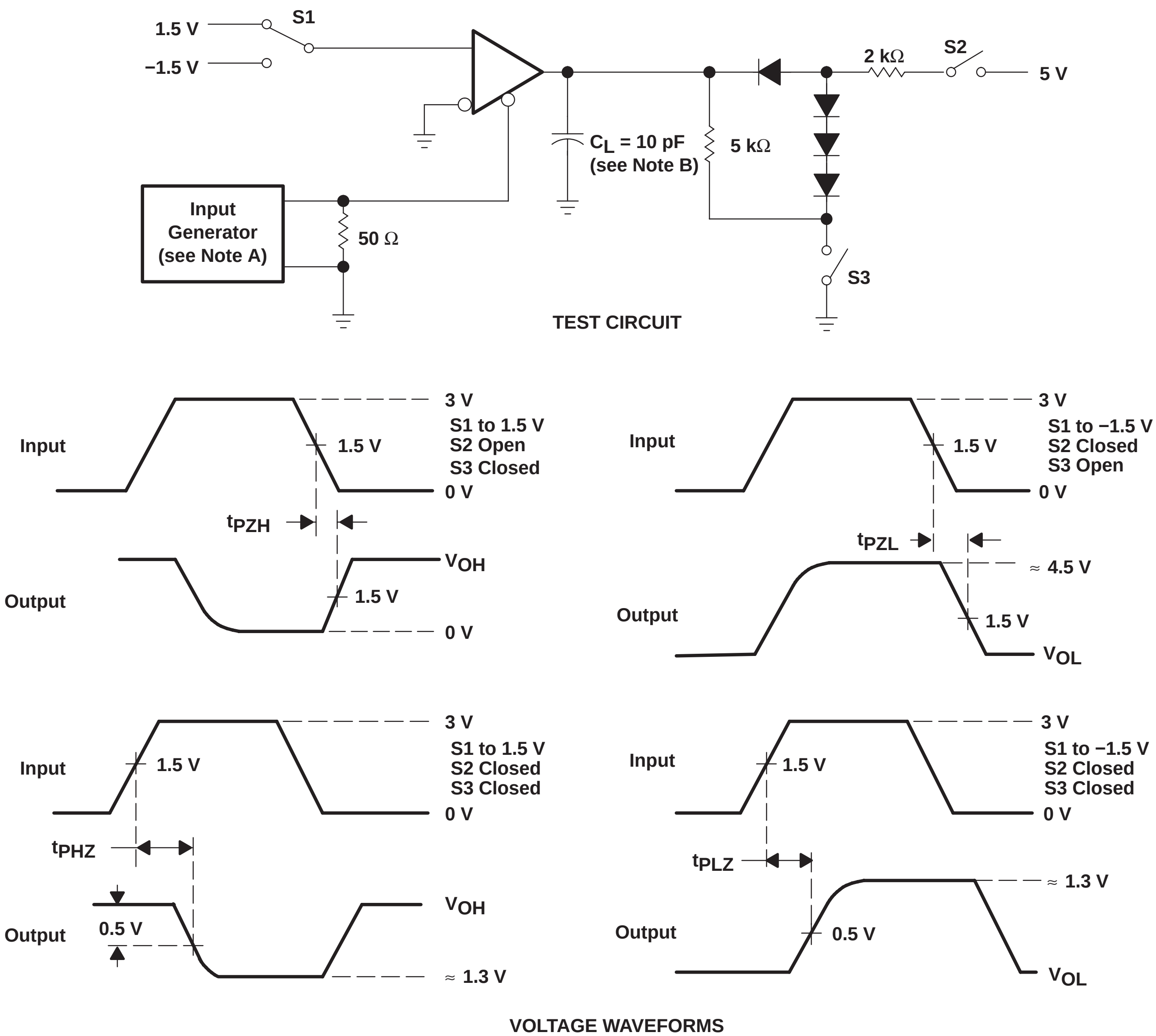
TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 7. Receiver Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

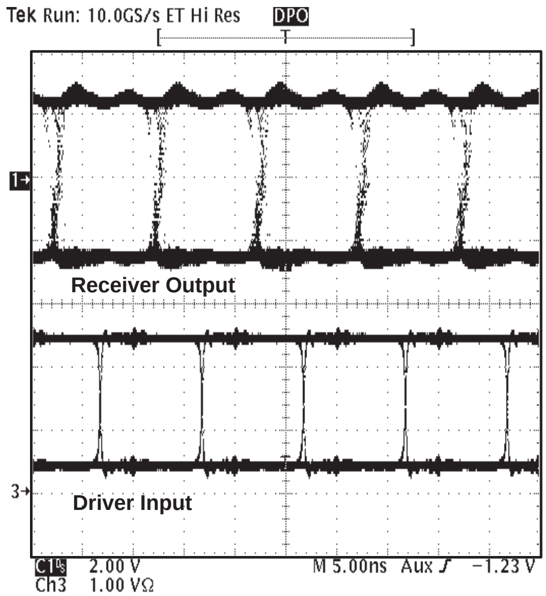


NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, $t_r \le 6$ ns, $t_f \le 6$ ns, $Z_O = 50\ \Omega$.

B. C_L includes probe and jig capacitance.

Figure 8. Receiver Output Enable and Disable Times

TYPICAL CHARACTERISTICS



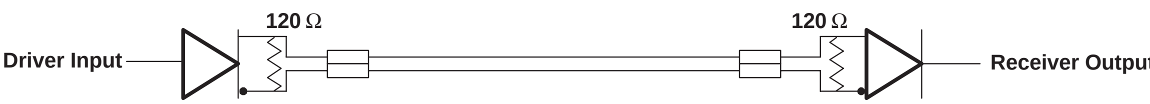


Figure 9. Typical Waveform of Nonreturn-to-Zero (NRZ), Pseudorandom Binary Sequence (PRBS) Data at 100 Mbps Through 15m, of CAT 5 Unshielded Twisted Pair (UTP) Cable

TIA/EIA-485-A defines a maximum signaling rate as that in which the transition time of the voltage transition of a logic-state change remains less than or equal to 30% of the bit length. Transition times of greater length perform quite well even though they do not meet the standard by definition.

TYPICAL CHARACTERISTICS

AVERAGE SUPPLY CURRENT vs FREQUENCY

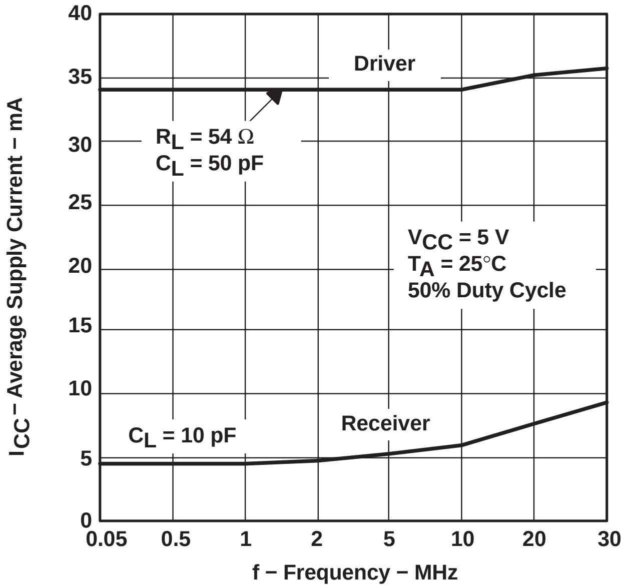


Figure 10

LOGIC INPUT CURRENT vs INPUT VOLTAGE

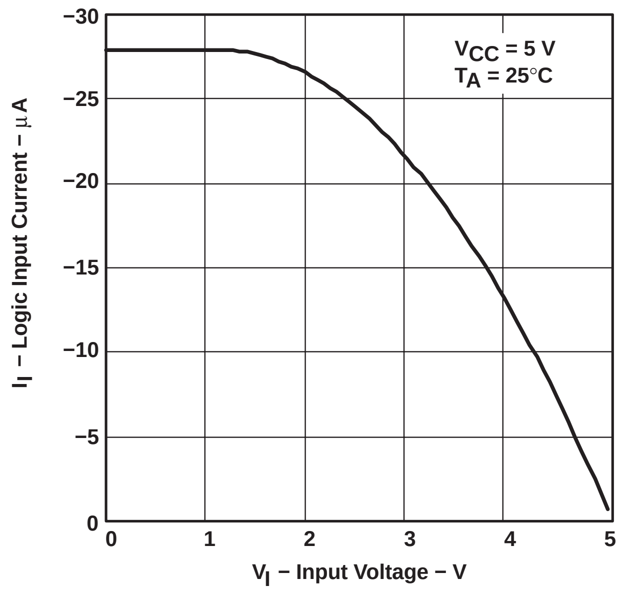


Figure 11

BUS INPUT CURRENT vs INPUT VOLTAGE

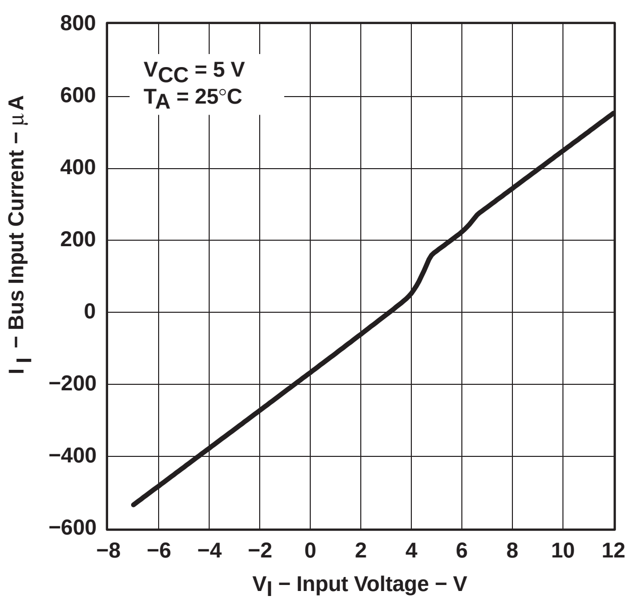


Figure 12

DRIVER LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

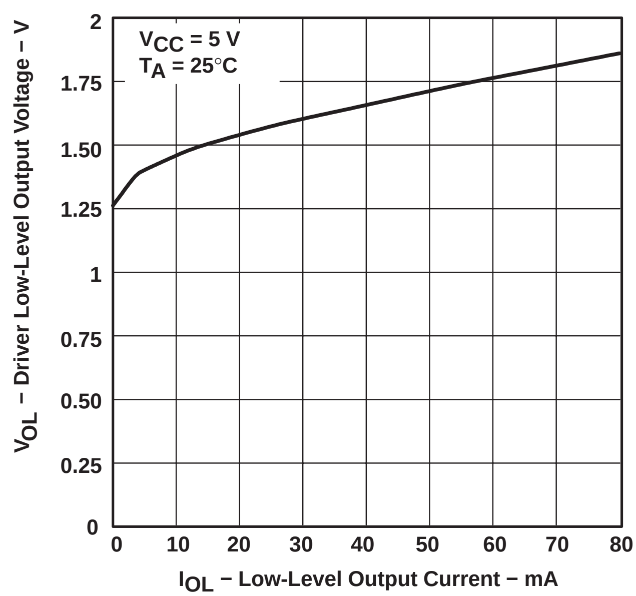


Figure 13

TYPICAL CHARACTERISTICS

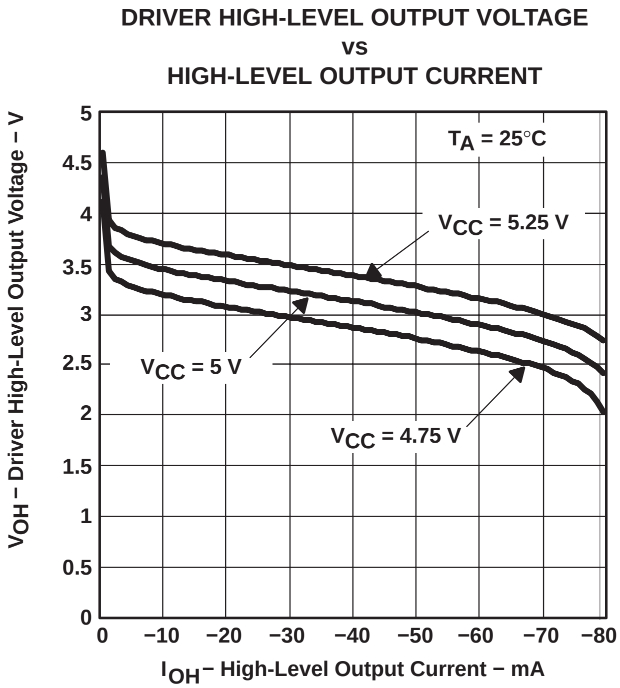


Figure 14

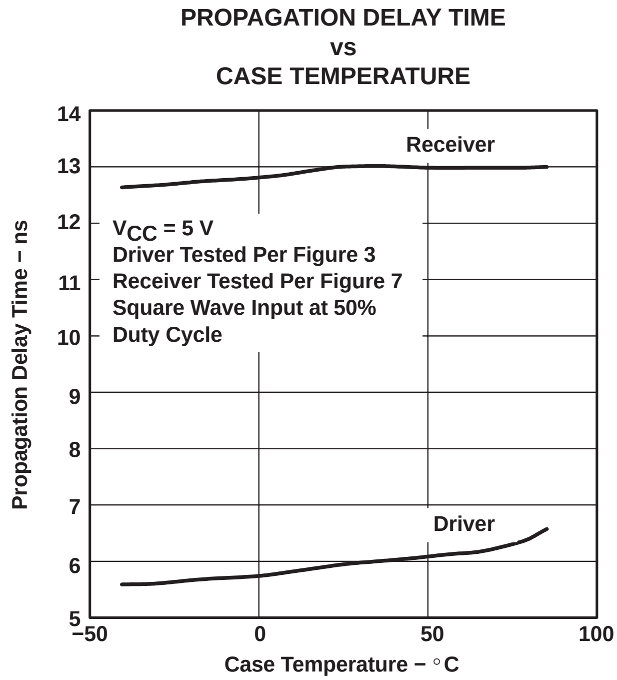
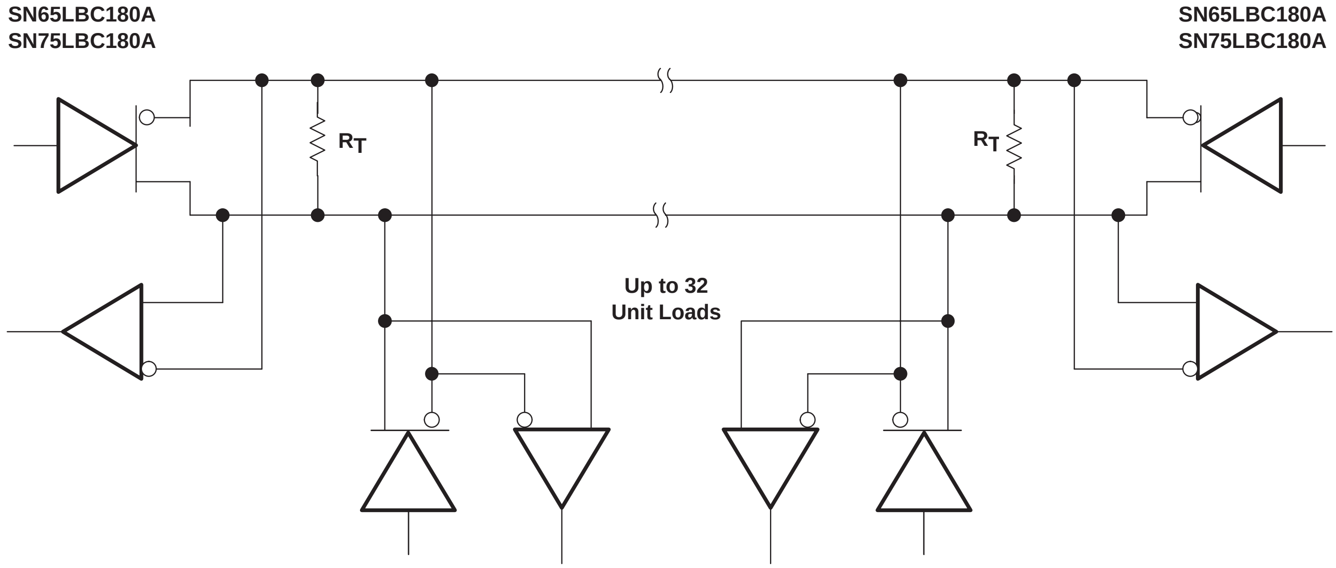


Figure 15

APPLICATION INFORMATION



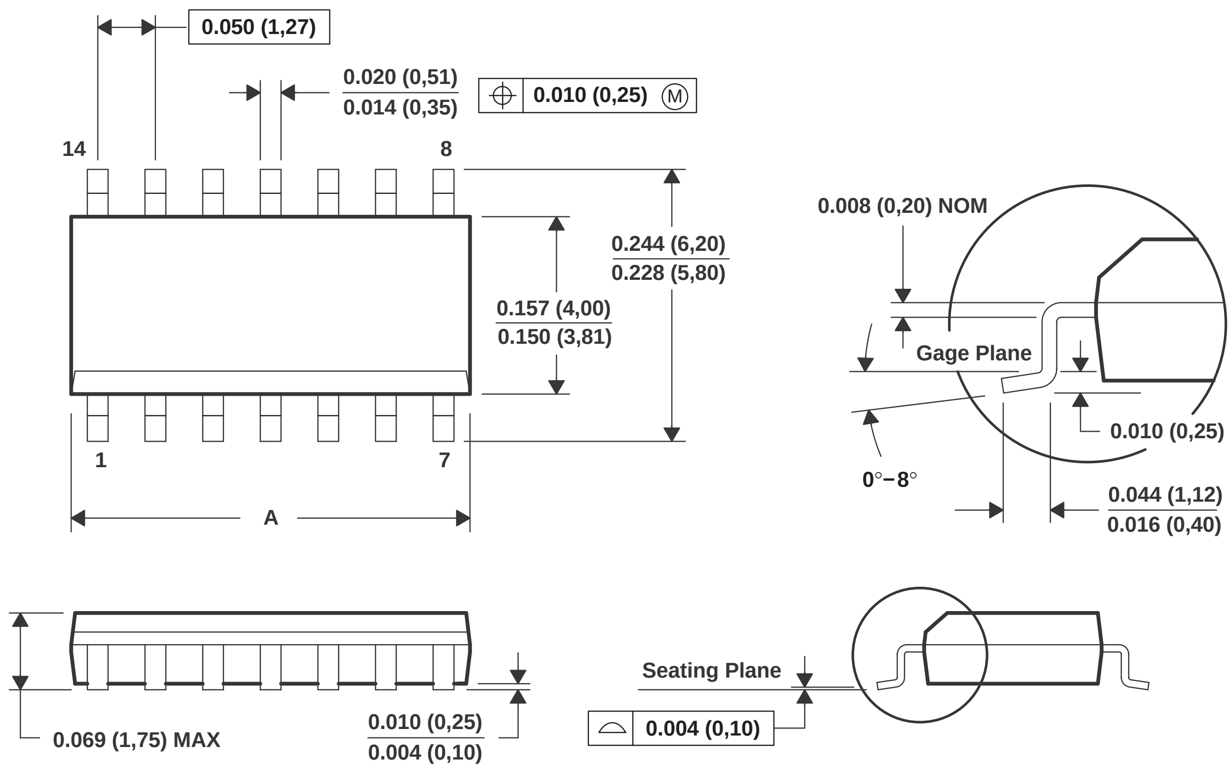
NOTE A: The line should be terminated at both ends in its characteristic impedance ($R_T = Z_O$). Stub lengths off the main line should be kept as short as possible. One SN65LBC180A typically represents less than one unit load.

Figure 16. Typical Application Circuit

MECHANICAL DATA

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



PINS ** / DIM	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047 / D 10/96

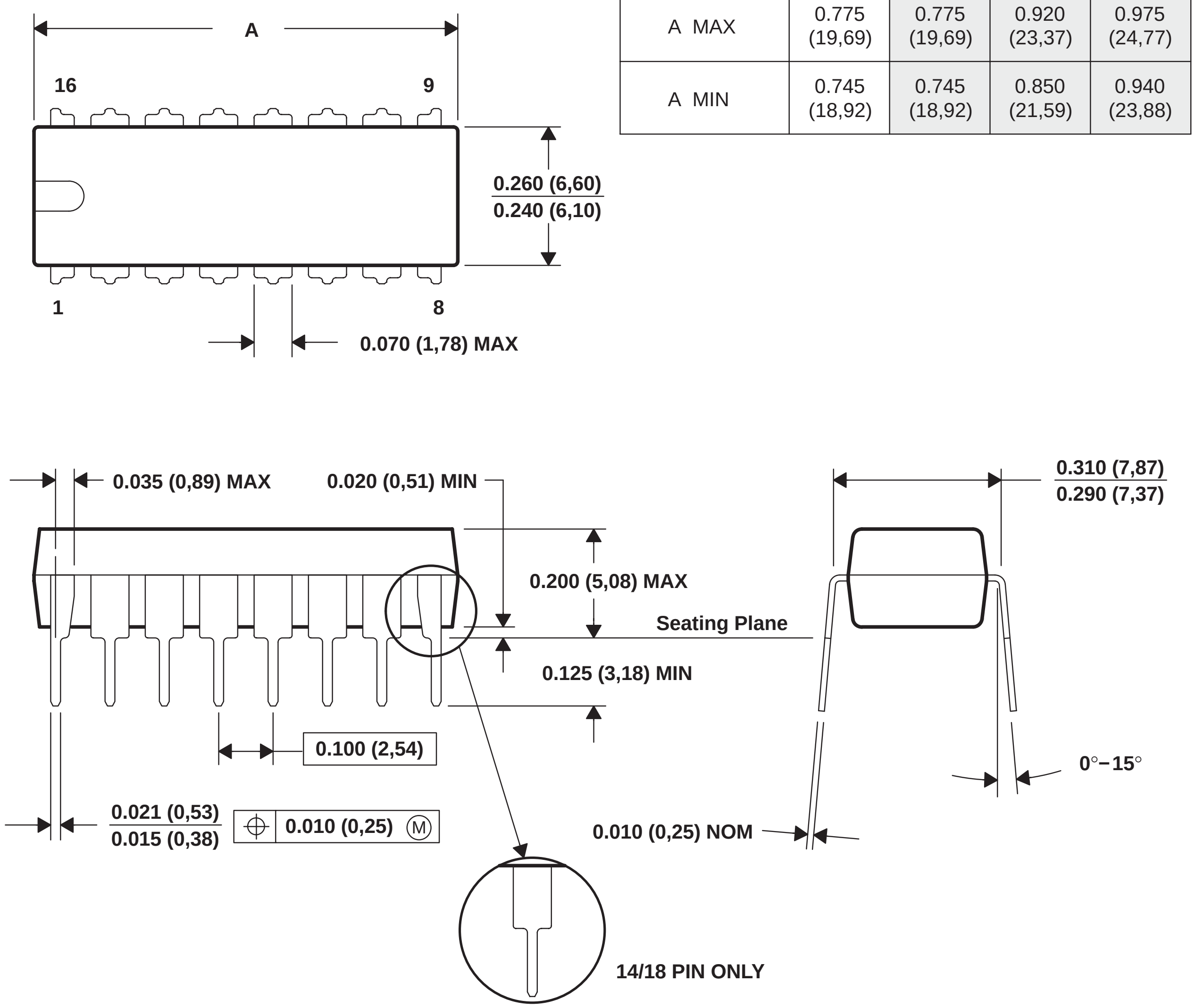
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

MECHANICAL DATA

N (R-PDIP-T)** **PLASTIC DUAL-IN-LINE PACKAGE**

16 PINS SHOWN

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	0.975 (24,77)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 (20-pin package is shorter than MS-001).

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN65LBC180AD	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
SN65LBC180ADR	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
SN65LBC180AN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN75LBC180AD	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
SN75LBC180ADR	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
SN75LBC180AN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
None: Not yet available Lead (Pb-Free).
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

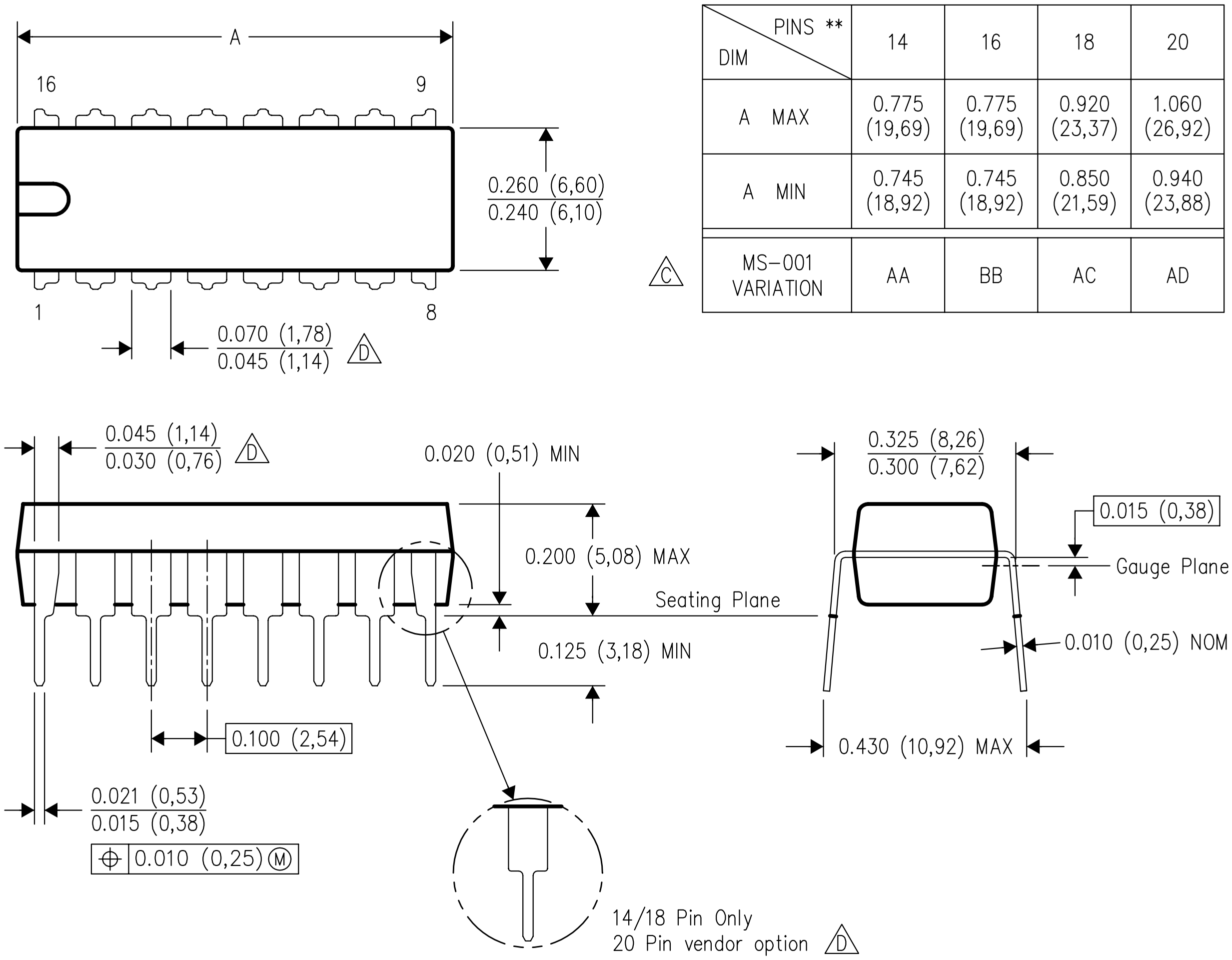
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

N (R-PDIP-T**) PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

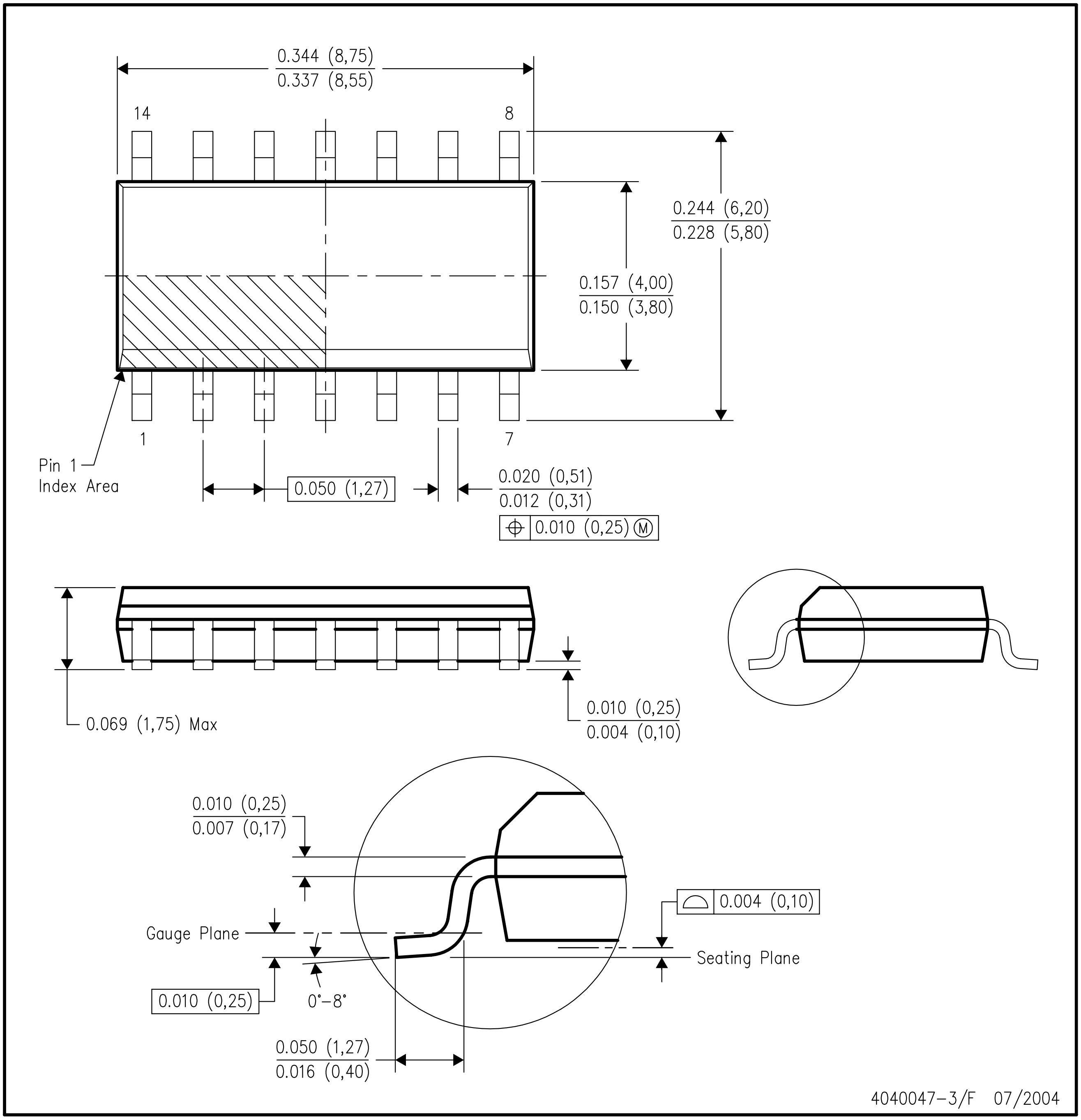


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
(C) MS-001 VARIATION	AA	BB	AC	AD

4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G14) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-012 variation AB.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265