

# 16-bit Proprietary Microcontroller

CMOS

## F<sup>2</sup>MC-16LX MB90590/590G Series

### MB90591/F591A/594/594G/F594A/F594G MB90V590A/V590G

#### ■ DESCRIPTION

The MB90590/590G series with two FULL-CAN\*<sup>1</sup> interfaces and FLASH ROM is especially designed for automotive and industrial applications. Its main features are two on board CAN Interfaces, which conform to V2.0 Part A and Part B, while supporting a very flexible message buffer scheme and so offering more functions than a normal full CAN approach.

The instruction set of F<sup>2</sup>MC-16LX CPU core inherits an AT architecture of the F<sup>2</sup>MC\*<sup>2</sup> family with additional instruction sets for high-level languages, extended addressing mode, enhanced multiplication/division instructions, and enhanced bit manipulation instructions. The microcontroller has a 32-bit accumulator for processing long word data.

The MB90590/590G series has peripheral resources of 8/10-bit A/D converters, UART (SCI), extended I/O serial interface, 8/16-bit PPG timer, I/O timer (input capture (ICU), output compare (OCU)), stepping motor controller, and sound generator.

\*1: Controller Area Network (CAN) - License of Robert Bosch GmbH

\*2: F<sup>2</sup>MC stands for FUJITSU Flexible Microcontroller.

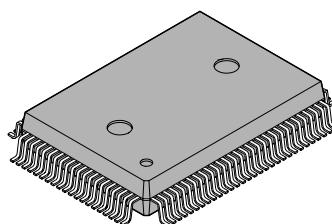
#### ■ FEATURES

- Clock
  - Embedded PLL clock multiplication circuit
  - Operating clock (PLL clock) can be selected from divided-by-2 of oscillation or one to four times the oscillation (at oscillation of 4 MHz, 4 MHz to 16 MHz).
  - Minimum instruction execution time: 62.5 ns (operation at oscillation of 4 MHz, four times the oscillation clock, V<sub>CC</sub> of 5.0 V)

(Continued)

#### ■ PACKAGE

100-pin Plastic QFP



(FPT-100P-M06)

# MB90590/590G Series

(Continued)

- Instruction set to optimize controller applications
  - Rich data types (bit, byte, word, long word)
  - Rich addressing mode (23 types)
  - Enhanced signed multiplication/division instruction and RETI instruction functions
  - Enhanced precision calculation realized by the 32-bit accumulator
- Instruction set designed for high level language (C language) and multi-task operations
  - Adoption of system stack pointer
  - Enhanced pointer indirect instructions
  - Barrel shift instructions
- Program patch function (for two address pointers)
- Enhanced execution speed: 4-byte instruction queue
- Enhanced interrupt function: 8 levels, 34 factors
- Automatic data transmission function independent of CPU operation
  - Extended intelligent I/O service function (EI<sup>2</sup>OS): Up to 10 channels
- Embedded ROM size and types
  - Mask ROM: 256 Kbytes/384 Kbytes
  - Flash ROM: 256 Kbytes/384 Kbytes
  - Embedded RAM size: 6 Kbytes/8 Kbytes
- Flash ROM
  - Supports automatic programming, Embedded Algorithm ™\*
  - Write/Erase/Erase-Suspend/Resume commands
  - A flag indicating completion of the algorithm
  - Hard-wired reset vector available in order to point to a fixed boot sector in Flash Memory
  - Erase can be performed on each block
  - Block protection with external programming voltage
- Low-power consumption (stand-by) mode
  - Sleep mode (mode in which CPU operating clock is stopped)
  - Stop mode (mode in which oscillation is stopped)
  - CPU intermittent operation mode
  - Clock mode
  - Hardware stand-by mode
- Process
  - 0.5μm CMOS technology
- I/O port
  - General-purpose I/O ports: 78 ports
- Timer
  - Watchdog timer: 1 channel
  - 8/16-bit PPG timer: 8/16-bit × 6 channels
  - 16-bit re-load timer: 2 channels
- 16-bit I/O timer
  - 16-bit free-run timer: 1 channel
  - Input capture: 6 channels
  - Output compare: 6 channels
- Extended I/O serial interface: 1 channel
- UART (3 channels)
  - With full-duplex double buffer (8-bit length)
  - Clock asynchronized or clock synchronized (with start/stop bit) transmission can be selectively used.
- Stepping motor controller (4 channels)

- External interrupt circuit (8 channels)  
A module for starting an extended intelligent I/O service (EI<sup>2</sup>OS) and generating an external interrupt which is triggered by an external input.
- Delayed interrupt generation module  
Generates an interrupt request for switching tasks.
- 8/10-bit A/D converter (8 channels)  
8/10-bit resolution can be selectively used.  
Starting by an external trigger input.
- FULL-CAN interfaces: 2  
Conforming to Version 2.0 Part A and Part B  
Flexible message buffering (mailbox and FIFO buffering can be mixed)
- Sound generator
- 18-bit Time-base counter
- Clock timer: 1 channel
- External bus interface: Maximum address space 16 Mbytes

\*: Embedded Algorithm is a trade mark of Advanced Micro Devices Inc.

# MB90590/590G Series

## ■ PRODUCT LINEUP

| Features                          |                        | MB90591/594/594G                                                                                                                                                                                                                                                                                                                                                                                              | MB90F591A/F594A/F594G                                   | MB90V590A/V590G    |
|-----------------------------------|------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------|--------------------|
| Classification                    |                        | Mask ROM product                                                                                                                                                                                                                                                                                                                                                                                              | Flash ROM product                                       | Evaluation product |
| ROM size                          |                        | 384/256 Kbytes                                                                                                                                                                                                                                                                                                                                                                                                | 384/256 Kbytes<br>Boot block<br>Hard-wired reset vector | None               |
| RAM size                          |                        | 8/6 Kbytes                                                                                                                                                                                                                                                                                                                                                                                                    | 8/6 Kbytes                                              | 8 Kbytes           |
| Emulator-specific power supply *1 |                        | —                                                                                                                                                                                                                                                                                                                                                                                                             |                                                         | None               |
| CPU functions                     |                        | The number of instructions: 340<br>Instruction bit length: 8 bits, 16 bits<br>Instruction length: 1 byte to 7 bytes<br>Data bit length: 1 bit, 8 bits, 16 bits<br>Minimum execution time: 62.5 ns (at machine clock frequency of 16 MHz)<br>Interrupt processing time: 1.5 $\mu$ s<br>(at machine clock frequency of 16 MHz, minimum value)                                                                   |                                                         |                    |
| UART (3 channels)                 |                        | Clock synchronized transmission (500 kbps / 1 Mbps / 2 Mbps)<br>Clock asynchronized transmission (4808/5208/9615/10417/19230/38460/62500 /500000 bps at machine clock frequency of 16 MHz)<br>Transmission can be performed by bi-directional serial transmission or by master/slave connection.                                                                                                              |                                                         |                    |
| 8/10-bit A/D converter            |                        | Conversion precision: 8/10-bit can be selectively used.<br>Number of inputs: 8<br>One-shot conversion mode (converts selected channel once only)<br>Scan conversion mode (converts two or more successive channels and can program up to 8 channels)<br>Continuous conversion mode (converts selected channel continuously)<br>Stop conversion mode (converts selected channel and stop operation repeatedly) |                                                         |                    |
| 8/16-bit PPG timers (6 channels)  |                        | Number of channels: 6 (8/16-bit $\times$ 6 channels)<br>PPG operation of 8-bit or 16-bit<br>A pulse wave of given intervals and given duty ratios can be output.<br>Pulse interval: $f_{sys}$ , $f_{sys}/2^1$ , $f_{sys}/2^2$ , $f_{sys}/2^3$ , $f_{sys}/2^4$ , 128 $\mu$ s<br>(at oscillation of 4 MHz, $f_{sys}$ = system clock frequency of 16 MHz, $f_{osc}$ = oscillation clock frequency)               |                                                         |                    |
| 16-bit Reload timer               |                        | Number of channels: 2<br>Operation clock frequency: $f_{sys}/2^1$ , $f_{sys}/2^3$ , $f_{sys}/2^5$ ( $f_{sys}$ = System clock frequency)<br>Supports External Event Count function                                                                                                                                                                                                                             |                                                         |                    |
| 16-bit I/O timer                  | 16-bit Output compares | Number of channels: 6 (8/16-bit $\times$ 6 channels)<br>Pin input factor: A match signal of compare register                                                                                                                                                                                                                                                                                                  |                                                         |                    |
|                                   | Input captures         | Number of channels: 6<br>Rewriting a register value upon a pin input (rising, falling, or both edges)                                                                                                                                                                                                                                                                                                         |                                                         |                    |

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# MB90590/590G Series

(Continued)

| Features                               | MB90591/594/594G                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | MB90F591A/F594A/F594G | MB90V590A/V590G |
|----------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|-----------------|
| CAN Interface                          | Number of channels: 2<br>Conforms to CAN Specification Version 2.0 Part A and B<br>Automatic re-transmission in case of error<br>Automatic transmission responding to Remote Frame<br>Prioritized 16 message buffers for data and ID's<br>Supports multiple messages<br>Flexible configuration of acceptance filtering:<br>Full bit compare / Full bit mask / Two partial bit masks<br>Supports up to 1Mbps<br>CAN bit timing setting:<br>MB90xxx:TSEG2 $\geq$ RSJW+2TQ<br>MB90xxxG:TSEG2 $\geq$ RSJW |                       |                 |
| Stepping motor controller (4 channels) | Four high current outputs for each channel<br>Synchronized two 8-bit PWM's for each channel                                                                                                                                                                                                                                                                                                                                                                                                           |                       |                 |
| External interrupt circuit             | Number of inputs: 8<br>Started by a rising edge, a falling edge, an "H" level input, or an "L" level input.                                                                                                                                                                                                                                                                                                                                                                                           |                       |                 |
| Sound generator                        | 8-bit PWM signal is mixed with tone frequency from 8-bit reload counter<br>PWM frequency: 62.5K, 31.2K, 15.6K, 7.8KHz (at System clock = 16MHz)<br>Tone frequency: PWM frequency / 2 / (reload value + 1)                                                                                                                                                                                                                                                                                             |                       |                 |
| Extended I/O serial interface          | Clock synchronized transmission (31.25K/62.5K/125K/500K/1Mbps at machine clock frequency of 16 MHz)<br>LSB first/MSB first                                                                                                                                                                                                                                                                                                                                                                            |                       |                 |
| Clock timer                            | Directly operates with the system clock<br>Read/Write accessible Second/Minute/Hour registers                                                                                                                                                                                                                                                                                                                                                                                                         |                       |                 |
| Watchdog timer                         | Reset generation interval: 3.58 ms, 14.33 ms, 57.23 ms, 458.75 ms<br>(at oscillation of 4 MHz, minimum value)                                                                                                                                                                                                                                                                                                                                                                                         |                       |                 |
| Flash Memory                           | Supports automatic programming, Embedded Algorithm™ and Write/Erase/Erase-Suspend/Resume commands<br>A flag indicating completion of the algorithm<br>Hard-wired reset vector available in order to point to a fixed boot sector in Flash Memory<br>Boot block configuration<br>Erase can be performed on each block<br>Block protection with external programming voltage<br>Flash Writer from Minato Electronics Inc.                                                                               |                       |                 |
| Low-power consumption (stand-by) mode  | Sleep/stop/CPU intermittent operation/clock timer/hardware stand-by                                                                                                                                                                                                                                                                                                                                                                                                                                   |                       |                 |
| Process                                | CMOS                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |                       |                 |
| Power supply voltage for operation*2   | 5 V $\pm$ 10 % (MB90V590A, MB90F594A, MB90594, MB90V590G, MB90F594G, MB90594G)<br>5 V $\pm$ 5 % (MB90F591A, MB90591)                                                                                                                                                                                                                                                                                                                                                                                  |                       |                 |
| Package                                | QFP-100                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |                       | PGA-256         |

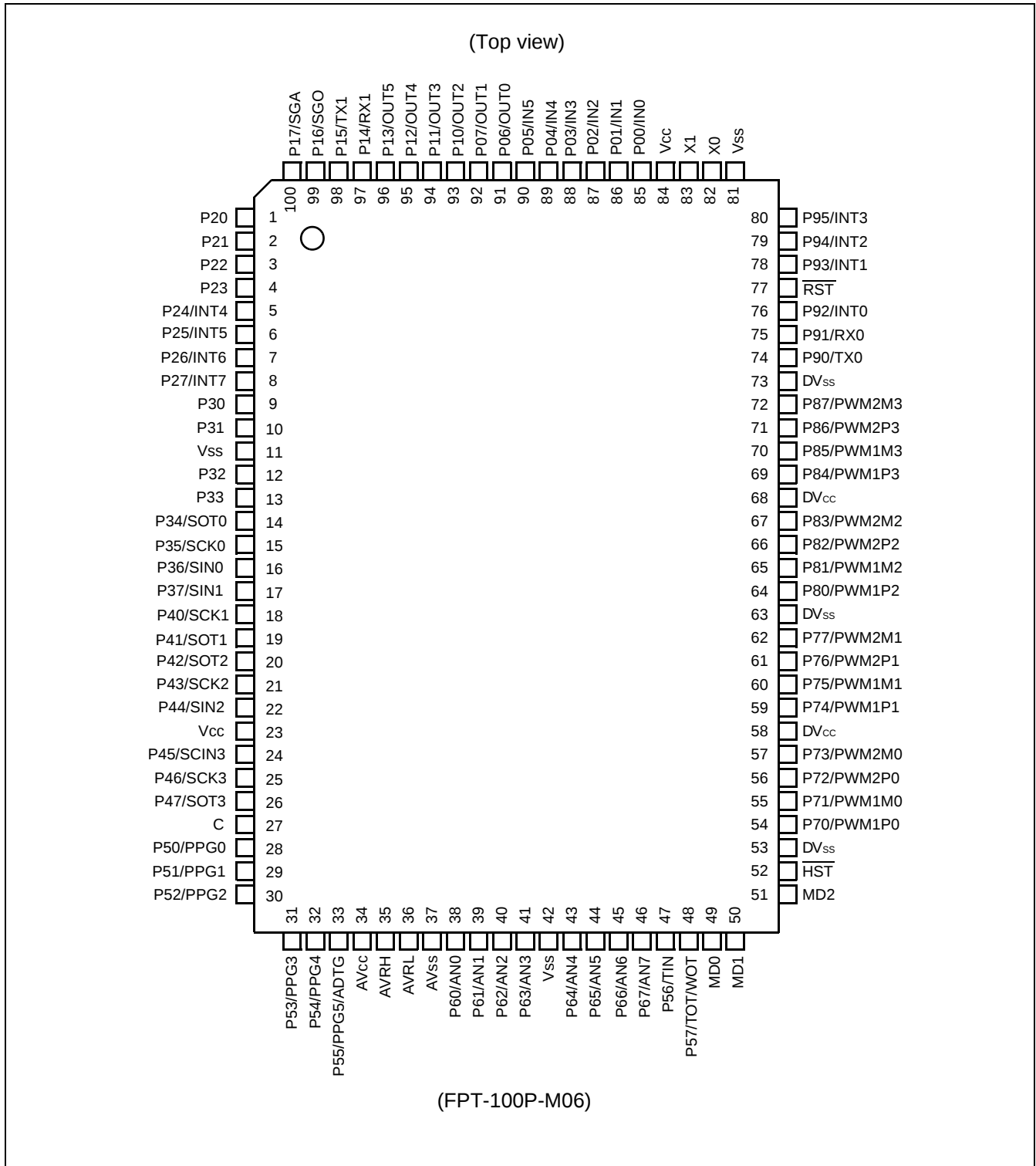
\*1: It is setting of DIP switch S2 when Emulation pod (MB2145-507) is used.

Please refer to the MB2145-507 hardware manual (2.7 Emulator-specific Power Pin) about details.

\*2: Varies with conditions such as the operating frequency. (See section "■ Electrical Characteristics.")

# MB90590/590G Series

## PIN ASSIGNMENT



## ■ PIN DESCRIPTION

| No.      | Pin name                 | Circuit type | Function                                                                                                                                       |
|----------|--------------------------|--------------|------------------------------------------------------------------------------------------------------------------------------------------------|
| 82       | X0                       | A            | Oscillator pin                                                                                                                                 |
| 83       | X1                       |              |                                                                                                                                                |
| 77       | $\overline{\text{RST}}$  | B            | Reset input                                                                                                                                    |
| 52       | $\overline{\text{HST}}$  | C            | Hardware standby input                                                                                                                         |
| 85 to 90 | P00 to P05               | D            | General purpose IO                                                                                                                             |
|          | IN0 to IN5               |              | Inputs for the Input Captures                                                                                                                  |
| 91 to 96 | P06 to P07<br>P10 to P13 | D            | General purpose IO                                                                                                                             |
|          | OUT0 to OUT5             |              | Outputs for the Output Compares.<br>To enable the signal outputs, the corresponding bits of the Port Direction registers should be set to "1". |
| 97       | P14                      | D            | General purpose IO                                                                                                                             |
|          | RX1                      |              | RX input for CAN Interface 1                                                                                                                   |
| 98       | P15                      | D            | General purpose IO                                                                                                                             |
|          | TX1                      |              | TX output for CAN Interface 1.<br>To enable the signal output, the corresponding bit of the Port Direction register should be set to "1".      |
| 99       | P16                      | D            | General purpose IO                                                                                                                             |
|          | SGO                      |              | SGO output for the Sound Generator.<br>To enable the signal output, the corresponding bit of the Port Direction register should be set to "1". |
| 100      | P17                      | D            | General purpose IO                                                                                                                             |
|          | SGA                      |              | SGA output for the Sound Generator.<br>To enable the signal output, the corresponding bit of the Port Direction register should be set to "1". |
| 1 to 4   | P20 to P23               | D            | General purpose IO                                                                                                                             |
| 5 to 8   | P24 to P27               | D            | General purpose IO                                                                                                                             |
|          | INT4 to INT7             |              | External interrupt input for INT4 to INT7                                                                                                      |
| 9 to 10  | P30 to P31               | D            | General purpose IO                                                                                                                             |
| 12 to 13 | P32 to P33               | D            | General purpose IO                                                                                                                             |
| 14       | P34                      | D            | General purpose IO                                                                                                                             |
|          | SOT0                     |              | SOT output for UART 0.<br>To enable the signal output, the corresponding bit of the Port Direction register should be set to "1".              |
| 15       | P35                      | D            | General purpose IO                                                                                                                             |
|          | SCK0                     |              | SCK input/output for UART 0.<br>To enable the signal output, the corresponding bit of the Port Direction register should be set to "1".        |

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# MB90590/590G Series

| No.      | Pin name           | Circuit type | Function                                                                                                                                                                                                       |
|----------|--------------------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 16       | P36                | D            | General purpose IO                                                                                                                                                                                             |
|          | SIN0               |              | SIN input for UART 0                                                                                                                                                                                           |
| 17       | P37                | D            | General purpose IO                                                                                                                                                                                             |
|          | SIN1               |              | SIN input for UART 1                                                                                                                                                                                           |
| 18       | P40                | D            | General purpose IO                                                                                                                                                                                             |
|          | SCK1               |              | SCK input/output for UART 1                                                                                                                                                                                    |
| 19       | P41                | D            | General purpose IO                                                                                                                                                                                             |
|          | SOT1               |              | SOT output for UART 1                                                                                                                                                                                          |
| 20       | P42                | D            | General purpose IO                                                                                                                                                                                             |
|          | SOT2               |              | SOT output for UART 2                                                                                                                                                                                          |
| 21       | P43                | D            | General purpose IO                                                                                                                                                                                             |
|          | SCK2               |              | SCK input/output for UART 2                                                                                                                                                                                    |
| 22       | P44                | D            | General purpose IO                                                                                                                                                                                             |
|          | SIN2               |              | SIN input for UART 2                                                                                                                                                                                           |
| 24       | P45                | D            | General purpose IO                                                                                                                                                                                             |
|          | SIN3               |              | SIN input for the Serial IO                                                                                                                                                                                    |
| 25       | P46                | D            | General purpose IO                                                                                                                                                                                             |
|          | SCK3               |              | SCK input/output for the Serial IO                                                                                                                                                                             |
| 26       | P47                | D            | General purpose IO                                                                                                                                                                                             |
|          | SOT3               |              | SOT output for the Serial IO                                                                                                                                                                                   |
| 28 to 33 | P50 to P55         | D            | General purpose IO                                                                                                                                                                                             |
|          | PPG0 to PPG5, ADTG |              | Outputs for the Programmable Pulse Generators. Pin number 33 is also shared with ADTG input for the external trigger of the A/D Converter.                                                                     |
| 38 to 41 | P60 to P63         | E            | General purpose IO                                                                                                                                                                                             |
|          | AN0 to AN3         |              | Inputs for the A/D Converter                                                                                                                                                                                   |
| 43 to 46 | P64 to P67         | E            | General purpose IO                                                                                                                                                                                             |
|          | AN4 to AN7         |              | Inputs for the A/D Converter                                                                                                                                                                                   |
| 47       | P56                | D            | General purpose IO                                                                                                                                                                                             |
|          | TIN                |              | TIN input for the 16-bit Reload Timers                                                                                                                                                                         |
| 48       | P57                | D            | General purpose IO                                                                                                                                                                                             |
|          | TOT/WOT            |              | TOT output for the 16-bit Reload Timers and WOT output for the Watch Timer. Only one of three output enable flags in these peripheral blocks can be set at a time. Otherwise the output signal has no meaning. |

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# MB90590/590G Series

| No.        | Pin name                             | Circuit type | Function                                                                                                                                                                                         |
|------------|--------------------------------------|--------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 54 to 57   | P70 to P73                           | F            | General purpose IO                                                                                                                                                                               |
|            | PWM1P0<br>PWM1M0<br>PWM2P0<br>PWM2M0 |              | Output for Stepping Motor Controller channel 0.                                                                                                                                                  |
| 59 to 62   | P74 to P77                           | F            | General purpose IO                                                                                                                                                                               |
|            | PWM1P1<br>PWM1M1<br>PWM2P1<br>PWM2M1 |              | Output for Stepping Motor Controller channel 1.                                                                                                                                                  |
| 64 to 67   | P80 to P83                           | F            | General purpose IO                                                                                                                                                                               |
|            | PWM1P2<br>PWM1M2<br>PWM2P2<br>PWM2M2 |              | Output for Stepping Motor Controller channel 2.                                                                                                                                                  |
| 69 to 72   | P84 to P87                           | F            | General purpose IO                                                                                                                                                                               |
|            | PWM1P3<br>PWM1M3<br>PWM2P3<br>PWM2M3 |              | Output for Stepping Motor Controller channel 3.                                                                                                                                                  |
| 74         | P90                                  | D            | General purpose IO                                                                                                                                                                               |
|            | TX0                                  |              | TX output for CAN Interface 0                                                                                                                                                                    |
| 75         | P91                                  | D            | General purpose IO                                                                                                                                                                               |
|            | RX0                                  |              | RX input for CAN Interface 0                                                                                                                                                                     |
| 76         | P92                                  | D            | General purpose IO                                                                                                                                                                               |
|            | INT0                                 |              | External interrupt input for INT0                                                                                                                                                                |
| 78         | P93                                  | D            | General purpose IO                                                                                                                                                                               |
|            | INT1                                 |              | External interrupt input for INT1                                                                                                                                                                |
| 79         | P94                                  | D            | General purpose IO                                                                                                                                                                               |
|            | INT2                                 |              | External interrupt input for INT2                                                                                                                                                                |
| 80         | P95                                  | D            | General purpose IO                                                                                                                                                                               |
|            | INT3                                 |              | External interrupt input for INT3                                                                                                                                                                |
| 58, 68     | DV <sub>CC</sub>                     | —            | Dedicated power supply pins for the high current output buffers (Pin No. 54 to 72)                                                                                                               |
| 53, 63, 73 | DV <sub>SS</sub>                     | —            | Dedicated ground pins for the high current output buffers (Pin No. 54 to 72)                                                                                                                     |
| 34         | AV <sub>CC</sub>                     | Power supply | Power supply for analog circuit pin<br>When turning this power supply on or off, always be sure to first apply electric potential equal to or greater than AV <sub>CC</sub> to V <sub>CC</sub> . |
| 37         | AV <sub>SS</sub>                     | Power supply | Ground level for analog circuit                                                                                                                                                                  |

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# MB90590/590G Series

(Continued)

| No.      | Pin name        | Circuit type | Function                                                                                                                                                                                         |
|----------|-----------------|--------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 35       | AVRH            | Power supply | Reference voltage input pin for analog circuit<br>When turning this power supply on or off, always be sure to first apply electric potential equal to or greater than AVRH to AV <sub>CC</sub> . |
| 36       | AVRL            | Power supply | Reference voltage input pin for analog circuit                                                                                                                                                   |
| 49, 50   | MD0, MD1        | C            | Operating mode selection input pins<br>Connect directly to V <sub>CC</sub> or V <sub>SS</sub> .                                                                                                  |
| 51       | MD2             | G            | Operating mode selection input pin<br>Connect directly to V <sub>CC</sub> or V <sub>SS</sub> .                                                                                                   |
| 27       | C               | —            | This is the power supply stabilization capacitor pin. It should be connected externally to an 0.1 $\mu$ F ceramic capacitor.                                                                     |
| 23, 84   | V <sub>CC</sub> | Power supply | Power supply (5.0 V) input pin for digital circuit                                                                                                                                               |
| 11,42,81 | V <sub>SS</sub> | Power supply | Power supply (GND) input pin for digital circuit                                                                                                                                                 |

## I/O CIRCUIT TYPE

| Circuit Type | Circuit | Remarks                                                                                                                       |
|--------------|---------|-------------------------------------------------------------------------------------------------------------------------------|
| A            |         | <ul style="list-style-type: none"> <li>Oscillation feedback resistor:<br/>1 M<math>\Omega</math> approx.</li> </ul>           |
| B            |         | <ul style="list-style-type: none"> <li>Hysteresis input with pull-up Resistor:<br/>50 k<math>\Omega</math> approx.</li> </ul> |
| C            |         | <ul style="list-style-type: none"> <li>Hysteresis input</li> </ul>                                                            |
| D            |         | <ul style="list-style-type: none"> <li>CMOS output</li> <li>Hysteresis input</li> </ul>                                       |

(Continued)

# MB90590/590G Series

| Circuit Type | Circuit | Remarks                                                                                                                                                                |
|--------------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| E            |         | <ul style="list-style-type: none"> <li>• CMOS output</li> <li>• Hysteresis input</li> <li>• Analog input</li> </ul>                                                    |
| F            |         | <ul style="list-style-type: none"> <li>• CMOS high current output</li> <li>• Hysteresis input</li> </ul>                                                               |
| G            |         | <ul style="list-style-type: none"> <li>• Hysteresis input with pull-down Resistor: 50 kΩ approx.</li> <li>• Flash version does not have pull-down resistor.</li> </ul> |

## ■ HANDLING DEVICES

### (1) Preventing latch-up

CMOS IC chips may suffer latch-up under the following conditions:

- A voltage higher than  $V_{CC}$  or lower than  $V_{SS}$  is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between  $V_{CC}$  and  $V_{SS}$ .
- The  $AV_{CC}$  power supply is applied before the  $V_{CC}$  voltage.

Latch-up may increase the power supply current drastically, causing thermal damage to the device.

For the same reason, also be careful not to let the analog power-supply voltage ( $AV_{CC}$ ,  $AV_{RH}$ ,  $DV_{CC}$ ) exceed the digital power-supply voltage.

### (2) Treatment of unused pins

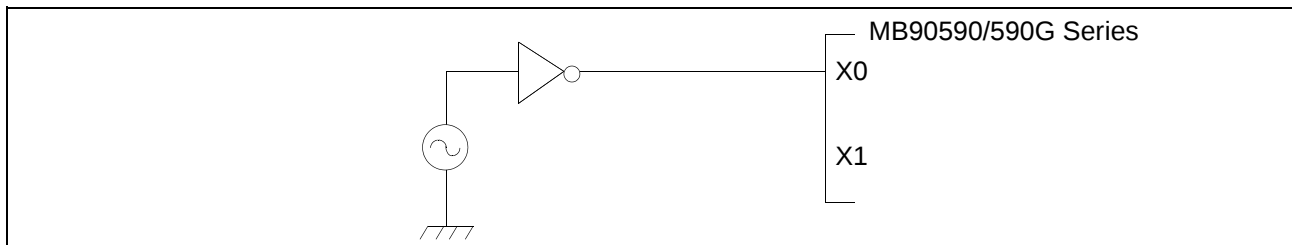
Leaving unused input pins open may result in misbehavior or latch up and possible permanent damage of the device. Therefore they must be pulled up or pulled down through resistors. In this case those resistors should be more than  $2\text{ k}\Omega$ .

Unused bidirectional pins should be set to the output state and can be left open, or the input state with the above described connection.

### (3) Using external clock

To use external clock, drive X0 pin only and leave X1 pin unconnected.

Below is a diagram of how to use external clock.



Using external clock

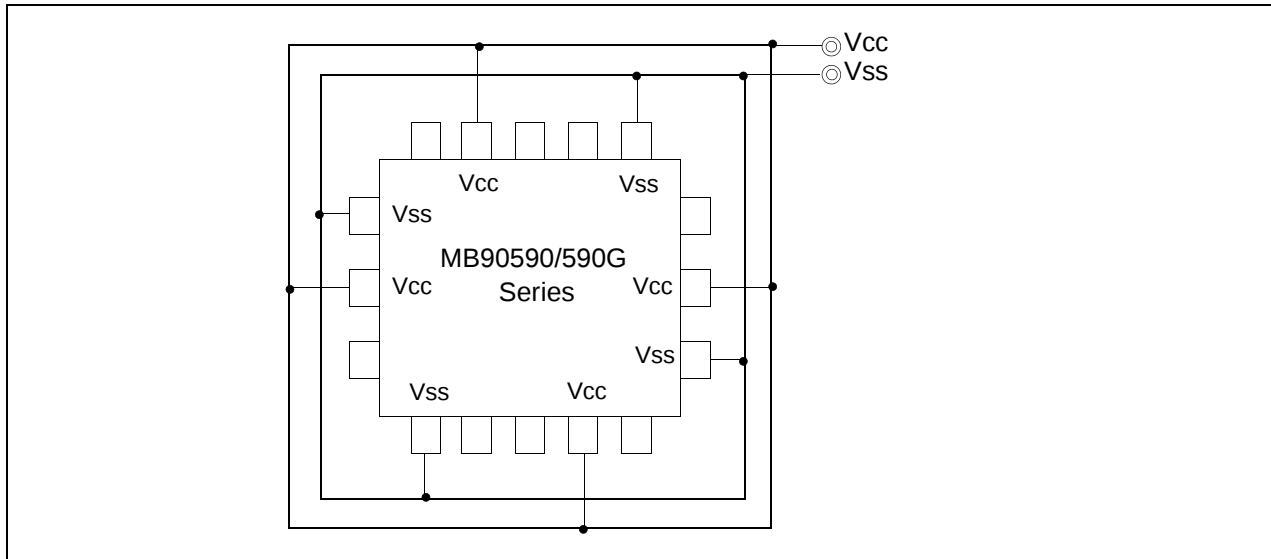
# MB90590/590G Series

## (4) Power supply pins (V<sub>CC</sub>/V<sub>SS</sub>)

In products with multiple V<sub>CC</sub> or V<sub>SS</sub> pins, pins with the same potential are internally connected in the device to avoid abnormal operations including latch-up. However, you must connect the pins to an external power and a ground line to lower the electro-magnetic emission level to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total current rating.

Make sure to connect V<sub>CC</sub> and V<sub>SS</sub> pins via lowest impedance to power lines.

It is recommended to provide a bypass capacitor of around 0.1  $\mu$ F between V<sub>CC</sub> and V<sub>SS</sub> pin near the device.



## (5) Pull-up/down resistors

The MB90590/590G Series does not support internal pull-up/down resistors. Use external components where needed.

## (6) Crystal Oscillator Circuit

Noises around X0 or X1 pins may cause abnormal operations. Make sure to provide bypass capacitors via the shortest distances from X0, X1 pins, crystal oscillator (or ceramic resonator) and ground lines, and make sure that lines of oscillation circuits do not cross the lines of other circuits.

A printed circuit board artwork surrounding the X0 and X1 pins with a ground area for stabilizing the operation is highly recommended.

## (7) Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs

Make sure to turn on the A/D converter power supply (AV<sub>CC</sub>, AVR<sub>H</sub>, AVR<sub>L</sub>) and analog inputs (AN0 to AN7) after turning-on the digital power supply (V<sub>CC</sub>).

Turn-off the digital power after turning off the A/D converter supply and analog inputs. In this case, make sure that the voltage does not exceed AVR<sub>H</sub> or AV<sub>CC</sub> (turning on/off the analog and digital power supplies simultaneously is acceptable).

## (8) Connection of Unused Pins of A/D Converter

Connect unused pins of A/D converter to AV<sub>CC</sub> = V<sub>CC</sub>, AV<sub>SS</sub> = AVR<sub>H</sub> = V<sub>SS</sub>.

## (9) N.C. Pin

The N.C. (internally connected) pin must be opened for use.

## (10) Notes on Energization

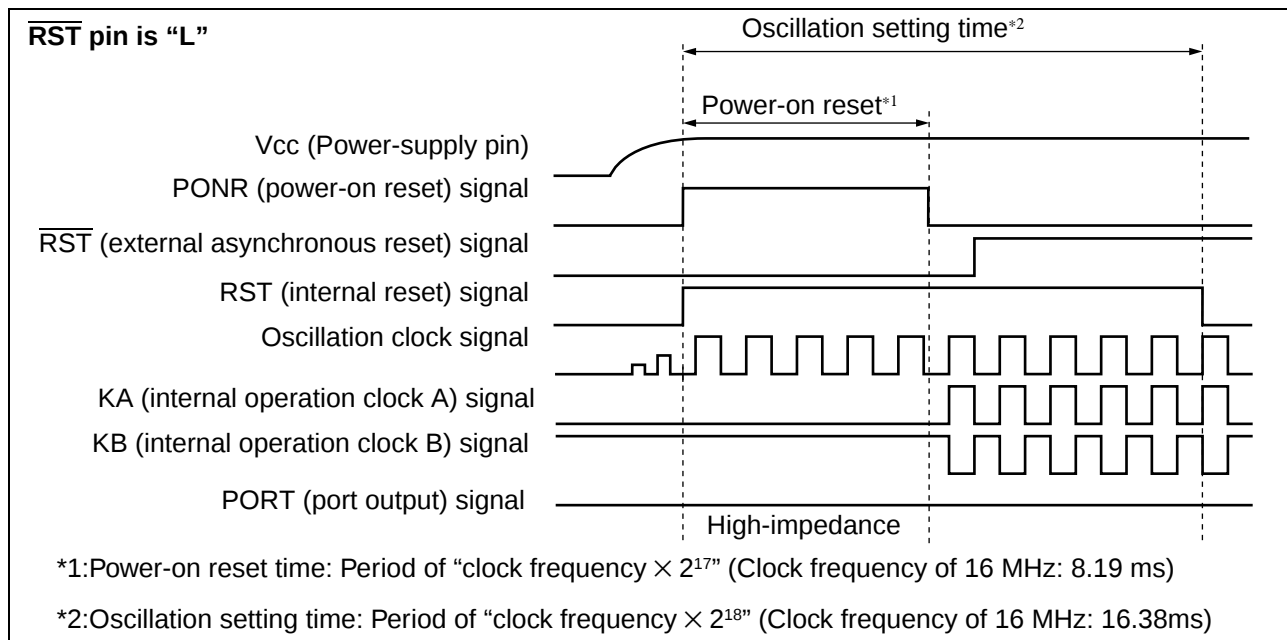
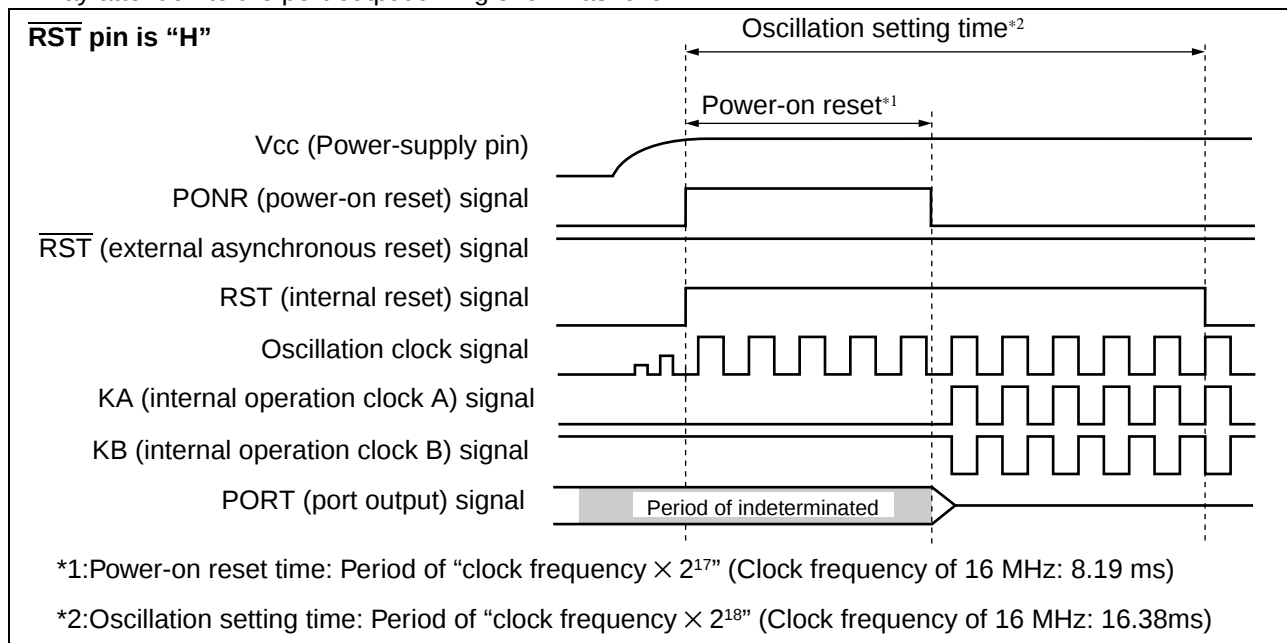
To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during energization at 50  $\mu$ s or more (0.2 V to 2.7 V).

## (11) Indeterminate outputs from ports 0 and 1

During oscillation setting time of step-down circuit (during a power-on reset) after the power is turned on, the outputs from ports 0 and 1 become following state.

- If  $\overline{\text{RST}}$  pin is "H", the outputs become indeterminate.
- If  $\overline{\text{RST}}$  pin is "L", the outputs become high-impedance.

Pay attention to the port output timing shown as follow.



## (12) Initialization

The device contains internal registers which are initialized only by a power-on reset. To initialize these registers, please turn on the power again.

## (13) Directions of “DIV A, Ri” and “DIVW A, RWi” instructions

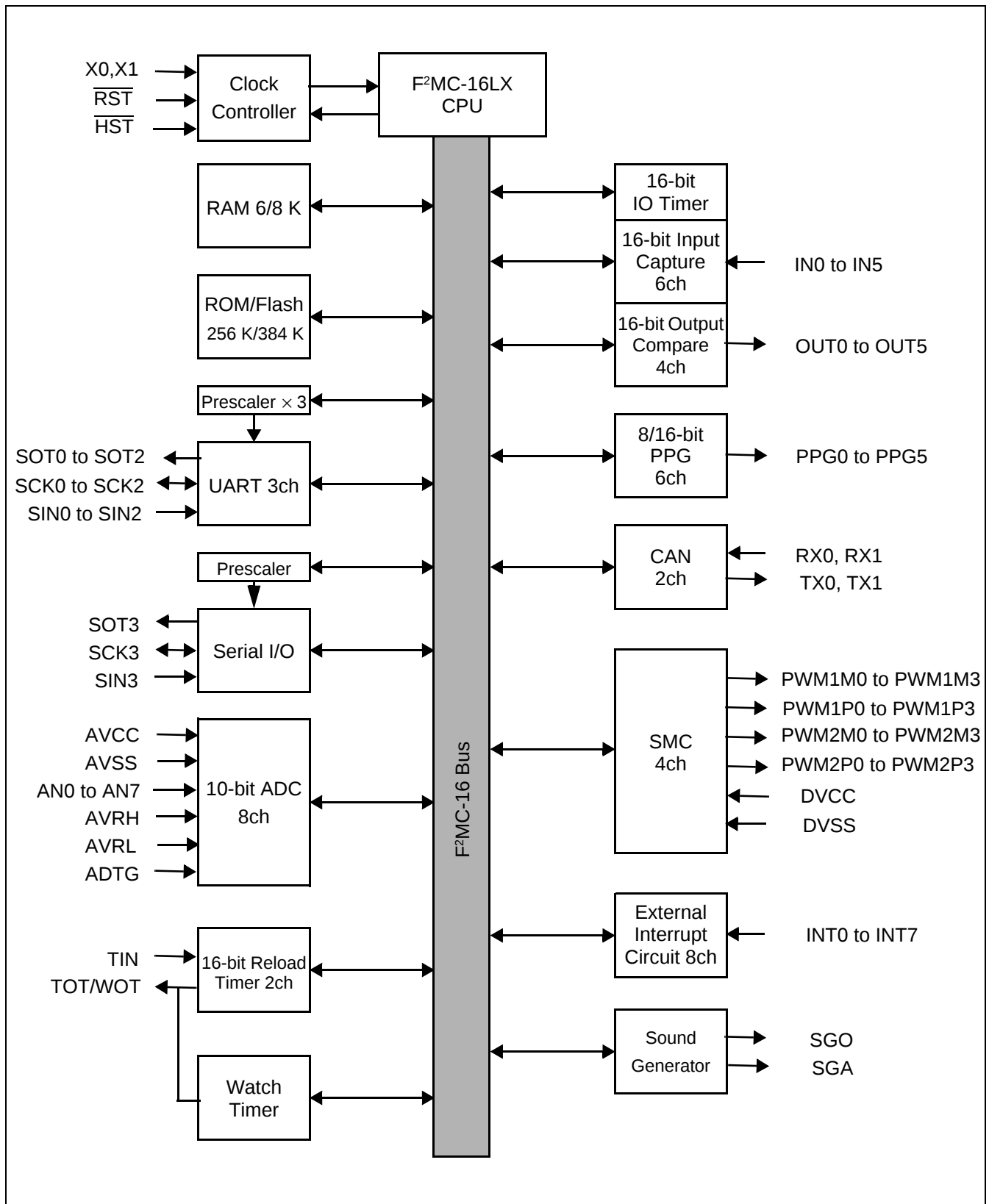
In the Signed multiplication and division instructions (“DIV A, Ri” and “DIVW A, RWi”), the value of the corresponding bank register (DTB, ADB, USB, SSB) is set in “00 H”.

If the values of the corresponding bank registers (DTB, ADB, USB, SSB) are set to other than “00 H”, the remainder by the execution result of the instruction is not stored in the register of the instruction operand.

## (14) Using REALOS

The use of EI<sup>2</sup>OS is not possible with the REALOS real time operating system.

## ■ BLOCK DIAGRAM



# MB90590/590G Series

## ■ MEMORY SPACE

The memory space of the MB90590/590G Series is shown below

| MB90V590A/V590G                                                   |                           | MB90594/F594A/<br>594G/F594G                                      |                           | MB90591/F591A                                                     |                           |
|-------------------------------------------------------------------|---------------------------|-------------------------------------------------------------------|---------------------------|-------------------------------------------------------------------|---------------------------|
| FFFFFF <sub>H</sub><br>FF0000 <sub>H</sub>                        | ROM (FF bank)             | FFFFFF <sub>H</sub><br>FF0000 <sub>H</sub>                        | ROM (FF bank)             | FFFFFF <sub>H</sub><br>FF0000 <sub>H</sub>                        | ROM (FF bank)             |
| FEFFFF <sub>H</sub><br>FE0000 <sub>H</sub>                        | ROM (FE bank)             | FEFFFF <sub>H</sub><br>FE0000 <sub>H</sub>                        | ROM (FE bank)             | FEFFFF <sub>H</sub><br>FE0000 <sub>H</sub>                        | ROM (FE bank)             |
| FDFFFF <sub>H</sub><br>FD0000 <sub>H</sub>                        | ROM (FD bank)             | FDFFFF <sub>H</sub><br>FD0000 <sub>H</sub>                        | ROM (FD bank)             | FDFFFF <sub>H</sub><br>FD0000 <sub>H</sub>                        | ROM (FD bank)             |
| FCFFFF <sub>H</sub><br>FC0000 <sub>H</sub>                        | ROM (FC bank)             | FCFFFF <sub>H</sub><br>FC0000 <sub>H</sub>                        | ROM (FC bank)             | FCFFFF <sub>H</sub><br>FC0000 <sub>H</sub>                        |                           |
| FBFFFF <sub>H</sub><br>FB0000 <sub>H</sub>                        | ROM (FB bank)             |                                                                   |                           | FBFFFF <sub>H</sub><br>FB0000 <sub>H</sub>                        | ROM (FB bank)             |
| FAFFFF <sub>H</sub><br>FA0000 <sub>H</sub>                        | ROM (FA bank)             |                                                                   |                           | FAFFFF <sub>H</sub><br>FA0000 <sub>H</sub>                        | ROM (FA bank)             |
| F9FFFF <sub>H</sub><br>F90000 <sub>H</sub>                        | ROM (F9 bank)             |                                                                   |                           | F9FFFF <sub>H</sub><br>F90000 <sub>H</sub>                        | ROM (F9 bank)             |
|                                                                   |                           |                                                                   |                           |                                                                   |                           |
| 00FFFF <sub>H</sub><br>004000 <sub>H</sub>                        | ROM<br>(Image of FF bank) | 00FFFF <sub>H</sub><br>004000 <sub>H</sub>                        | ROM<br>(Image of FF bank) | 00FFFF <sub>H</sub><br>004000 <sub>H</sub>                        | ROM<br>(Image of FF bank) |
|                                                                   |                           |                                                                   |                           |                                                                   |                           |
| 0028FF <sub>H</sub><br>002100 <sub>H</sub><br>0020FF <sub>H</sub> | RAM 2K                    |                                                                   |                           | 0028FF <sub>H</sub><br>002100 <sub>H</sub><br>0020FF <sub>H</sub> | RAM 2K                    |
|                                                                   |                           |                                                                   |                           |                                                                   |                           |
| 001FFF <sub>H</sub><br>001900 <sub>H</sub><br>0018FF <sub>H</sub> | Peripheral                | 001FFF <sub>H</sub><br>001900 <sub>H</sub><br>0018FF <sub>H</sub> | Peripheral                | 001FFF <sub>H</sub><br>001900 <sub>H</sub><br>0018FF <sub>H</sub> | Peripheral                |
|                                                                   | RAM 6K                    |                                                                   | RAM 6K                    |                                                                   | RAM 6K                    |
| 000100 <sub>H</sub>                                               |                           | 000100 <sub>H</sub>                                               |                           | 000100 <sub>H</sub>                                               |                           |
|                                                                   |                           |                                                                   |                           |                                                                   |                           |
| 0000BF <sub>H</sub><br>000000 <sub>H</sub>                        | Peripheral                | 0000BF <sub>H</sub><br>000000 <sub>H</sub>                        | Peripheral                | 0000BF <sub>H</sub><br>000000 <sub>H</sub>                        | Peripheral                |

**Memory space map**

Note: The ROM data of bank FF is reflected in the upper address of bank 00, realizing effective use of the C compiler small model. The lower 16-bit of bank FF and the lower 16-bit of bank 00 are assigned to the same address, enabling reference of the table on the ROM without stating "far".  
For example, if an attempt has been made to access 00C000<sub>H</sub>, the contents of the ROM at FFC000<sub>H</sub> are accessed. Since the ROM area of the FF bank exceeds 48 Kbytes, the whole area cannot be reflected in the image for the 00 bank. The ROM data at FF4000<sub>H</sub> to FFFFFFF<sub>H</sub> looks, therefore, as if it were the image for 004000<sub>H</sub> to 00FFFF<sub>H</sub>. Thus, it is recommended that the ROM data table be stored in the area of FF4000<sub>H</sub> to FFFFFFF<sub>H</sub>.

## I/O MAP

| Address                            | Register                            | Abbreviation    | Access | Peripheral  | Initial value                |
|------------------------------------|-------------------------------------|-----------------|--------|-------------|------------------------------|
| 00 <sub>H</sub>                    | Port 0 Data Register                | PDR0            | R/W    | Port 0      | XXXXXXXX <sub>B</sub>        |
| 01 <sub>H</sub>                    | Port 1 Data Register                | PDR1            | R/W    | Port 1      | XXXXXXXX <sub>B</sub>        |
| 02 <sub>H</sub>                    | Port 2 Data Register                | PDR2            | R/W    | Port 2      | XXXXXXXX <sub>B</sub>        |
| 03 <sub>H</sub>                    | Port 3 Data Register                | PDR3            | R/W    | Port 3      | XXXXXXXX <sub>B</sub>        |
| 04 <sub>H</sub>                    | Port 4 Data Register                | PDR4            | R/W    | Port 4      | XXXXXXXX <sub>B</sub>        |
| 05 <sub>H</sub>                    | Port 5 Data Register                | PDR5            | R/W    | Port 5      | XXXXXXXX <sub>B</sub>        |
| 06 <sub>H</sub>                    | Port 6 Data Register                | PDR6            | R/W    | Port 6      | XXXXXXXX <sub>B</sub>        |
| 07 <sub>H</sub>                    | Port 7 Data Register                | PDR7            | R/W    | Port 7      | XXXXXXXX <sub>B</sub>        |
| 08 <sub>H</sub>                    | Port 8 Data Register                | PDR8            | R/W    | Port 8      | XXXXXXXX <sub>B</sub>        |
| 09 <sub>H</sub>                    | Port 9 Data Register                | PDR9            | R/W    | Port 9      | __ XXXXXX <sub>B</sub>       |
| 0A <sub>H</sub> to 0F <sub>H</sub> | Reserved                            |                 |        |             |                              |
| 10 <sub>H</sub>                    | Port 0 Direction Register           | DDR0            | R/W    | Port 0      | 0 0 0 0 0 0 0 0 <sub>B</sub> |
| 11 <sub>H</sub>                    | Port 1 Direction Register           | DDR1            | R/W    | Port 1      | 0 0 0 0 0 0 0 0 <sub>B</sub> |
| 12 <sub>H</sub>                    | Port 2 Direction Register           | DDR2            | R/W    | Port 2      | 0 0 0 0 0 0 0 0 <sub>B</sub> |
| 13 <sub>H</sub>                    | Port 3 Direction Register           | DDR3            | R/W    | Port 3      | 0 0 0 0 0 0 0 0 <sub>B</sub> |
| 14 <sub>H</sub>                    | Port 4 Direction Register           | DDR4            | R/W    | Port 4      | 0 0 0 0 0 0 0 0 <sub>B</sub> |
| 15 <sub>H</sub>                    | Port 5 Direction Register           | DDR5            | R/W    | Port 5      | 0 0 0 0 0 0 0 0 <sub>B</sub> |
| 16 <sub>H</sub>                    | Port 6 Direction Register           | DDR6            | R/W    | Port 6      | 0 0 0 0 0 0 0 0 <sub>B</sub> |
| 17 <sub>H</sub>                    | Port 7 Direction Register           | DDR7            | R/W    | Port 7      | 0 0 0 0 0 0 0 0 <sub>B</sub> |
| 18 <sub>H</sub>                    | Port 8 Direction Register           | DDR8            | R/W    | Port 8      | 0 0 0 0 0 0 0 0 <sub>B</sub> |
| 19 <sub>H</sub>                    | Port 9 Direction Register           | DDR9            | R/W    | Port 9      | __ 0 0 0 0 0 0 <sub>B</sub>  |
| 1A <sub>H</sub>                    | Reserved                            |                 |        |             |                              |
| 1B <sub>H</sub>                    | Analog Input Enable Register        | ADER            | R/W    | Port 6, A/D | 1 1 1 1 1 1 1 1 <sub>B</sub> |
| 1C <sub>H</sub> to 1F <sub>H</sub> | Reserved                            |                 |        |             |                              |
| 20 <sub>H</sub>                    | Serial Mode Control Register 0      | UMC0            | R/W    | UART0       | 0 0 0 0 1 0 0 <sub>B</sub>   |
| 21 <sub>H</sub>                    | Serial Status Register 0            | USR0            | R/W    |             | 0 0 0 1 0 0 0 0 <sub>B</sub> |
| 22 <sub>H</sub>                    | Serial Input/Output Data Register 0 | UIDR0/<br>UODR0 | R/W    |             | XXXXXXXX <sub>B</sub>        |
| 23 <sub>H</sub>                    | Rate and Data Register 0            | URD0            | R/W    |             | 0 0 0 0 0 0 0 X <sub>B</sub> |
| 24 <sub>H</sub>                    | Serial Mode Control Register 1      | UMC1            | R/W    | UART1       | 0 0 0 0 1 0 0 <sub>B</sub>   |
| 25 <sub>H</sub>                    | Serial Status Register 1            | USR1            | R/W    |             | 0 0 0 1 0 0 0 0 <sub>B</sub> |
| 26 <sub>H</sub>                    | Serial Input/Output Data Register 1 | UIDR1/<br>UODR1 | R/W    |             | XXXXXXXX <sub>B</sub>        |
| 27 <sub>H</sub>                    | Rate and Data Register 1            | URD1            | R/W    |             | 0 0 0 0 0 0 0 X <sub>B</sub> |

(Continued)

# MB90590/590G Series

| Address         | Register                                  | Abbreviation    | Access | Peripheral                                    | Initial value                |
|-----------------|-------------------------------------------|-----------------|--------|-----------------------------------------------|------------------------------|
| 28 <sub>H</sub> | Serial Mode Control Register 2            | UMC2            | R/W    | UART2                                         | 0 0 0 0 0 1 0 0 <sub>B</sub> |
| 29 <sub>H</sub> | Serial Status Register 2                  | USR2            | R/W    |                                               | 0 0 0 1 0 0 0 0 <sub>B</sub> |
| 2A <sub>H</sub> | Serial Input/Output Data Register 2       | UIDR2/<br>UODR2 | R/W    |                                               | XXXXXXXX <sub>B</sub>        |
| 2B <sub>H</sub> | Rate and Data Register 2                  | URD2            | R/W    |                                               | 0 0 0 0 0 0 0 X <sub>B</sub> |
| 2C <sub>H</sub> | Serial Mode Control Register (low-order)  | SMCS            | R/W    | Serial IO                                     | ___ _ 0 0 0 0 <sub>B</sub>   |
| 2D <sub>H</sub> | Serial Mode Control Register (high-order) | SMCS            | R/W    |                                               | 0 0 0 0 0 0 1 0 <sub>B</sub> |
| 2E <sub>H</sub> | Serial Data Register                      | SDR             | R/W    |                                               | XXXXXXXX <sub>B</sub>        |
| 2F <sub>H</sub> | Edge Selector Register                    | SES             | R/W    |                                               | ___ _ _ _ _ 0 <sub>B</sub>   |
| 30 <sub>H</sub> | External Interrupt Enable Register        | ENIR            | R/W    | External Interrupt                            | 0 0 0 0 0 0 0 0 <sub>B</sub> |
| 31 <sub>H</sub> | External Interrupt Request Register       | EIRR            | R/W    |                                               | XXXXXXXX <sub>B</sub>        |
| 32 <sub>H</sub> | External Interrupt Level Register         | ELVR            | R/W    |                                               | 0 0 0 0 0 0 0 0 <sub>B</sub> |
| 33 <sub>H</sub> | External Interrupt Level Register         | ELVR            | R/W    |                                               | 0 0 0 0 0 0 0 0 <sub>B</sub> |
| 34 <sub>H</sub> | A/D Control Status Register 0             | ADCS0           | R/W    | A/D Converter                                 | 0 0 0 0 0 0 0 0 <sub>B</sub> |
| 35 <sub>H</sub> | A/D Control Status Register 1             | ADCS1           | R/W    |                                               | 0 0 0 0 0 0 0 0 <sub>B</sub> |
| 36 <sub>H</sub> | A/D Data Register 0                       | ADCR0           | R      |                                               | XXXXXXXX <sub>B</sub>        |
| 37 <sub>H</sub> | A/D Data Register 1                       | ADCR1           | R/W    |                                               | 0 0 0 0 1 0 X X <sub>B</sub> |
| 38 <sub>H</sub> | PPG0 Operation Mode Control Register      | PPGC0           | R/W    | 16-bit Programmable<br>Pulse<br>Generator 0/1 | 0 _ 0 0 0 _ _ 1 <sub>B</sub> |
| 39 <sub>H</sub> | PPG1 Operation Mode Control Register      | PPGC1           | R/W    |                                               | 0 _ 0 0 0 0 0 1 <sub>B</sub> |
| 3A <sub>H</sub> | PPG0,1 Output Pin Control Register        | PPG01           | R/W    |                                               | 0 0 0 0 0 0 0 0 <sub>B</sub> |
| 3B <sub>H</sub> | Reserved                                  |                 |        |                                               |                              |
| 3C <sub>H</sub> | PPG2 Operation Mode Control Register      | PPGC2           | R/W    | 16-bit Programmable<br>Pulse<br>Generator 2/3 | 0 _ 0 0 0 _ _ 1 <sub>B</sub> |
| 3D <sub>H</sub> | PPG3 Operation Mode Control Register      | PPGC3           | R/W    |                                               | 0 _ 0 0 0 0 0 1 <sub>B</sub> |
| 3E <sub>H</sub> | PPG2,3 Output Pin Control Register        | PPG23           | R/W    |                                               | 0 0 0 0 0 0 0 0 <sub>B</sub> |
| 3F <sub>H</sub> | Reserved                                  |                 |        |                                               |                              |
| 40 <sub>H</sub> | PPG4 Operation Mode Control Register      | PPGC4           | R/W    | 16-bit Programmable<br>Pulse<br>Generator 4/5 | 0 _ 0 0 0 _ _ 1 <sub>B</sub> |
| 41 <sub>H</sub> | PPG5 Operation Mode Control Register      | PPGC5           | R/W    |                                               | 0 _ 0 0 0 0 0 1 <sub>B</sub> |
| 42 <sub>H</sub> | PPG4,5 Output Pin Control Register        | PPG45           | R/W    |                                               | 0 0 0 0 0 0 0 0 <sub>B</sub> |
| 43 <sub>H</sub> | Reserved                                  |                 |        |                                               |                              |
| 44 <sub>H</sub> | PPG6 Operation Mode Control Register      | PPGC6           | R/W    | 16-bit Programmable<br>Pulse<br>Generator 6/7 | 0 _ 0 0 0 _ _ 1 <sub>B</sub> |
| 45 <sub>H</sub> | PPG7 Operation Mode Control Register      | PPGC7           | R/W    |                                               | 0 _ 0 0 0 0 0 1 <sub>B</sub> |
| 46 <sub>H</sub> | PPG6,7 Output Pin Control Register        | PPG67           | R/W    |                                               | 0 0 0 0 0 0 0 0 <sub>B</sub> |
| 47 <sub>H</sub> | Reserved                                  |                 |        |                                               |                              |

(Continued)

# MB90590/590G Series

| Address         | Register                                     | Abbreviation | Access | Peripheral                              | Initial value         |
|-----------------|----------------------------------------------|--------------|--------|-----------------------------------------|-----------------------|
| 48 <sub>H</sub> | PPG8 Operation Mode Control Register         | PPGC8        | R/W    | 16-bit Programmable Pulse Generator 8/9 | 0_000__1 <sub>B</sub> |
| 49 <sub>H</sub> | PPG9 Operation Mode Control Register         | PPGC9        | R/W    |                                         | 0_000001 <sub>B</sub> |
| 4A <sub>H</sub> | PPG8,9 Output Pin Control Register           | PPG89        | R/W    |                                         | 00000000 <sub>B</sub> |
| 4B <sub>H</sub> | Reserved                                     |              |        |                                         |                       |
| 4C <sub>H</sub> | PPGA Operation Mode Control Register         | PPGCA        | R/W    | 16-bit Programmable Pulse Generator A/B | 0_000__1 <sub>B</sub> |
| 4D <sub>H</sub> | PPGB Operation Mode Control Register         | PPGCB        | R/W    |                                         | 0_000001 <sub>B</sub> |
| 4E <sub>H</sub> | PPGA,B Output Pin Control Register           | PPGAB        | R/W    |                                         | 00000000 <sub>B</sub> |
| 4F <sub>H</sub> | Reserved                                     |              |        |                                         |                       |
| 50 <sub>H</sub> | Timer Control Status Register 0 (low-order)  | TMCSR0       | R/W    | 16-bit Reload Timer 0                   | 00000000 <sub>B</sub> |
| 51 <sub>H</sub> | Timer Control Status Register 0 (high-order) | TMCSR0       | R/W    |                                         | ____0000 <sub>B</sub> |
| 52 <sub>H</sub> | Timer Control Status Register 1 (low-order)  | TMCSR1       | R/W    | 16-bit Reload Timer 1                   | 00000000 <sub>B</sub> |
| 53 <sub>H</sub> | Timer Control Status Register 1 (high-order) | TMCSR1       | R/W    |                                         | ____0000 <sub>B</sub> |
| 54 <sub>H</sub> | Input Capture Control Status Register 0/1    | ICS01        | R/W    | Input Capture 0/1                       | 00000000 <sub>B</sub> |
| 55 <sub>H</sub> | Input Capture Control Status Register 2/3    | ICS23        | R/W    | Input Capture 2/3                       | 00000000 <sub>B</sub> |
| 56 <sub>H</sub> | Input Capture Control Status Register 4/5    | ICS45        | R/W    | Input Capture 4/5                       | 00000000 <sub>B</sub> |
| 57 <sub>H</sub> | Reserved                                     |              |        |                                         |                       |
| 58 <sub>H</sub> | Output Compare Control Status Register 0     | OCS0         | R/W    | Output Compare 0/1                      | 0000__00 <sub>B</sub> |
| 59 <sub>H</sub> | Output Compare Control Status Register 1     | OCS1         | R/W    |                                         | __000000 <sub>B</sub> |
| 5A <sub>H</sub> | Output Compare Control Status Register 2     | OCS2         | R/W    | Output Compare 2/3                      | 0000__00 <sub>B</sub> |
| 5B <sub>H</sub> | Output Compare Control Status Register 3     | OCS3         | R/W    |                                         | __000000 <sub>B</sub> |
| 5C <sub>H</sub> | Output Compare Control Status Register 4     | OCS4         | R/W    | Output Compare 4/5                      | 0000__00 <sub>B</sub> |
| 5D <sub>H</sub> | Output Compare Control Status Register 5     | OCS5         | R/W    |                                         | __000000 <sub>B</sub> |
| 5E <sub>H</sub> | Sound Control Register (low-order)           | SGCR         | R/W    | Sound Generator                         | 00000000 <sub>B</sub> |
| 5F <sub>H</sub> | Sound Control Register (high-order)          | SGCR         | R/W    |                                         | 0_____0 <sub>B</sub>  |

(Continued)

# MB90590/590G Series

| Address                            | Register                                                                      | Abbreviation | Access | Peripheral                       | Initial value                |
|------------------------------------|-------------------------------------------------------------------------------|--------------|--------|----------------------------------|------------------------------|
| 60 <sub>H</sub>                    | Watch Timer Control Register (low-order)                                      | WTCR         | R/W    | Watch Timer                      | 0 0 0 _ _ 0 0 0 <sub>B</sub> |
| 61 <sub>H</sub>                    | Watch Timer Control Register (high-order)                                     | WTCR         | R/W    |                                  | 0 0 0 0 0 0 0 0 <sub>B</sub> |
| 62 <sub>H</sub>                    | PWM Control Register 0                                                        | PWC0         | R/W    | Stepping Motor Controller 0      | 0 0 0 0 0 _ _ 0 <sub>B</sub> |
| 63 <sub>H</sub>                    | Reserved                                                                      |              |        |                                  |                              |
| 64 <sub>H</sub>                    | PWM Control Register 1                                                        | PWC1         | R/W    | Stepping Motor Controller 1      | 0 0 0 0 0 _ _ 0 <sub>B</sub> |
| 65 <sub>H</sub>                    | Reserved                                                                      |              |        |                                  |                              |
| 66 <sub>H</sub>                    | PWM Control Register 2                                                        | PWC2         | R/W    | Stepping Motor Controller 2      | 0 0 0 0 0 _ _ 0 <sub>B</sub> |
| 67 <sub>H</sub>                    | Reserved                                                                      |              |        |                                  |                              |
| 68 <sub>H</sub>                    | PWM Control Register 3                                                        | PWC3         | R/W    | Stepping Motor Controller 3      | 0 0 0 0 0 _ _ 0 <sub>B</sub> |
| 69 <sub>H</sub> to 6C <sub>H</sub> | Reserved                                                                      |              |        |                                  |                              |
| 6D <sub>H</sub>                    | Serial IO Prescaler Register                                                  | CDCR         | R/W    | Prescaler (Serial IO)            | 0 XXX 1 1 1 1 <sub>B</sub>   |
| 6E <sub>H</sub>                    | Timer Control Status Register                                                 | TCCS         | R/W    | I/O Timer                        | 0 0 0 0 0 0 0 0 <sub>B</sub> |
| 6F <sub>H</sub>                    | ROM Mirror Function Select Register                                           | ROMM         | W      | ROM Mirror                       | XXXXXXXX1 <sub>B</sub>       |
| 70 <sub>H</sub> to 8F <sub>H</sub> | Reserved for CAN Interface 0/1. Refer to section about CAN Controller         |              |        |                                  |                              |
| 90 <sub>H</sub> to 9D <sub>H</sub> | Reserved                                                                      |              |        |                                  |                              |
| 9E <sub>H</sub>                    | Program Address Detection Control Status Register                             | PACSR        | R/W    | Address Match Detection Function | 0 0 0 0 0 0 0 0 <sub>B</sub> |
| 9F <sub>H</sub>                    | Delayed Interrupt/Release Register                                            | DIRR         | R/W    | Delayed Interrupt                | _ _ _ _ _ _ _ 0 <sub>B</sub> |
| A0 <sub>H</sub>                    | Low Power Mode Control Register                                               | LPMCR        | R/W    | Low Power Controller             | 0 0 0 1 1 0 0 0 <sub>B</sub> |
| A1 <sub>H</sub>                    | Clock Selection Register                                                      | CKSCR        | R/W    | Low Power Controller             | 1 1 1 1 1 1 0 0 <sub>B</sub> |
| A2 <sub>H</sub> to A7 <sub>H</sub> | Reserved                                                                      |              |        |                                  |                              |
| A8 <sub>H</sub>                    | Watchdog Timer Control Register                                               | WDTC         | R/W    | Watchdog Timer                   | XXXXX 1 1 1 <sub>B</sub>     |
| A9 <sub>H</sub>                    | Time Base Timer Control Register                                              | TBTC         | R/W    | Time Base Timer                  | 1 - - 0 0 1 0 0 <sub>B</sub> |
| AA <sub>H</sub> to AD <sub>H</sub> | Reserved                                                                      |              |        |                                  |                              |
| AE <sub>H</sub>                    | Flash Memory Control Status Register (Flash product only. Otherwise reserved) | FMCS         | R/W    | Flash Memory                     | 0 0 0 X 0 0 0 0 <sub>B</sub> |
| AF <sub>H</sub>                    | Reserved                                                                      |              |        |                                  |                              |

(Continued)

# MB90590/590G Series

| Address                               | Register                      | Abbreviation | Access | Peripheral                                    | Initial value                |
|---------------------------------------|-------------------------------|--------------|--------|-----------------------------------------------|------------------------------|
| B0 <sub>H</sub>                       | Interrupt Control Register 00 | ICR00        | R/W    | Interrupt controller                          | 0 0 0 0 0 1 1 1 <sub>B</sub> |
| B1 <sub>H</sub>                       | Interrupt Control Register 01 | ICR01        | R/W    |                                               | 0 0 0 0 0 1 1 1 <sub>B</sub> |
| B2 <sub>H</sub>                       | Interrupt Control Register 02 | ICR02        | R/W    |                                               | 0 0 0 0 0 1 1 1 <sub>B</sub> |
| B3 <sub>H</sub>                       | Interrupt Control Register 03 | ICR03        | R/W    |                                               | 0 0 0 0 0 1 1 1 <sub>B</sub> |
| B4 <sub>H</sub>                       | Interrupt Control Register 04 | ICR04        | R/W    |                                               | 0 0 0 0 0 1 1 1 <sub>B</sub> |
| B5 <sub>H</sub>                       | Interrupt Control Register 05 | ICR05        | R/W    |                                               | 0 0 0 0 0 1 1 1 <sub>B</sub> |
| B6 <sub>H</sub>                       | Interrupt Control Register 06 | ICR06        | R/W    |                                               | 0 0 0 0 0 1 1 1 <sub>B</sub> |
| B7 <sub>H</sub>                       | Interrupt Control Register 07 | ICR07        | R/W    |                                               | 0 0 0 0 0 1 1 1 <sub>B</sub> |
| B8 <sub>H</sub>                       | Interrupt Control Register 08 | ICR08        | R/W    |                                               | 0 0 0 0 0 1 1 1 <sub>B</sub> |
| B9 <sub>H</sub>                       | Interrupt Control Register 09 | ICR09        | R/W    |                                               | 0 0 0 0 0 1 1 1 <sub>B</sub> |
| BA <sub>H</sub>                       | Interrupt Control Register 10 | ICR10        | R/W    |                                               | 0 0 0 0 0 1 1 1 <sub>B</sub> |
| BB <sub>H</sub>                       | Interrupt Control Register 11 | ICR11        | R/W    |                                               | 0 0 0 0 0 1 1 1 <sub>B</sub> |
| BC <sub>H</sub>                       | Interrupt Control Register 12 | ICR12        | R/W    |                                               | 0 0 0 0 0 1 1 1 <sub>B</sub> |
| BD <sub>H</sub>                       | Interrupt Control Register 13 | ICR13        | R/W    |                                               | 0 0 0 0 0 1 1 1 <sub>B</sub> |
| BE <sub>H</sub>                       | Interrupt Control Register 14 | ICR14        | R/W    |                                               | 0 0 0 0 0 1 1 1 <sub>B</sub> |
| BF <sub>H</sub>                       | Interrupt Control Register 15 | ICR15        | R/W    |                                               | 0 0 0 0 0 1 1 1 <sub>B</sub> |
| C0 <sub>H</sub> to<br>FF <sub>H</sub> | Reserved                      |              |        |                                               |                              |
| 1900 <sub>H</sub>                     | Reload L Register             | PRLLO        | R/W    | 16-bit Programmable<br>Pulse<br>Generator 0/1 | XXXXXXXX <sub>B</sub>        |
| 1901 <sub>H</sub>                     | Reload H Register             | PRLH0        | R/W    |                                               | XXXXXXXX <sub>B</sub>        |
| 1902 <sub>H</sub>                     | Reload L Register             | PRLLO1       | R/W    |                                               | XXXXXXXX <sub>B</sub>        |
| 1903 <sub>H</sub>                     | Reload H Register             | PRLH1        | R/W    |                                               | XXXXXXXX <sub>B</sub>        |
| 1904 <sub>H</sub>                     | Reload L Register             | PRLLO2       | R/W    | 16-bit Programmable<br>Pulse<br>Generator 2/3 | XXXXXXXX <sub>B</sub>        |
| 1905 <sub>H</sub>                     | Reload H Register             | PRLH2        | R/W    |                                               | XXXXXXXX <sub>B</sub>        |
| 1906 <sub>H</sub>                     | Reload L Register             | PRLLO3       | R/W    |                                               | XXXXXXXX <sub>B</sub>        |
| 1907 <sub>H</sub>                     | Reload H Register             | PRLH3        | R/W    |                                               | XXXXXXXX <sub>B</sub>        |
| 1908 <sub>H</sub>                     | Reload L Register             | PRLLO4       | R/W    | 16-bit Programmable<br>Pulse<br>Generator 4/5 | XXXXXXXX <sub>B</sub>        |
| 1909 <sub>H</sub>                     | Reload H Register             | PRLH4        | R/W    |                                               | XXXXXXXX <sub>B</sub>        |
| 190A <sub>H</sub>                     | Reload L Register             | PRLLO5       | R/W    |                                               | XXXXXXXX <sub>B</sub>        |
| 190B <sub>H</sub>                     | Reload H Register             | PRLH5        | R/W    |                                               | XXXXXXXX <sub>B</sub>        |
| 190C <sub>H</sub>                     | Reload L Register             | PRLLO6       | R/W    | 16-bit Programmable<br>Pulse<br>Generator 6/7 | XXXXXXXX <sub>B</sub>        |
| 190D <sub>H</sub>                     | Reload H Register             | PRLH6        | R/W    |                                               | XXXXXXXX <sub>B</sub>        |
| 190E <sub>H</sub>                     | Reload L Register             | PRLLO7       | R/W    |                                               | XXXXXXXX <sub>B</sub>        |
| 190F <sub>H</sub>                     | Reload H Register             | PRLH7        | R/W    |                                               | XXXXXXXX <sub>B</sub>        |

(Continued)

# MB90590/590G Series

| Address                                | Register                              | Abbreviation | Access | Peripheral                              | Initial value         |
|----------------------------------------|---------------------------------------|--------------|--------|-----------------------------------------|-----------------------|
| 1910 <sub>H</sub>                      | Reload L Register                     | PRLL8        | R/W    | 16-bit Programmable Pulse Generator 8/9 | XXXXXXXX <sub>B</sub> |
| 1911 <sub>H</sub>                      | Reload H Register                     | PRLH8        | R/W    |                                         | XXXXXXXX <sub>B</sub> |
| 1912 <sub>H</sub>                      | Reload L Register                     | PRLL9        | R/W    |                                         | XXXXXXXX <sub>B</sub> |
| 1913 <sub>H</sub>                      | Reload H Register                     | PRLH9        | R/W    |                                         | XXXXXXXX <sub>B</sub> |
| 1914 <sub>H</sub>                      | Reload L Register                     | PRLLA        | R/W    | 16-bit Programmable Pulse Generator A/B | XXXXXXXX <sub>B</sub> |
| 1915 <sub>H</sub>                      | Reload H Register                     | PRLHA        | R/W    |                                         | XXXXXXXX <sub>B</sub> |
| 1916 <sub>H</sub>                      | Reload L Register                     | PRLLB        | R/W    |                                         | XXXXXXXX <sub>B</sub> |
| 1917 <sub>H</sub>                      | Reload H Register                     | PRLHB        | R/W    |                                         | XXXXXXXX <sub>B</sub> |
| 1918 <sub>H</sub> to 191F <sub>H</sub> | Reserved                              |              |        |                                         |                       |
| 1920 <sub>H</sub>                      | Input Capture Register 0 (low-order)  | IPCP0        | R      | Input Capture 0/1                       | XXXXXXXX <sub>B</sub> |
| 1921 <sub>H</sub>                      | Input Capture Register 0 (high-order) | IPCP0        | R      |                                         | XXXXXXXX <sub>B</sub> |
| 1922 <sub>H</sub>                      | Input Capture Register 1 (low-order)  | IPCP1        | R      |                                         | XXXXXXXX <sub>B</sub> |
| 1923 <sub>H</sub>                      | Input Capture Register 1 (high-order) | IPCP1        | R      |                                         | XXXXXXXX <sub>B</sub> |
| 1924 <sub>H</sub>                      | Input Capture Register 2 (low-order)  | IPCP2        | R      | Input Capture 2/3                       | XXXXXXXX <sub>B</sub> |
| 1925 <sub>H</sub>                      | Input Capture Register 2 (high-order) | IPCP2        | R      |                                         | XXXXXXXX <sub>B</sub> |
| 1926 <sub>H</sub>                      | Input Capture Register 3 (low-order)  | IPCP3        | R      |                                         | XXXXXXXX <sub>B</sub> |
| 1927 <sub>H</sub>                      | Input Capture Register 3 (high-order) | IPCP3        | R      |                                         | XXXXXXXX <sub>B</sub> |
| 1928 <sub>H</sub>                      | Input Capture Register 4 (low-order)  | IPCP4        | R      | Input Capture 4/5                       | XXXXXXXX <sub>B</sub> |
| 1929 <sub>H</sub>                      | Input Capture Register 4 (high-order) | IPCP4        | R      |                                         | XXXXXXXX <sub>B</sub> |
| 192A <sub>H</sub>                      | Input Capture Register 5 (low-order)  | IPCP5        | R      |                                         | XXXXXXXX <sub>B</sub> |
| 192B <sub>H</sub>                      | Input Capture Register 5 (high-order) | IPCP5        | R      |                                         | XXXXXXXX <sub>B</sub> |
| 192C <sub>H</sub> to 192F <sub>H</sub> | Reserved                              |              |        |                                         |                       |

(Continued)

# MB90590/590G Series

| Address                                | Register                               | Abbreviation | Access | Peripheral            | Initial value              |
|----------------------------------------|----------------------------------------|--------------|--------|-----------------------|----------------------------|
| 1930 <sub>H</sub>                      | Output Compare Register 0 (low-order)  | OCCP0        | R/W    | Output Compare 0/1    | XXXXXXXX <sub>B</sub>      |
| 1931 <sub>H</sub>                      | Output Compare Register 0 (high-order) | OCCP0        | R/W    |                       | XXXXXXXX <sub>B</sub>      |
| 1932 <sub>H</sub>                      | Output Compare Register 1 (low-order)  | OCCP1        | R/W    |                       | XXXXXXXX <sub>B</sub>      |
| 1933 <sub>H</sub>                      | Output Compare Register 1 (high-order) | OCCP1        | R/W    |                       | XXXXXXXX <sub>B</sub>      |
| 1934 <sub>H</sub>                      | Output Compare Register 2 (low-order)  | OCCP2        | R/W    | Output Compare 2/3    | XXXXXXXX <sub>B</sub>      |
| 1935 <sub>H</sub>                      | Output Compare Register 2 (high-order) | OCCP2        | R/W    |                       | XXXXXXXX <sub>B</sub>      |
| 1936 <sub>H</sub>                      | Output Compare Register 3 (low-order)  | OCCP3        | R/W    |                       | XXXXXXXX <sub>B</sub>      |
| 1937 <sub>H</sub>                      | Output Compare Register 3 (high-order) | OCCP3        | R/W    |                       | XXXXXXXX <sub>B</sub>      |
| 1938 <sub>H</sub>                      | Output Compare Register 4 (low-order)  | OCCP4        | R/W    | Output Compare 4/5    | XXXXXXXX <sub>B</sub>      |
| 1939 <sub>H</sub>                      | Output Compare Register 4 (high-order) | OCCP4        | R/W    |                       | XXXXXXXX <sub>B</sub>      |
| 193A <sub>H</sub>                      | Output Compare Register 5 (low-order)  | OCCP5        | R/W    |                       | XXXXXXXX <sub>B</sub>      |
| 193B <sub>H</sub>                      | Output Compare Register 5 (high-order) | OCCP5        | R/W    |                       | XXXXXXXX <sub>B</sub>      |
| 193C <sub>H</sub> to 193F <sub>H</sub> | Reserved                               |              |        |                       |                            |
| 1940 <sub>H</sub>                      | Timer 0/Reload Register 0 (low-order)  | TMR0/ TMRLR0 | R/W    | 16-bit Reload Timer 0 | XXXXXXXX <sub>B</sub>      |
| 1941 <sub>H</sub>                      | Timer 0/Reload Register 0 (high-order) | TMR0/ TMRLR0 | R/W    |                       | XXXXXXXX <sub>B</sub>      |
| 1942 <sub>H</sub>                      | Timer 1/Reload Register 1 (low-order)  | TMR1/ TMRLR1 | R/W    | 16-bit Reload Timer 1 | XXXXXXXX <sub>B</sub>      |
| 1943 <sub>H</sub>                      | Timer 1/Reload Register 1 (high-order) | TMR1/ TMRLR1 | R/W    |                       | XXXXXXXX <sub>B</sub>      |
| 1944 <sub>H</sub>                      | Timer Data Register (low-order)        | TCDT         | R/W    | IO Timer              | 0 0 0 0 0 0 0 <sub>B</sub> |
| 1945 <sub>H</sub>                      | Timer Data Register (high-order)       | TCDT         | R/W    |                       | 0 0 0 0 0 0 0 <sub>B</sub> |
| 1946 <sub>H</sub>                      | Frequency Data Register                | SGFR         | R/W    | Sound Generator       | XXXXXXXX <sub>B</sub>      |
| 1947 <sub>H</sub>                      | Amplitude Data Register                | SGAR         | R/W    |                       | XXXXXXXX <sub>B</sub>      |
| 1948 <sub>H</sub>                      | Decrement Grade Register               | SGDR         | R/W    |                       | XXXXXXXX <sub>B</sub>      |
| 1949 <sub>H</sub>                      | Tone Count Register                    | SGTR         | R/W    |                       | XXXXXXXX <sub>B</sub>      |

(Continued)

# MB90590/590G Series

| Address                                | Register                                                            | Abbreviation | Access | Peripheral                  | Initial value         |
|----------------------------------------|---------------------------------------------------------------------|--------------|--------|-----------------------------|-----------------------|
| 194A <sub>H</sub>                      | Sub-second Data Register (low-order)                                | WTBR         | R/W    | Watch Timer                 | XXXXXXXX <sub>B</sub> |
| 194B <sub>H</sub>                      | Sub-second Data Register (middle-order)                             | WTBR         | R/W    |                             | XXXXXXXX <sub>B</sub> |
| 194C <sub>H</sub>                      | Sub-second Data Register (high-order)                               | WTBR         | R/W    |                             | ___XXXX <sub>B</sub>  |
| 194D <sub>H</sub>                      | Second Data Register                                                | WTSR         | R/W    |                             | __000000 <sub>B</sub> |
| 194E <sub>H</sub>                      | Minute Data Register                                                | WTMR         | R/W    | Watch Timer                 | __000000 <sub>B</sub> |
| 194F <sub>H</sub>                      | Hour Data Register                                                  | WTHR         | R/W    |                             | ___00000 <sub>B</sub> |
| 1950 <sub>H</sub>                      | PWM1 Compare Register 0                                             | PWC10        | R/W    | Stepping Motor Controller 0 | XXXXXXXX <sub>B</sub> |
| 1951 <sub>H</sub>                      | PWM2 Compare Register 0                                             | PWC20        | R/W    |                             | XXXXXXXX <sub>B</sub> |
| 1952 <sub>H</sub>                      | PWM1 Select Register 0                                              | PWS10        | R/W    |                             | __000000 <sub>B</sub> |
| 1953 <sub>H</sub>                      | PWM2 Select Register 0                                              | PWS20        | R/W    |                             | _0000000 <sub>B</sub> |
| 1954 <sub>H</sub>                      | PWM1 Compare Register 1                                             | PWC11        | R/W    | Stepping Motor Controller 1 | XXXXXXXX <sub>B</sub> |
| 1955 <sub>H</sub>                      | PWM2 Compare Register 1                                             | PWC21        | R/W    |                             | XXXXXXXX <sub>B</sub> |
| 1956 <sub>H</sub>                      | PWM1 Select Register 1                                              | PWS11        | R/W    |                             | __000000 <sub>B</sub> |
| 1957 <sub>H</sub>                      | PWM2 Select Register 1                                              | PWS21        | R/W    |                             | _0000000 <sub>B</sub> |
| 1958 <sub>H</sub>                      | PWM1 Compare Register 2                                             | PWC12        | R/W    | Stepping Motor Controller 2 | XXXXXXXX <sub>B</sub> |
| 1959 <sub>H</sub>                      | PWM2 Compare Register 2                                             | PWC22        | R/W    |                             | XXXXXXXX <sub>B</sub> |
| 195A <sub>H</sub>                      | PWM1 Select Register 2                                              | PWS12        | R/W    |                             | __000000 <sub>B</sub> |
| 195B <sub>H</sub>                      | PWM2 Select Register 2                                              | PWS22        | R/W    |                             | _0000000 <sub>B</sub> |
| 195C <sub>H</sub>                      | PWM1 Compare Register 3                                             | PWC13        | R/W    | Stepping Motor Controller 3 | XXXXXXXX <sub>B</sub> |
| 195D <sub>H</sub>                      | PWM2 Compare Register 3                                             | PWC23        | R/W    |                             | XXXXXXXX <sub>B</sub> |
| 195E <sub>H</sub>                      | PWM1 Select Register 3                                              | PWS13        | R/W    |                             | __000000 <sub>B</sub> |
| 195F <sub>H</sub>                      | PWM2 Select Register 3                                              | PWS23        | R/W    |                             | _0000000 <sub>B</sub> |
| 1960 <sub>H</sub> to 19FF <sub>H</sub> | Reserved                                                            |              |        |                             |                       |
| 1A00 <sub>H</sub> to 1AFF <sub>H</sub> | Reserved for CAN Interface 0. Refer to section about CAN Controller |              |        |                             |                       |
| 1B00 <sub>H</sub> to 1BFF <sub>H</sub> | Reserved for CAN Interface 1. Refer to section about CAN Controller |              |        |                             |                       |
| 1C00 <sub>H</sub> to 1CFF <sub>H</sub> | Reserved for CAN Interface 0. Refer to section about CAN Controller |              |        |                             |                       |
| 1D00 <sub>H</sub> to 1DFF <sub>H</sub> | Reserved for CAN Interface 1. Refer to section about CAN Controller |              |        |                             |                       |
| 1E00 <sub>H</sub> to 1EFF <sub>H</sub> | Reserved                                                            |              |        |                             |                       |

(Continued)

(Continued)

| Address                                | Register                                            | Abbreviation | Access | Peripheral                       | Initial value         |
|----------------------------------------|-----------------------------------------------------|--------------|--------|----------------------------------|-----------------------|
| 1FF0 <sub>H</sub>                      | Program Address Detection Register 0 (low-order)    | PADR0        | R/W    | Address Match Detection Function | XXXXXXXX <sub>B</sub> |
| 1FF1 <sub>H</sub>                      | Program Address Detection Register 0 (middle-order) | PADR0        | R/W    |                                  | XXXXXXXX <sub>B</sub> |
| 1FF2 <sub>H</sub>                      | Program Address Detection Register 0 (high-order)   | PADR0        | R/W    |                                  | XXXXXXXX <sub>B</sub> |
| 1FF3 <sub>H</sub>                      | Program Address Detection Register 1 (low-order)    | PADR1        | R/W    |                                  | XXXXXXXX <sub>B</sub> |
| 1FF4 <sub>H</sub>                      | Program Address Detection Register 1 (middle-order) | PADR1        | R/W    |                                  | XXXXXXXX <sub>B</sub> |
| 1FF5 <sub>H</sub>                      | Program Address Detection Register 1 (high-order)   | PADR1        | R/W    |                                  | XXXXXXXX <sub>B</sub> |
| 1FF6 <sub>H</sub> to 1FFF <sub>H</sub> | Reserved                                            |              |        |                                  |                       |

Note: Initial value of “\_” represents unused bit; “X” represents unknown value.

Addresses in the range 0000<sub>H</sub> to 00FF<sub>H</sub>, which are not listed in the table, are reserved for the primary functions of the MCU. A read access to these reserved addresses results in reading “X”, and any write access should not be performed.

# MB90590/590G Series

## ■ CAN CONTROLLERS

The CAN controller has the following features:

- Conforms to CAN Specification Version 2.0 Part A and B
  - Supports transmission/reception in standard frame and extended frame formats
- Supports transmission of data frames by receiving remote frames
- 16 transmitting/receiving message buffers
  - 29-bit ID and 8-byte data
  - Multi-level message buffer configuration
- Provides full-bit comparison, full-bit mask, acceptance register 0/acceptance register 1 for each message buffer as 1D acceptance mask
  - Two acceptance mask registers in either standard frame format or extended frame formats
- Bit rate programmable from 10 kbit/s to 2 Mbit/s (when input clock is at 16 MHz)

**List of Control Registers**

| Address             |                     | Register                          | Abbreviation | Access | Initial Value                  |
|---------------------|---------------------|-----------------------------------|--------------|--------|--------------------------------|
| CAN0                | CAN1                |                                   |              |        |                                |
| 000070 <sub>H</sub> | 000080 <sub>H</sub> | Message buffer valid register     | BVALR        | R/W    | 00000000 00000000 <sub>B</sub> |
| 000071 <sub>H</sub> | 000081 <sub>H</sub> |                                   |              |        |                                |
| 000072 <sub>H</sub> | 000082 <sub>H</sub> | Transmit request register         | TREQR        | R/W    | 00000000 00000000 <sub>B</sub> |
| 000073 <sub>H</sub> | 000083 <sub>H</sub> |                                   |              |        |                                |
| 000074 <sub>H</sub> | 000084 <sub>H</sub> | Transmit cancel register          | TCANR        | W      | 00000000 00000000 <sub>B</sub> |
| 000075 <sub>H</sub> | 000085 <sub>H</sub> |                                   |              |        |                                |
| 000076 <sub>H</sub> | 000086 <sub>H</sub> | Transmit complete register        | TCR          | R/W    | 00000000 00000000 <sub>B</sub> |
| 000077 <sub>H</sub> | 000087 <sub>H</sub> |                                   |              |        |                                |
| 000078 <sub>H</sub> | 000088 <sub>H</sub> | Receive complete register         | RCR          | R/W    | 00000000 00000000 <sub>B</sub> |
| 000079 <sub>H</sub> | 000089 <sub>H</sub> |                                   |              |        |                                |
| 00007A <sub>H</sub> | 00008A <sub>H</sub> | Remote request receiving register | RRTRR        | R/W    | 00000000 00000000 <sub>B</sub> |
| 00007B <sub>H</sub> | 00008B <sub>H</sub> |                                   |              |        |                                |
| 00007C <sub>H</sub> | 00008C <sub>H</sub> | Receive overrun register          | ROVRR        | R/W    | 00000000 00000000 <sub>B</sub> |
| 00007D <sub>H</sub> | 00008D <sub>H</sub> |                                   |              |        |                                |
| 00007E <sub>H</sub> | 00008E <sub>H</sub> | Receive interrupt enable register | RIER         | R/W    | 00000000 00000000 <sub>B</sub> |
| 00007F <sub>H</sub> | 00008F <sub>H</sub> |                                   |              |        |                                |

# MB90590/590G Series

List of Control Registers

| Address             |                     | Register                              | Abbreviation | Access | Initial Value                     |
|---------------------|---------------------|---------------------------------------|--------------|--------|-----------------------------------|
| CAN0                | CAN1                |                                       |              |        |                                   |
| 001C00 <sub>H</sub> | 001D00 <sub>H</sub> | Control status register               | CSR          | R/W, R | 00---000 0---0-1 <sub>B</sub>     |
| 001C01 <sub>H</sub> | 001D01 <sub>H</sub> |                                       |              |        |                                   |
| 001C02 <sub>H</sub> | 001D02 <sub>H</sub> | Last event indicator register         | LEIR         | R/W    | ----- 000-0000 <sub>B</sub>       |
| 001C03 <sub>H</sub> | 001D03 <sub>H</sub> |                                       |              |        |                                   |
| 001C04 <sub>H</sub> | 001D04 <sub>H</sub> | Receive/transmit error counter        | RTEC         | R      | 00000000 00000000 <sub>B</sub>    |
| 001C05 <sub>H</sub> | 001D05 <sub>H</sub> |                                       |              |        |                                   |
| 001C06 <sub>H</sub> | 001D06 <sub>H</sub> | Bit timing register                   | BTR          | R/W    | -1111111 11111111 <sub>B</sub>    |
| 001C07 <sub>H</sub> | 001D07 <sub>H</sub> |                                       |              |        |                                   |
| 001C08 <sub>H</sub> | 001D08 <sub>H</sub> | IDE register                          | IDER         | R/W    | XXXXXXXX<br>XXXXXXXX <sub>B</sub> |
| 001C09 <sub>H</sub> | 001D09 <sub>H</sub> |                                       |              |        |                                   |
| 001C0A <sub>H</sub> | 001D0A <sub>H</sub> | Transmit RTR register                 | TRTRR        | R/W    | 00000000 00000000 <sub>B</sub>    |
| 001C0B <sub>H</sub> | 001D0B <sub>H</sub> |                                       |              |        |                                   |
| 001C0C <sub>H</sub> | 001D0C <sub>H</sub> | Remote frame receive waiting register | RFWTR        | R/W    | XXXXXXXX<br>XXXXXXXX <sub>B</sub> |
| 001C0D <sub>H</sub> | 001D0D <sub>H</sub> |                                       |              |        |                                   |
| 001C0E <sub>H</sub> | 001D0E <sub>H</sub> | Transmit interrupt enable register    | TIER         | R/W    | 00000000 00000000 <sub>B</sub>    |
| 001C0F <sub>H</sub> | 001D0F <sub>H</sub> |                                       |              |        |                                   |
| 001C10 <sub>H</sub> | 001D10 <sub>H</sub> | Acceptance mask select register       | AMSR         | R/W    | XXXXXXXX<br>XXXXXXXX <sub>B</sub> |
| 001C11 <sub>H</sub> | 001D11 <sub>H</sub> |                                       |              |        |                                   |
| 001C12 <sub>H</sub> | 001D12 <sub>H</sub> |                                       |              |        | XXXXXXXX<br>XXXXXXXX <sub>B</sub> |
| 001C13 <sub>H</sub> | 001D13 <sub>H</sub> | Acceptance mask register 0            | AMR0         | R/W    | XXXXXXXX<br>XXXXXXXX <sub>B</sub> |
| 001C14 <sub>H</sub> | 001D14 <sub>H</sub> |                                       |              |        | XXXXX--- XXXXXXXX <sub>B</sub>    |
| 001C15 <sub>H</sub> | 001D15 <sub>H</sub> |                                       |              |        |                                   |
| 001C16 <sub>H</sub> | 001D16 <sub>H</sub> |                                       |              |        |                                   |
| 001C17 <sub>H</sub> | 001D17 <sub>H</sub> | Acceptance mask register 1            | AMR1         | R/W    | XXXXXXXX<br>XXXXXXXX <sub>B</sub> |
| 001C18 <sub>H</sub> | 001D18 <sub>H</sub> |                                       |              |        | XXXXX--- XXXXXXXX <sub>B</sub>    |
| 001C19 <sub>H</sub> | 001D19 <sub>H</sub> |                                       |              |        |                                   |
| 001C1A <sub>H</sub> | 001D1A <sub>H</sub> |                                       |              |        |                                   |
| 001C1B <sub>H</sub> | 001D1B <sub>H</sub> |                                       |              |        | XXXXX--- XXXXXXXX <sub>B</sub>    |

# MB90590/590G Series

**List of Message Buffers (ID Registers)**

| Address             |                     | Register      | Abbreviation | Access | Initial Value                  |
|---------------------|---------------------|---------------|--------------|--------|--------------------------------|
| CAN0                | CAN1                |               |              |        |                                |
| 001A20 <sub>H</sub> | 001B20 <sub>H</sub> | ID register 0 | IDR0         | R/W    | XXXXXXXX XXXXXXXX <sub>B</sub> |
| 001A21 <sub>H</sub> | 001B21 <sub>H</sub> |               |              |        |                                |
| 001A22 <sub>H</sub> | 001B22 <sub>H</sub> |               |              |        | XXXXX--- XXXXXXXX <sub>B</sub> |
| 001A23 <sub>H</sub> | 001B23 <sub>H</sub> |               |              |        |                                |
| 001A24 <sub>H</sub> | 001B24 <sub>H</sub> | ID register 1 | IDR1         | R/W    | XXXXXXXX XXXXXXXX <sub>B</sub> |
| 001A25 <sub>H</sub> | 001B25 <sub>H</sub> |               |              |        |                                |
| 001A26 <sub>H</sub> | 001B26 <sub>H</sub> |               |              |        | XXXXX--- XXXXXXXX <sub>B</sub> |
| 001A27 <sub>H</sub> | 001B27 <sub>H</sub> |               |              |        |                                |
| 001A28 <sub>H</sub> | 001B28 <sub>H</sub> | ID register 2 | IDR2         | R/W    | XXXXXXXX XXXXXXXX <sub>B</sub> |
| 001A29 <sub>H</sub> | 001B29 <sub>H</sub> |               |              |        |                                |
| 001A2A <sub>H</sub> | 001B2A <sub>H</sub> |               |              |        | XXXXX--- XXXXXXXX <sub>B</sub> |
| 001A2B <sub>H</sub> | 001B2B <sub>H</sub> |               |              |        |                                |
| 001A2C <sub>H</sub> | 001B2C <sub>H</sub> | ID register 3 | IDR3         | R/W    | XXXXXXXX XXXXXXXX <sub>B</sub> |
| 001A2D <sub>H</sub> | 001B2D <sub>H</sub> |               |              |        |                                |
| 001A2E <sub>H</sub> | 001B2E <sub>H</sub> |               |              |        | XXXXX--- XXXXXXXX <sub>B</sub> |
| 001A2F <sub>H</sub> | 001B2F <sub>H</sub> |               |              |        |                                |
| 001A30 <sub>H</sub> | 001B30 <sub>H</sub> | ID register 4 | IDR4         | R/W    | XXXXXXXX XXXXXXXX <sub>B</sub> |
| 001A31 <sub>H</sub> | 001B31 <sub>H</sub> |               |              |        |                                |
| 001A32 <sub>H</sub> | 001B32 <sub>H</sub> |               |              |        | XXXXX--- XXXXXXXX <sub>B</sub> |
| 001A33 <sub>H</sub> | 001B33 <sub>H</sub> |               |              |        |                                |
| 001A34 <sub>H</sub> | 001B34 <sub>H</sub> | ID register 5 | IDR5         | R/W    | XXXXXXXX XXXXXXXX <sub>B</sub> |
| 001A35 <sub>H</sub> | 001B35 <sub>H</sub> |               |              |        |                                |
| 001A36 <sub>H</sub> | 001B36 <sub>H</sub> |               |              |        | XXXXX--- XXXXXXXX <sub>B</sub> |
| 001A37 <sub>H</sub> | 001B37 <sub>H</sub> |               |              |        |                                |
| 001A38 <sub>H</sub> | 001B38 <sub>H</sub> | ID register 6 | IDR6         | R/W    | XXXXXXXX XXXXXXXX <sub>B</sub> |
| 001A39 <sub>H</sub> | 001B39 <sub>H</sub> |               |              |        |                                |
| 001A3A <sub>H</sub> | 001B3A <sub>H</sub> |               |              |        | XXXXX--- XXXXXXXX <sub>B</sub> |
| 001A3B <sub>H</sub> | 001B3B <sub>H</sub> |               |              |        |                                |
| 001A3C <sub>H</sub> | 001B3C <sub>H</sub> | ID register 7 | IDR7         | R/W    | XXXXXXXX XXXXXXXX <sub>B</sub> |
| 001A3D <sub>H</sub> | 001B3D <sub>H</sub> |               |              |        |                                |
| 001A3E <sub>H</sub> | 001B3E <sub>H</sub> |               |              |        | XXXXX--- XXXXXXXX <sub>B</sub> |
| 001A3F <sub>H</sub> | 001B3F <sub>H</sub> |               |              |        |                                |

(Continued)

# MB90590/590G Series

(Continued)

| Address             |                     | Register       | Abbreviation | Access | Initial Value                  |
|---------------------|---------------------|----------------|--------------|--------|--------------------------------|
| CAN0                | CAN1                |                |              |        |                                |
| 001A40 <sub>H</sub> | 001B40 <sub>H</sub> | ID register 8  | IDR8         | R/W    | XXXXXXXX XXXXXXXX <sub>B</sub> |
| 001A41 <sub>H</sub> | 001B41 <sub>H</sub> |                |              |        |                                |
| 001A42 <sub>H</sub> | 001B42 <sub>H</sub> |                |              |        | XXXXX--- XXXXXXXX <sub>B</sub> |
| 001A43 <sub>F</sub> | 001B43 <sub>H</sub> |                |              |        |                                |
| 001A44 <sub>H</sub> | 001B44 <sub>H</sub> | ID register 9  | IDR9         | R/W    | XXXXXXXX XXXXXXXX <sub>B</sub> |
| 001A45 <sub>H</sub> | 001B45 <sub>H</sub> |                |              |        |                                |
| 001A46 <sub>H</sub> | 001B46 <sub>H</sub> |                |              |        | XXXXX--- XXXXXXXX <sub>B</sub> |
| 001A47 <sub>H</sub> | 001B47 <sub>H</sub> |                |              |        |                                |
| 001A48 <sub>H</sub> | 001B48 <sub>H</sub> | ID register 10 | IDR10        | R/W    | XXXXXXXX XXXXXXXX <sub>B</sub> |
| 001A49 <sub>H</sub> | 001B49 <sub>H</sub> |                |              |        |                                |
| 001A4A <sub>H</sub> | 001B4A <sub>H</sub> |                |              |        | XXXXX--- XXXXXXXX <sub>B</sub> |
| 001A4B <sub>H</sub> | 001B4B <sub>H</sub> |                |              |        |                                |
| 001A4C <sub>H</sub> | 001B4C <sub>H</sub> | ID register 11 | IDR11        | R/W    | XXXXXXXX XXXXXXXX <sub>B</sub> |
| 001A4D <sub>H</sub> | 001B4D <sub>H</sub> |                |              |        |                                |
| 001A4E <sub>H</sub> | 001B4E <sub>H</sub> |                |              |        | XXXXX--- XXXXXXXX <sub>B</sub> |
| 001A4F <sub>H</sub> | 001B4F <sub>H</sub> |                |              |        |                                |
| 001A50 <sub>H</sub> | 001B50 <sub>H</sub> | ID register 12 | IDR12        | R/W    | XXXXXXXX XXXXXXXX <sub>B</sub> |
| 001A51 <sub>H</sub> | 001B51 <sub>H</sub> |                |              |        |                                |
| 001A52 <sub>H</sub> | 001B52 <sub>H</sub> |                |              |        | XXXXX--- XXXXXXXX <sub>B</sub> |
| 001A53 <sub>H</sub> | 001B53 <sub>H</sub> |                |              |        |                                |
| 001A54 <sub>H</sub> | 001B54 <sub>H</sub> | ID register 13 | IDR13        | R/W    | XXXXXXXX XXXXXXXX <sub>B</sub> |
| 001A55 <sub>H</sub> | 001B55 <sub>H</sub> |                |              |        |                                |
| 001A56 <sub>H</sub> | 001B56 <sub>H</sub> |                |              |        | XXXXX--- XXXXXXXX <sub>B</sub> |
| 001A57 <sub>H</sub> | 001B57 <sub>H</sub> |                |              |        |                                |
| 001A58 <sub>H</sub> | 001B58 <sub>H</sub> | ID register 14 | IDR14        | R/W    | XXXXXXXX XXXXXXXX <sub>B</sub> |
| 001A59 <sub>H</sub> | 001B59 <sub>H</sub> |                |              |        |                                |
| 001A5A <sub>H</sub> | 001B5A <sub>H</sub> |                |              |        | XXXXX--- XXXXXXXX <sub>B</sub> |
| 001A5B <sub>H</sub> | 001B5B <sub>H</sub> |                |              |        |                                |
| 001A5C <sub>H</sub> | 001B5C <sub>H</sub> | ID register 15 | IDR15        | R/W    | XXXXXXXX XXXXXXXX <sub>B</sub> |
| 001A5D <sub>H</sub> | 001B5D <sub>H</sub> |                |              |        |                                |
| 001A5E <sub>H</sub> | 001B5E <sub>H</sub> |                |              |        | XXXXX--- XXXXXXXX <sub>B</sub> |
| 001A5F <sub>H</sub> | 001B5F <sub>H</sub> |                |              |        |                                |

# MB90590/590G Series

**List of Message Buffers (DLC Registers and Data Registers)**

| Address                                          |                                                  | Register                  | Abbreviation | Access | Initial Value                                        |
|--------------------------------------------------|--------------------------------------------------|---------------------------|--------------|--------|------------------------------------------------------|
| CAN0                                             | CAN1                                             |                           |              |        |                                                      |
| 001A60 <sub>H</sub>                              | 001B60 <sub>H</sub>                              | DLC register 0            | DLCR0        | R/W    | ----XXXX <sub>B</sub>                                |
| 001A61 <sub>H</sub>                              | 001B61 <sub>H</sub>                              |                           |              |        |                                                      |
| 001A62 <sub>H</sub>                              | 001B62 <sub>H</sub>                              | DLC register 1            | DLCR1        | R/W    | ----XXXX <sub>B</sub>                                |
| 001A63 <sub>H</sub>                              | 001B63 <sub>H</sub>                              |                           |              |        |                                                      |
| 001A64 <sub>H</sub>                              | 001B64 <sub>H</sub>                              | DLC register 2            | DLCR2        | R/W    | ----XXXX <sub>B</sub>                                |
| 001A65 <sub>H</sub>                              | 001B65 <sub>H</sub>                              |                           |              |        |                                                      |
| 001A66 <sub>H</sub>                              | 001B66 <sub>H</sub>                              | DLC register 3            | DLCR3        | R/W    | ----XXXX <sub>B</sub>                                |
| 001A67 <sub>H</sub>                              | 001B67 <sub>H</sub>                              |                           |              |        |                                                      |
| 001A68 <sub>H</sub>                              | 001B68 <sub>H</sub>                              | DLC register 4            | DLCR4        | R/W    | ----XXXX <sub>B</sub>                                |
| 001A69 <sub>H</sub>                              | 001B69 <sub>H</sub>                              |                           |              |        |                                                      |
| 001A6A <sub>H</sub>                              | 001B6A <sub>H</sub>                              | DLC register 5            | DLCR5        | R/W    | ----XXXX <sub>B</sub>                                |
| 001A6B <sub>H</sub>                              | 001B6B <sub>H</sub>                              |                           |              |        |                                                      |
| 001A6C <sub>H</sub>                              | 001B6C <sub>H</sub>                              | DLC register 6            | DLCR6        | R/W    | ----XXXX <sub>B</sub>                                |
| 001A6D <sub>H</sub>                              | 001B6D <sub>H</sub>                              |                           |              |        |                                                      |
| 001A6E <sub>H</sub>                              | 001B6E <sub>H</sub>                              | DLC register 7            | DLCR7        | R/W    | ----XXXX <sub>B</sub>                                |
| 001A6F <sub>H</sub>                              | 001B6F <sub>H</sub>                              |                           |              |        |                                                      |
| 001A70 <sub>H</sub>                              | 001B70 <sub>H</sub>                              | DLC register 8            | DLCR8        | R/W    | ----XXXX                                             |
| 001A71 <sub>H</sub>                              | 001B71 <sub>H</sub>                              |                           |              |        |                                                      |
| 001A72 <sub>H</sub>                              | 001B72 <sub>H</sub>                              | DLC register 9            | DLCR9        | R/W    | ----XXXX <sub>B</sub>                                |
| 001A73 <sub>H</sub>                              | 001B73 <sub>H</sub>                              |                           |              |        |                                                      |
| 001A74 <sub>H</sub>                              | 001B74 <sub>H</sub>                              | DLC register 10           | DLCR10       | R/W    | ----XXXX <sub>B</sub>                                |
| 001A75 <sub>H</sub>                              | 001B75 <sub>H</sub>                              |                           |              |        |                                                      |
| 001A76 <sub>H</sub>                              | 001B76 <sub>H</sub>                              | DLC register 11           | DLCR11       | R/W    | ----XXXX <sub>B</sub>                                |
| 001A77 <sub>H</sub>                              | 001B77 <sub>H</sub>                              |                           |              |        |                                                      |
| 001A78 <sub>H</sub>                              | 001B78 <sub>H</sub>                              | DLC register 12           | DLCR12       | R/W    | ----XXXX <sub>B</sub>                                |
| 001A79 <sub>H</sub>                              | 001B79 <sub>H</sub>                              |                           |              |        |                                                      |
| 001A7A <sub>H</sub>                              | 001B7A <sub>H</sub>                              | DLC register 13           | DLCR13       | R/W    | ----XXXX <sub>B</sub>                                |
| 001A7B <sub>H</sub>                              | 001B7B <sub>H</sub>                              |                           |              |        |                                                      |
| 001A7C <sub>H</sub>                              | 001B7C <sub>H</sub>                              | DLC register 14           | DLCR14       | R/W    | ----XXXX <sub>B</sub>                                |
| 001A7D <sub>H</sub>                              | 001B7D <sub>H</sub>                              |                           |              |        |                                                      |
| 001A7E <sub>H</sub>                              | 001B7E <sub>H</sub>                              | DLC register 15           | DLCR15       | R/W    | ----XXXX <sub>B</sub>                                |
| 001A7F <sub>H</sub>                              | 001B7F <sub>H</sub>                              |                           |              |        |                                                      |
| 001A80 <sub>H</sub><br>to<br>001A87 <sub>H</sub> | 001B80 <sub>H</sub><br>to<br>001B87 <sub>H</sub> | Data register 0 (8 bytes) | DTR0         | R/W    | XXXXXXXX <sub>B</sub><br>to<br>XXXXXXXX <sub>B</sub> |

(Continued)

# MB90590/590G Series

(Continued)

| Address                                          |                                                  | Register                   | Abbreviation | Access | Initial Value                                        |
|--------------------------------------------------|--------------------------------------------------|----------------------------|--------------|--------|------------------------------------------------------|
| CAN0                                             | CAN1                                             |                            |              |        |                                                      |
| 001A88 <sub>H</sub><br>to<br>001A8F <sub>H</sub> | 001B88 <sub>H</sub><br>to<br>001B8F <sub>H</sub> | Data register 1 (8 bytes)  | DTR1         | R/W    | XXXXXXXX <sub>B</sub><br>to<br>XXXXXXXX <sub>B</sub> |
| 001A90 <sub>H</sub><br>to<br>001A97 <sub>H</sub> | 001B90 <sub>H</sub><br>to<br>001B97 <sub>H</sub> | Data register 2 (8 bytes)  | DTR2         | R/W    | XXXXXXXX <sub>B</sub><br>to<br>XXXXXXXX <sub>B</sub> |
| 001A98 <sub>H</sub><br>to<br>001A9F <sub>H</sub> | 001B98 <sub>H</sub><br>to<br>001B9F <sub>H</sub> | Data register 3 (8 bytes)  | DTR3         | R/W    | XXXXXXXX <sub>B</sub><br>to<br>XXXXXXXX <sub>B</sub> |
| 001AA0 <sub>H</sub><br>to<br>001AA7 <sub>H</sub> | 001BA0 <sub>H</sub><br>to<br>001BA7 <sub>H</sub> | Data register 4 (8 bytes)  | DTR4         | R/W    | XXXXXXXX <sub>B</sub><br>to<br>XXXXXXXX <sub>B</sub> |
| 001AA8 <sub>H</sub><br>to<br>001AAF <sub>H</sub> | 001BA8 <sub>H</sub><br>to<br>001BAF <sub>H</sub> | Data register 5 (8 bytes)  | DTR5         | R/W    | XXXXXXXX <sub>B</sub><br>to<br>XXXXXXXX <sub>B</sub> |
| 001AB0 <sub>H</sub><br>to<br>001AB7 <sub>H</sub> | 001BB0 <sub>H</sub><br>to<br>001BB7 <sub>H</sub> | Data register 6 (8 bytes)  | DTR6         | R/W    | XXXXXXXX <sub>B</sub><br>to<br>XXXXXXXX <sub>B</sub> |
| 001AB8 <sub>H</sub><br>to<br>001ABF <sub>H</sub> | 001BB8 <sub>H</sub><br>to<br>001BBF <sub>H</sub> | Data register 7 (8 bytes)  | DTR7         | R/W    | XXXXXXXX <sub>B</sub><br>to<br>XXXXXXXX <sub>B</sub> |
| 001AC0 <sub>H</sub><br>to<br>001AC7 <sub>H</sub> | 001BC0 <sub>H</sub><br>to<br>001BC7 <sub>H</sub> | Data register 8 (8 bytes)  | DTR8         | R/W    | XXXXXXXX <sub>B</sub><br>to<br>XXXXXXXX <sub>B</sub> |
| 001AC8 <sub>H</sub><br>to<br>001ACF <sub>H</sub> | 001BC8 <sub>H</sub><br>to<br>001BCF <sub>H</sub> | Data register 9 (8 bytes)  | DTR9         | R/W    | XXXXXXXX <sub>B</sub><br>to<br>XXXXXXXX <sub>B</sub> |
| 001AD0 <sub>H</sub><br>to<br>001AD7 <sub>H</sub> | 001BD0 <sub>H</sub><br>to<br>001BD7 <sub>H</sub> | Data register 10 (8 bytes) | DTR10        | R/W    | XXXXXXXX <sub>B</sub><br>to<br>XXXXXXXX <sub>B</sub> |
| 001AD8 <sub>H</sub><br>to<br>001ADF <sub>H</sub> | 001BD8 <sub>H</sub><br>to<br>001BDF <sub>H</sub> | Data register 11 (8 bytes) | DTR11        | R/W    | XXXXXXXX <sub>B</sub><br>to<br>XXXXXXXX <sub>B</sub> |
| 001AE0 <sub>H</sub><br>to<br>001AE7 <sub>H</sub> | 001BE0 <sub>H</sub><br>to<br>001BE7 <sub>H</sub> | Data register 12 (8 bytes) | DTR12        | R/W    | XXXXXXXX <sub>B</sub><br>to<br>XXXXXXXX <sub>B</sub> |
| 001AE8 <sub>H</sub><br>to<br>001AEF <sub>H</sub> | 001BE8 <sub>H</sub><br>to<br>001BEF <sub>H</sub> | Data register 13 (8 bytes) | DTR13        | R/W    | XXXXXXXX <sub>B</sub><br>to<br>XXXXXXXX <sub>B</sub> |
| 001AF0 <sub>H</sub><br>to<br>001AF7 <sub>H</sub> | 001BF0 <sub>H</sub><br>to<br>001BF7 <sub>H</sub> | Data register 14 (8 bytes) | DTR14        | R/W    | XXXXXXXX <sub>B</sub><br>to<br>XXXXXXXX <sub>B</sub> |
| 001AF8 <sub>H</sub><br>to<br>001AFF <sub>H</sub> | 001BF8 <sub>H</sub><br>to<br>001BFF <sub>H</sub> | Data register 15 (8 bytes) | DTR15        | R/W    | XXXXXXXX <sub>B</sub><br>to<br>XXXXXXXX <sub>B</sub> |

# MB90590/590G Series

## ■ INTERRUPT MAP

| Interrupt cause                   | I <sup>2</sup> O/S clear | Interrupt vector |                     | Interrupt control register |                     |
|-----------------------------------|--------------------------|------------------|---------------------|----------------------------|---------------------|
|                                   |                          | Number           | Address             | Number                     | Address             |
| Reset                             | N/A                      | # 08             | FFFFDC <sub>H</sub> | —                          | —                   |
| INT9 instruction                  | N/A                      | # 09             | FFFFD8 <sub>H</sub> | —                          | —                   |
| Exception                         | N/A                      | # 10             | FFFFD4 <sub>H</sub> | —                          | —                   |
| Time Base Timer                   | N/A                      | # 11             | FFFFD0 <sub>H</sub> | ICR00                      | 0000B0 <sub>H</sub> |
| External Interrupt (INT0 to INT7) | *1                       | # 12             | FFFFCC <sub>H</sub> |                            |                     |
| CAN 0 RX                          | N/A                      | # 13             | FFFFC8 <sub>H</sub> | ICR01                      | 0000B1 <sub>H</sub> |
| CAN 0 TX/NS                       | N/A                      | # 14             | FFFFC4 <sub>H</sub> |                            |                     |
| CAN 1 RX                          | N/A                      | # 15             | FFFFC0 <sub>H</sub> | ICR02                      | 0000B2 <sub>H</sub> |
| CAN 1 TX/NS                       | N/A                      | # 16             | FFFFBC <sub>H</sub> |                            |                     |
| 8/16 bit PPG 0/1                  | N/A                      | # 17             | FFFFB8 <sub>H</sub> | ICR03                      | 0000B3 <sub>H</sub> |
| 8/16 bit PPG 2/3                  | N/A                      | # 18             | FFFFB4 <sub>H</sub> |                            |                     |
| 8/16 bit PPG 4/5                  | N/A                      | # 19             | FFFFB0 <sub>H</sub> | ICR04                      | 0000B4 <sub>H</sub> |
| 8/16 bit PPG 6/7                  | N/A                      | # 20             | FFFFAC <sub>H</sub> |                            |                     |
| 8/16 bit PPG 8/9                  | N/A                      | # 21             | FFFFA8 <sub>H</sub> | ICR05                      | 0000B5 <sub>H</sub> |
| 8/16 bit PPG A/B                  | N/A                      | # 22             | FFFFA4 <sub>H</sub> |                            |                     |
| 16-bit Reload Timer 0             | *1                       | # 23             | FFFFA0 <sub>H</sub> | ICR06                      | 0000B6 <sub>H</sub> |
| 16-bit Reload Timer 1             | *1                       | # 24             | FFFF9C <sub>H</sub> |                            |                     |
| Input Capture 0/1                 | *1                       | # 25             | FFFF98 <sub>H</sub> | ICR07                      | 0000B7 <sub>H</sub> |
| Output compare 0/1                | *1                       | # 26             | FFFF94 <sub>H</sub> |                            |                     |
| Input Capture 2/3                 | *1                       | # 27             | FFFF90 <sub>H</sub> | ICR08                      | 0000B8 <sub>H</sub> |
| Output Compare 2/3                | *1                       | # 28             | FFFF8C <sub>H</sub> |                            |                     |
| Input Capture 4/5                 | *1                       | # 29             | FFFF88 <sub>H</sub> | ICR09                      | 0000B9 <sub>H</sub> |
| Output Compare 4/5                | *1                       | # 30             | FFFF84 <sub>H</sub> |                            |                     |
| 8/10 bit A/D Converter            | *1                       | # 31             | FFFF80 <sub>H</sub> | ICR10                      | 0000BA <sub>H</sub> |
| I/O Timer/Watch Timer             | N/A                      | # 32             | FFFF7C <sub>H</sub> |                            |                     |
| Serial I/O                        | *1                       | # 33             | FFFF78 <sub>H</sub> | ICR11                      | 0000BB <sub>H</sub> |
| Sound Generator                   | N/A                      | # 34             | FFFF74 <sub>H</sub> |                            |                     |
| UART 0 RX                         | *2                       | # 35             | FFFF70 <sub>H</sub> | ICR12                      | 0000BC <sub>H</sub> |
| UART 0 TX                         | *1                       | # 36             | FFFF6C <sub>H</sub> |                            |                     |
| UART 1 RX                         | *2                       | # 37             | FFFF68 <sub>H</sub> | ICR13                      | 0000BD <sub>H</sub> |
| UART 1 TX                         | *1                       | # 38             | FFFF64 <sub>H</sub> |                            |                     |
| UART 2 RX                         | *2                       | # 39             | FFFF60 <sub>H</sub> | ICR14                      | 0000BE <sub>H</sub> |
| UART 2 TX                         | *1                       | # 40             | FFFF5C <sub>H</sub> |                            |                     |
| Flash Memory                      | N/A                      | # 41             | FFFF58 <sub>H</sub> | ICR15                      | 0000BF <sub>H</sub> |
| Delayed interrupt                 | N/A                      | # 42             | FFFF54 <sub>H</sub> |                            |                     |

\*1: The interrupt request flag is cleared by the I<sup>2</sup>OS interrupt clear signal.

\*2: The interrupt request flag is cleared by the I<sup>2</sup>OS interrupt clear signal. A stop request is available.

N/A: The interrupt request flag is not cleared by the I<sup>2</sup>OS interrupt clear signal.

Note: • For a peripheral module with two interrupt for a single interrupt number, both interrupt request flags are cleared by the I<sup>2</sup>OS interrupt clear signal.

- At the end of I<sup>2</sup>OS, the I<sup>2</sup>OS clear signal will be asserted for all the interrupt flags assigned to the same interrupt number. If one interrupt flag starts the I<sup>2</sup>OS and in the meantime another interrupt flag is set by a hardware event, the later event is lost because the flag is cleared by the I<sup>2</sup>OS clear signal caused by the first event. So it is recommended not to use the I<sup>2</sup>OS for this interrupt number.
- If I<sup>2</sup>OS is enabled, I<sup>2</sup>OS is initiated when one of the two interrupt signals in the same interrupt control register (ICR) is asserted. This means that different interrupt sources share the same I<sup>2</sup>OS Descriptor which should be unique for each interrupt source. For this reason, when one interrupt source uses the I<sup>2</sup>OS, the other interrupt should be disabled.

# MB90590/590G Series

## ■ ELECTRICAL CHARACTERISTICS

### 1. Absolute Maximum Ratings

( $V_{SS} = AV_{SS} = 0\text{ V}$ )

| Parameter                             | Symbol             | Rating         |                | Unit | Remarks                                     |
|---------------------------------------|--------------------|----------------|----------------|------|---------------------------------------------|
|                                       |                    | Min.           | Max.           |      |                                             |
| Power supply voltage                  | $V_{CC}$           | $V_{SS} - 0.3$ | $V_{SS} + 6.0$ | V    |                                             |
|                                       | $AV_{CC}$          | $V_{SS} - 0.3$ | $V_{SS} + 6.0$ | V    | $V_{CC} = AV_{CC}$ *1                       |
|                                       | AVRH, AVRL         | $V_{SS} - 0.3$ | $V_{SS} + 6.0$ | V    | $AV_{CC} \geq AVRH/L$ , $AVRH \geq AVRL$ *1 |
|                                       | $DV_{CC}$          | $V_{SS} - 0.3$ | $V_{SS} + 6.0$ | V    | $V_{CC} \geq DV_{CC}$                       |
| Input voltage                         | $V_I$              | $V_{SS} - 0.3$ | $V_{SS} + 6.0$ | V    | *2                                          |
| Output voltage                        | $V_O$              | $V_{SS} - 0.3$ | $V_{SS} + 6.0$ | V    | *2                                          |
| Clamp Current                         | $I_{CLAMP}$        | -2.0           | 2.0            | mA   |                                             |
| "L" level max. output current         | $I_{OL1}$          | —              | 15             | mA   | Normal output *3                            |
| "L" level avg. output current         | $I_{OLAV1}$        | —              | 4              | mA   | Normal output, average value *4             |
| "L" level max. output current         | $I_{OL2}$          | —              | 40             | mA   | High current output *3                      |
| "L" level avg. output current         | $I_{OLAV2}$        | —              | 30             | mA   | High current output, average value *4       |
| "L" level max. overall output current | $\Sigma I_{OL1}$   | —              | 100            | mA   | Total normal output                         |
| "L" level max. overall output current | $\Sigma I_{OL2}$   | —              | 330            | mA   | Total high current output                   |
| "L" level avg. overall output current | $\Sigma I_{OLAV1}$ | —              | 50             | mA   | Total normal output, average value *5       |
| "L" level avg. overall output current | $\Sigma I_{OLAV2}$ | —              | 250            | mA   | Total high current output, average value *5 |
| "H" level max. output current         | $I_{OH1}$          | —              | -15            | mA   | Normal output *3                            |
| "H" level avg. output current         | $I_{OHAV1}$        | —              | -4             | mA   | Normal output, average value *4             |
| "H" level max. output current         | $I_{OH2}$          | —              | -40            | mA   | High current output *3                      |
| "H" level avg. output current         | $I_{OHAV2}$        | —              | -30            | mA   | High current output, average value *4       |
| "H" level max. overall output current | $\Sigma I_{OH1}$   | —              | -100           | mA   | Total normal output                         |
| "H" level max. overall output current | $\Sigma I_{OH2}$   | —              | -330           | mA   | Total high current output                   |
| "H" level avg. overall output current | $\Sigma I_{OHAV1}$ | —              | -50            | mA   | Total normal output, average value *5       |
| "H" level avg. overall output current | $\Sigma I_{OHAV2}$ | —              | -250           | mA   | Total high current output, average value *5 |
| Power consumption                     | $P_D$              | —              | 500            | mW   | MB90F594A, MB90F591A, MB90F594G             |
|                                       |                    | —              | 400            | mW   | MB90594, MB90591, MB90594G                  |
| Operating temperature                 | $T_A$              | -40            | +85            | °C   |                                             |
| Storage temperature                   | $T_{STG}$          | -55            | +150           | °C   |                                             |

\*1:  $AV_{CC}$ , AVRH and AVRL should not exceed  $V_{CC}$  and AVRL should not exceed AVRH.

\*2:  $V_I$  and  $V_O$  should not exceed  $V_{CC} + 0.3V$ .  $V_I$  should not exceed the specified ratings. However if the maximum current to/from an input is limited by some means with external components, the  $I_{CLAMP}$  rating supercedes the  $V_I$  rating.

\*3: The maximum output current is a peak value for a corresponding pin.

\*4: Average output current is an average current value observed for a 100 ms period for a corresponding pin.

\*5: Total average current is an average current value observed for a 100 ms period for all corresponding pins.

Note: Average output current = operating current  $\times$  operating efficiency

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## 2. Recommended Conditions

( $V_{SS} = AV_{SS} = 0\text{ V}$ )

| Parameter             | Symbol                | Value          |      |                | Unit               | Remarks                         |                                                                         |
|-----------------------|-----------------------|----------------|------|----------------|--------------------|---------------------------------|-------------------------------------------------------------------------|
|                       |                       | Min.           | Typ. | Max.           |                    |                                 |                                                                         |
| Power supply voltage  | $V_{CC}$<br>$AV_{CC}$ | 4.5            | 5.0  | 5.5            | V                  | Under normal operation          | MB90V590A<br>MB90V590G<br>MB90F594A<br>MB90F594G<br>MB90594<br>MB90594G |
|                       |                       | 3.0            | —    | 5.5            | V                  | Maintains RAM data in stop mode |                                                                         |
|                       |                       | 4.75           | 5.0  | 5.25           | V                  | Under normal operation          | MB90F591A<br>MB90591                                                    |
|                       |                       | 3.0            | —    | 5.25           | V                  | Maintains RAM data in stop mode |                                                                         |
| Input H voltage       | $V_{IHS}$             | $0.8 V_{CC}$   | —    | $V_{CC} + 0.3$ | V                  | CMOS hysteresis input pin       |                                                                         |
|                       | $V_{IHM}$             | $V_{CC} - 0.3$ | —    | $V_{CC} + 0.3$ | V                  | MD input pin                    |                                                                         |
| Input L voltage       | $V_{ILS}$             | $V_{SS} - 0.3$ | —    | $0.6V_{CC}$    | V                  | CMOS hysteresis input pin       |                                                                         |
|                       | $V_{ILM}$             | $V_{SS} - 0.3$ | —    | $V_{SS} + 0.3$ | V                  | MD input pin                    |                                                                         |
| Smooth capacitor      | $C_S$                 | 0.022          | 0.1  | 1.0            | $\mu\text{F}$      | *                               |                                                                         |
| Operating temperature | $T_A$                 | -40            | —    | +85            | $^{\circ}\text{C}$ |                                 |                                                                         |

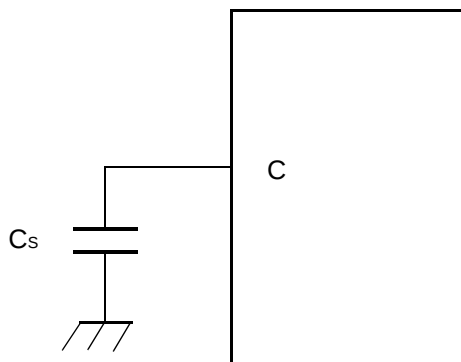
\*: Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The smoothing capacitor to be connected to the  $V_{CC}$  pin must have a capacitance value higher than  $C_S$ .

**WARNING:** The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

### • C Pin Connection Diagram



# MB90590/590G Series

## 3. DC Characteristics

(MB90V590A, MB90F594A, MB90594, MB90V590G, MB90F594G, MB90594G:

$V_{CC} = 5.0 \text{ V} \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0\text{V}$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

(MB90F591A, MB90591:  $V_{CC} = 5.0 \text{ V} \pm 5\%$ ,  $V_{SS} = AV_{SS} = 0\text{V}$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

| Parameter                 | Symbol           | Pin name                                                                                                                                                            | Condition                                                                              | Value                 |      |      | Unit | Remarks         |
|---------------------------|------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------|-----------------------|------|------|------|-----------------|
|                           |                  |                                                                                                                                                                     |                                                                                        | Min.                  | Typ. | Max. |      |                 |
| Output H voltage          | V <sub>OH1</sub> | Normal output                                                                                                                                                       | V <sub>CC</sub> = 4.5 V,<br>I <sub>OH1</sub> = −4.0 mA                                 | V <sub>CC</sub> − 0.5 | —    | —    | V    |                 |
|                           | V <sub>OH2</sub> | High current output                                                                                                                                                 | V <sub>CC</sub> = 4.5 V,<br>I <sub>OH2</sub> = −30.0 mA                                | V <sub>CC</sub> − 0.5 | —    | —    | V    |                 |
| Output L voltage          | V <sub>OL1</sub> | Normal output                                                                                                                                                       | V <sub>CC</sub> = 4.5 V,<br>I <sub>OL1</sub> = 4.0 mA                                  | —                     | —    | 0.4  | V    |                 |
|                           | V <sub>OL2</sub> | High current output                                                                                                                                                 | V <sub>CC</sub> = 4.5 V,<br>I <sub>OL2</sub> = 30.0 mA                                 | —                     | —    | 0.5  | V    |                 |
| Input leak current        | I <sub>IL</sub>  | —                                                                                                                                                                   | V <sub>CC</sub> = 5.5 V,<br>V <sub>SS</sub> < V <sub>I</sub> < V <sub>CC</sub>         | −5                    | —    | 5    | μA   |                 |
| Analog input leak current | I <sub>IAL</sub> | AN0 to AN7                                                                                                                                                          | V <sub>CC</sub> = 5.5 V,<br>AV <sub>SS</sub> < V <sub>I</sub> < AV <sub>CC</sub>       | −1                    | —    | 1    | μA   |                 |
| Power supply current *    | I <sub>CC</sub>  | V <sub>CC</sub>                                                                                                                                                     | V <sub>CC</sub> = 5.0 V±10%,<br>Internal frequency:<br>16 MHz,<br>At normal operation. | —                     | 37   | 60   | mA   | MB90594/594G    |
|                           |                  |                                                                                                                                                                     |                                                                                        | —                     | 50   | 80   | mA   | MB90F594A/F594G |
|                           |                  |                                                                                                                                                                     |                                                                                        | —                     | 50   | 80   | mA   | MB90F591A       |
|                           |                  |                                                                                                                                                                     |                                                                                        | —                     | 45   | 60   | mA   | MB90591         |
|                           | I <sub>CCS</sub> |                                                                                                                                                                     | V <sub>CC</sub> = 5.0 V±10%,<br>Internal frequency:<br>16 MHz,<br>At Sleep mode.       | —                     | 13   | 20   | mA   | MB90594/594G    |
|                           |                  |                                                                                                                                                                     |                                                                                        | —                     | 15   | 23   | mA   | MB90F594A/F594G |
|                           |                  |                                                                                                                                                                     |                                                                                        | —                     | 15   | 23   | mA   | MB90F591A       |
|                           |                  |                                                                                                                                                                     |                                                                                        | —                     | 15   | 23   | mA   | MB90591         |
|                           | I <sub>CTS</sub> |                                                                                                                                                                     | V <sub>CC</sub> = 5.0 V±1%,<br>Internal frequency:<br>2 MHz,<br>At Timer mode          | —                     | 0.3  | 0.6  | mA   | MB90594/594G    |
|                           |                  |                                                                                                                                                                     |                                                                                        | —                     | 0.35 | 0.6  | mA   | MB90F594A/F594G |
|                           |                  |                                                                                                                                                                     |                                                                                        | —                     | 0.35 | 0.6  | mA   | MB90F591A       |
|                           |                  |                                                                                                                                                                     |                                                                                        | —                     | 0.35 | 0.6  | mA   | MB90591         |
|                           | I <sub>CCH</sub> |                                                                                                                                                                     | V <sub>CC</sub> = 5.0 V±10%,<br>At Stop mode,<br>T <sub>A</sub> = 25°C                 | —                     | 5    | 20   | μA   | MB90594/594G    |
|                           |                  |                                                                                                                                                                     |                                                                                        | —                     | 5    | 20   | μA   | MB90F594A/F594G |
|                           |                  |                                                                                                                                                                     |                                                                                        | —                     | 5    | 20   | μA   | MB90F591A       |
|                           |                  |                                                                                                                                                                     |                                                                                        | —                     | 5    | 20   | μA   | MB90591         |
| Input capacity            | C <sub>IN</sub>  | Other than C,<br>AV <sub>CC</sub> , AV <sub>SS</sub> ,<br>AVRH, AVRL,<br>V <sub>CC</sub> , V <sub>SS</sub> ,<br>DV <sub>CC</sub> , DV <sub>SS</sub> ,<br>P70 to P87 | —                                                                                      | —                     | 5    | 15   | pF   |                 |
|                           |                  | P70 to P87                                                                                                                                                          | —                                                                                      | —                     | 15   | 30   | pF   |                 |

\*: Current values are tentative and subject to change without notice according to improvements in the characteristics. The power supply current testing conditions are when using the external clock.

## 4. AC Characteristics

### (1) Clock Timing

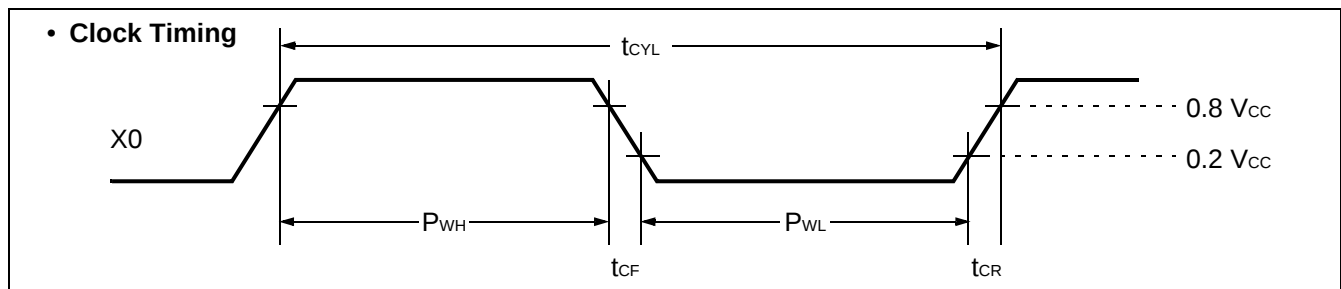
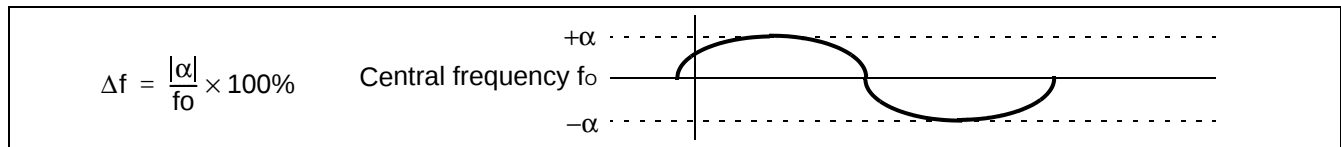
(MB90V590A, MB90F594A, MB90594, MB90V590G, MB90F594G, MB90594G:

$V_{CC} = 5.0 \text{ V} \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0\text{V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

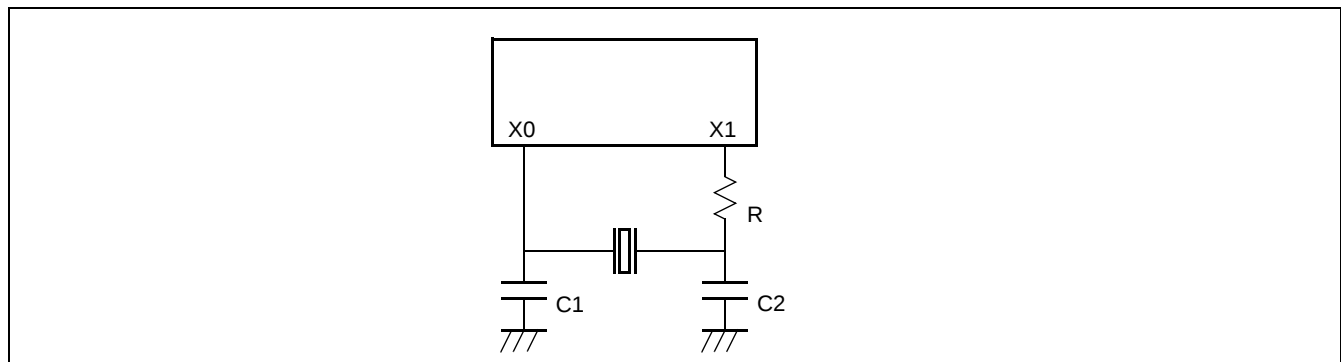
(MB90F591A, MB90591:  $V_{CC} = 5.0 \text{ V} \pm 5\%$ ,  $V_{SS} = AV_{SS} = 0\text{V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

| Parameter                      | Symbol           | Pin name | Value |            |      | Unit | Remarks                            |
|--------------------------------|------------------|----------|-------|------------|------|------|------------------------------------|
|                                |                  |          | Min.  | Typ.       | Max. |      |                                    |
| Oscillation frequency          | $f_c$            | X0, X1   | 3     | —          | 5    | MHz  | When using an oscillation circuit. |
|                                |                  |          | 3     | —          | 16   | MHz  | When using an external clock.      |
| Oscillation cycle time         | $t_{CYL}$        | X0, X1   | 200   | —          | 333  | ns   | When using an oscillation circuit. |
|                                |                  |          | 62.5  | —          | 333  | ns   | When using an external clock.      |
| Frequency deviation with PLL*  | $\Delta f$       | —        | —     | —          | 5    | %    |                                    |
| Input clock pulse width        | $P_{WH}, P_{WL}$ | X0       | 10    | —          | —    | ns   | Duty ratio is about 30 to 70%.     |
| Input clock rise and fall time | $t_{CR}, t_{CF}$ | X0       | —     | —          | 5    | ns   | When using external clock          |
| Machine clock frequency        | $f_{CP}$         | —        | 1.5   | —          | 16   | MHz  |                                    |
| Machine clock cycle time       | $t_{CP}$         | —        | 62.5  | —          | 666  | ns   |                                    |
| Flash read cycle time          | $t_{CYCFL}$      | —        | —     | $2 t_{CP}$ | —    | ns   | When Flash is accessed by CPU      |

\*: Frequency deviation indicates the maximum frequency difference from the target frequency when using a multiplied clock.

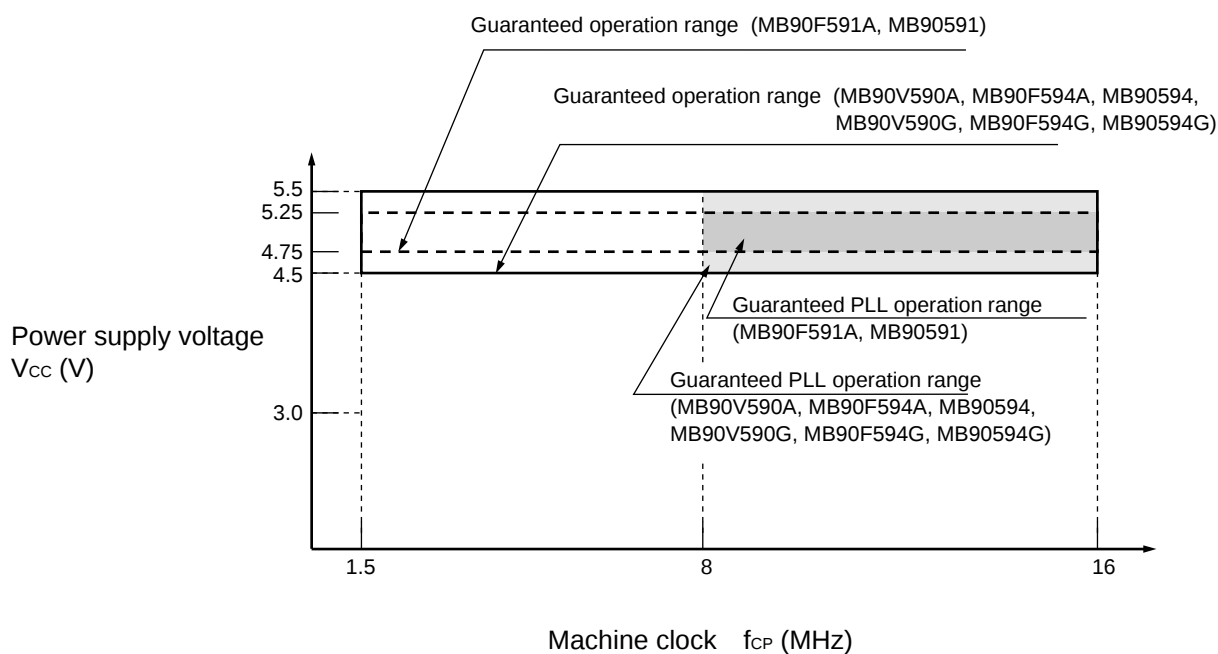


Example of Oscillation circuit

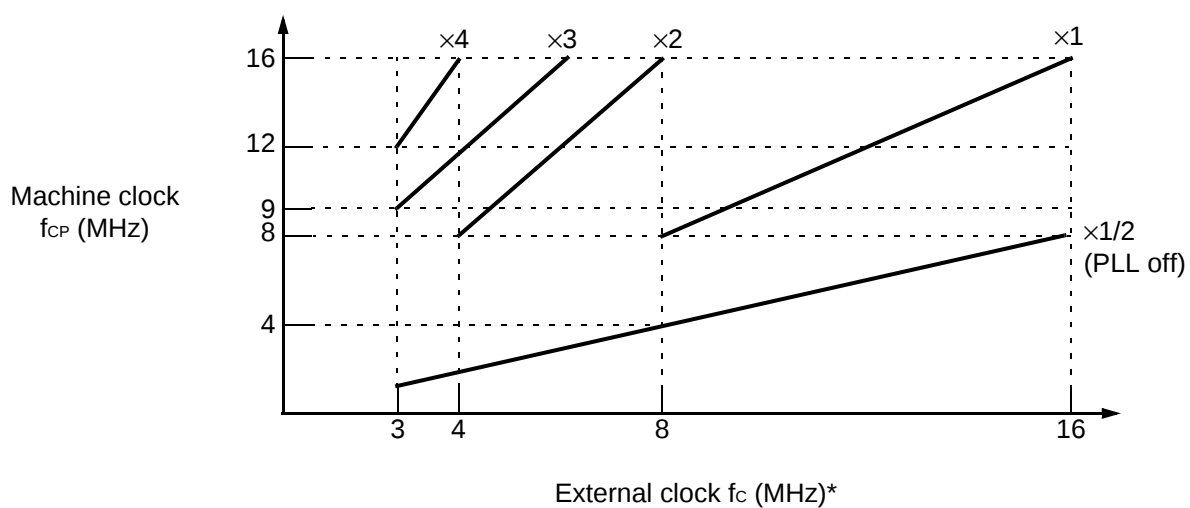


# MB90590/590G Series

## • Guaranteed operation range



## • External clock frequency and machine clock frequency



\*: When using the oscillation circuit, the maximum oscillation clock frequency is 5 MHz.

## (2) Reset and Hardware Standby Input

(MB90V590A, MB90F594A, MB90594, MB90V590G, MB90F594G, MB90594G:

$V_{CC} = 5.0 \text{ V} \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0\text{V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

(MB90F591A, MB90591:  $V_{CC} = 5.0 \text{ V} \pm 5\%$ ,  $V_{SS} = AV_{SS} = 0\text{V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

| Parameter                   | Symbol     | Pin name                | Value                                                           |      | Unit | Remarks                |
|-----------------------------|------------|-------------------------|-----------------------------------------------------------------|------|------|------------------------|
|                             |            |                         | Min.                                                            | Max. |      |                        |
| Reset input time            | $t_{RSTL}$ | $\overline{\text{RST}}$ | $16 t_{CP}^{*1}$                                                | —    | ns   | Under normal operation |
|                             |            |                         | Oscillation time of oscillator <sup>*2</sup> + $16 t_{CP}^{*1}$ | —    | ms   | In stop mode           |
| Hardware standby input time | $t_{HSTL}$ | $\overline{\text{HST}}$ | $16 t_{CP}^{*1}$                                                | —    | ns   | Under normal operation |
|                             |            |                         | Oscillation time of oscillator <sup>*2</sup> + $16 t_{CP}^{*1}$ | —    | ms   | In stop mode           |

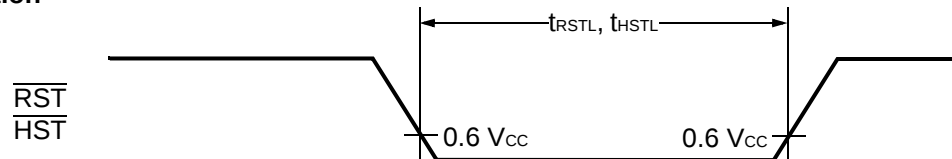
\*1: " $t_{CP}$ " represents one cycle time of the machine clock.

No reset can fully initialize the Flash Memory if it is performing the automatic algorithm.

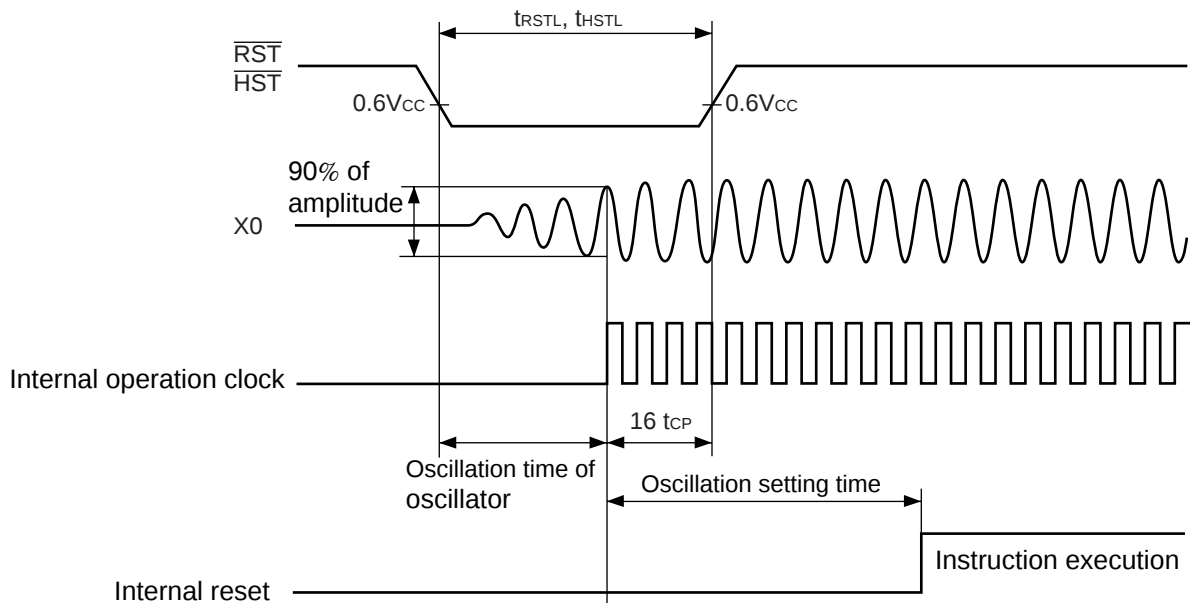
\*2: Oscillation time of oscillator is time that the amplitude reached the 90%.

In the crystal oscillator, the oscillation time is between several ms to tens of ms. In FAR / ceramic oscillator, the oscillation time is between hundreds of  $\mu\text{s}$  to several ms. In the external clock, the oscillation time is 0 ms.

### Under Normal Operation



### In Stop Mode



# MB90590/590G Series

## (3) Power On Reset

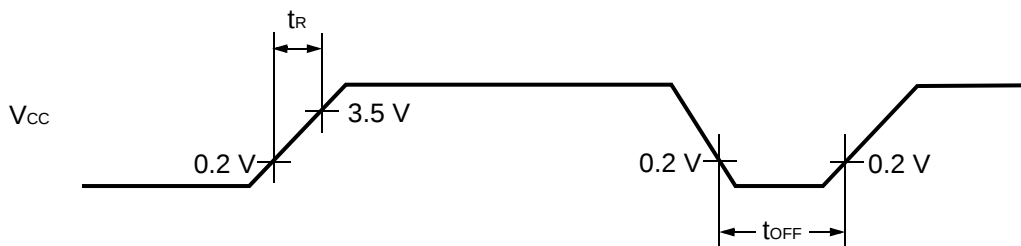
(MB90V590A, MB90F594A, MB90594, MB90V590G, MB90F594G, MB90594G:

$V_{CC} = 5.0 \text{ V} \pm 10 \%$ ,  $V_{SS} = AV_{SS} = 0 \text{ V}$ ,  $T_A = -40^\circ \text{C}$  to  $+85^\circ \text{C}$ )

(MB90F591A, MB90591:  $V_{CC} = 5.0 \text{ V} \pm 5 \%$ ,  $V_{SS} = AV_{SS} = 0 \text{ V}$ ,  $T_A = -40^\circ \text{C}$  to  $+85^\circ \text{C}$ )

| Parameter          | Symbol    | Pin name | Condition | Value |      | Unit | Remarks                     |
|--------------------|-----------|----------|-----------|-------|------|------|-----------------------------|
|                    |           |          |           | Min.  | Max. |      |                             |
| Power on rise time | $t_R$     | $V_{CC}$ | —         | 0.05  | 30   | ms   |                             |
| Power off time     | $t_{OFF}$ | $V_{CC}$ |           | 50    | —    | ms   | Due to repetitive operation |

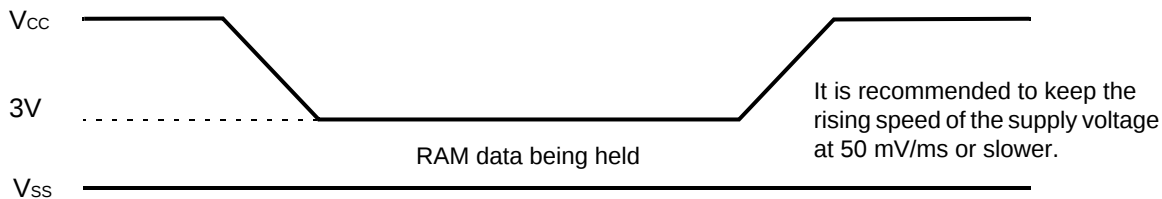
- Note
- $V_{CC}$  must be kept lower than 0.2 V before power-on.
  - The above values are used for creating a power-on reset.
  - Some registers in the device are initialized only upon a power-on reset. To initialize these register, turn on the power supply using the above values.



Sudden changes in the power supply voltage may cause a power-on reset.

To change the power supply voltage while the device is in operation, it is recommended to raise the voltage smoothly to suppress fluctuations as shown below.

In this case, change the supply voltage with the PLL clock not used. If the voltage drop is 1 V or fewer per second, however, you can use the PLL clock.



## (4) UART0/1/2, Serial I/O

(MB90V590A, MB90F594A, MB90594, MB90V590G, MB90F594G, MB90594G:

$V_{CC} = 5.0 V \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0V$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ )

(MB90F591A, MB90591:  $V_{CC} = 5.0 V \pm 5\%$ ,  $V_{SS} = AV_{SS} = 0V$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ )

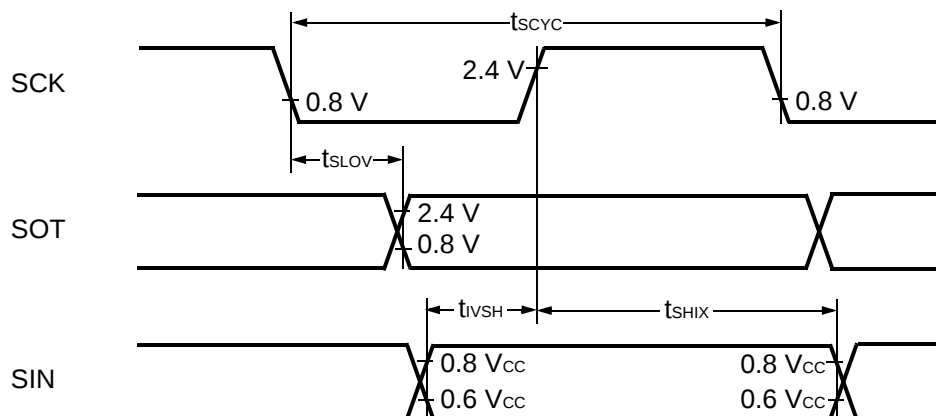
| Parameter                                      | Symbol     | Pin name                   | Condition                                                                      | Value         |      | Unit | Remarks |
|------------------------------------------------|------------|----------------------------|--------------------------------------------------------------------------------|---------------|------|------|---------|
|                                                |            |                            |                                                                                | Min.          | Max. |      |         |
| Serial clock cycle time                        | $t_{SCYC}$ | SCK0 to SCK3               | Internal clock operation output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$ . | $8\ t_{CP}^*$ | —    | ns   |         |
| SCK $\downarrow \Rightarrow$ SOT delay time    | $t_{SLOV}$ | SCK0 to SCK3, SOT0 to SOT3 |                                                                                | -80           | 80   | ns   |         |
| Valid SIN $\Rightarrow$ SCK $\uparrow$         | $t_{IVSH}$ | SCK0 to SCK3, SIN0 to SIN3 |                                                                                | 100           | —    | ns   |         |
| SCK $\uparrow \Rightarrow$ Valid SIN hold time | $t_{SHIX}$ | SCK0 to SCK3, SIN0 to SIN3 |                                                                                | 60            | —    | ns   |         |
| Serial clock "H" pulse width                   | $t_{SHSL}$ | SCK0 to SCK3               | External clock operation output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$ . | $4\ t_{CP}$   | —    | ns   |         |
| Serial clock "L" pulse width                   | $t_{SLSH}$ | SCK0 to SCK3               |                                                                                | $4\ t_{CP}$   | —    | ns   |         |
| SCK $\downarrow \Rightarrow$ SOT delay time    | $t_{SLOV}$ | SCK0 to SCK3, SOT0 to SOT3 |                                                                                | —             | 150  | ns   |         |
| Valid SIN $\Rightarrow$ SCK $\uparrow$         | $t_{IVSH}$ | SCK0 to SCK3, SIN0 to SIN3 |                                                                                | 60            | —    | ns   |         |
| SCK $\uparrow \Rightarrow$ Valid SIN hold time | $t_{SHIX}$ | SCK0 to SCK3, SIN0 to SIN3 |                                                                                | 60            | —    | ns   |         |

\*:  $t_{CP}$  is the machine cycle (Unit: ns)

Notes: • AC characteristic in CLK synchronized mode.

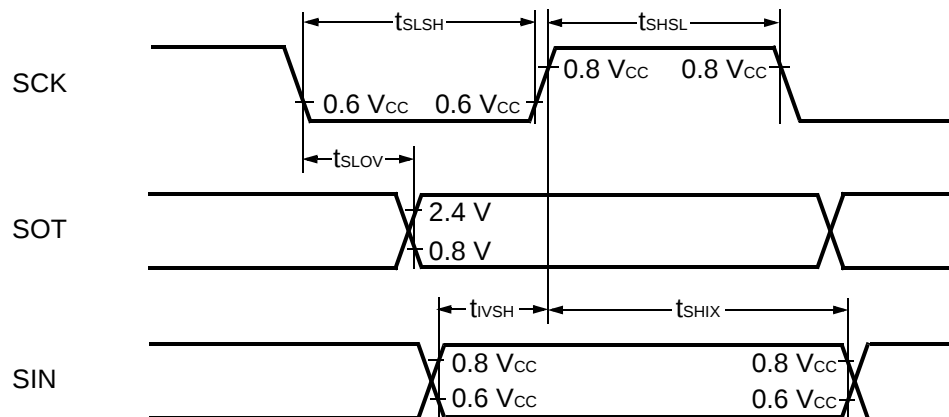
•  $C_L$  is load capacity value of pins when testing.

### • Internal Shift Clock Mode



# MB90590/590G Series

## • External Shift Clock Mode



## (5) Timer Input Timing

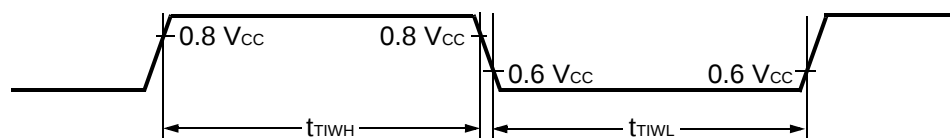
(MB90V590A, MB90F594A, MB90594, MB90V590G, MB90F594G, MB90594G:

$V_{CC} = 5.0 V \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0V$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ )

(MB90F591A, MB90591:  $V_{CC} = 5.0 V \pm 5\%$ ,  $V_{SS} = AV_{SS} = 0V$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ )

| Parameter         | Symbol     | Pin name   | Condition | Value      |      | Unit    | Remarks                |
|-------------------|------------|------------|-----------|------------|------|---------|------------------------|
|                   |            |            |           | Min.       | Max. |         |                        |
| Input pulse width | $t_{TIWH}$ | TIN0       | —         | $4 t_{CP}$ | —    | ns      | Under normal operation |
|                   | $t_{TIWL}$ | IN0 to IN5 |           | 1          | —    | $\mu s$ | In stop mode           |

## • Timer Input Timing



## (6) Trigger Input Timing

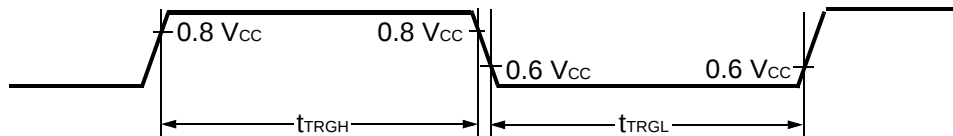
(MB90V590A, MB90F594A, MB90594, MB90V590G, MB90F594G, MB90594G:

$V_{CC} = 5.0 \text{ V} \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0\text{V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

(MB90F591A, MB90591:  $V_{CC} = 5.0 \text{ V} \pm 5\%$ ,  $V_{SS} = AV_{SS} = 0\text{V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

| Parameter         | Symbol                   | Pin name              | Condition | Value      |      | Unit | Remarks |
|-------------------|--------------------------|-----------------------|-----------|------------|------|------|---------|
|                   |                          |                       |           | Min.       | Max. |      |         |
| Input pulse width | $t_{TRGH}$<br>$t_{TRGL}$ | INT0 to<br>INT7, ADTG | —         | 5 $t_{CP}$ | —    | ns   |         |

### • Trigger Input Timing



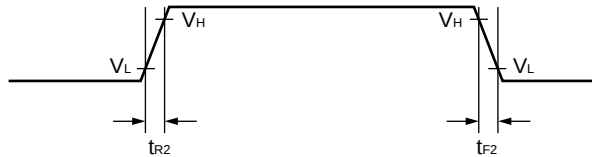
## (7) Slew Rate High Current Outputs (MB90F591A, MB90591, MB90594G and MB90F594G only)

(MB90F594G, MB90594G:  $V_{CC} = 5.0 \text{ V} \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0\text{V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

(MB90F591A, MB90591:  $V_{CC} = 5.0 \text{ V} \pm 5\%$ ,  $V_{SS} = AV_{SS} = 0\text{V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

| Parameter             | Symbol               | Pin name                            | Condition | Value |      | Unit | Remarks |
|-----------------------|----------------------|-------------------------------------|-----------|-------|------|------|---------|
|                       |                      |                                     |           | Min.  | Max. |      |         |
| Output Rise/Fall time | $t_{R2}$<br>$t_{F2}$ | Port P70 to P77,<br>Port P80 to P87 | —         | 15    | 40   | ns   |         |

### • Slew Rate Output Timing



$$V_H = V_{OL2} + 0.1 \times (V_{OH2} - V_{OL2})$$

$$V_L = V_{OL2} + 0.9 \times (V_{OH2} - V_{OL2})$$

# MB90590/590G Series

## 5. A/D Converter

(MB90V590A, MB90F594A, MB90594, MB90V590G, MB90F594G, MB90594G:

$V_{CC} = AV_{CC} = 5.0 \text{ V} \pm 10 \%$ ,  $V_{SS} = AV_{SS} = 0 \text{ V}$ ,  $3.0 \text{ V} \leq AVR+ - AVR-$ ,  $T_A = -40 \text{ }^\circ\text{C}$  to  $+85 \text{ }^\circ\text{C}$ )

(MB90F591A, MB90591:  $V_{CC} = AV_{CC} = 5.0 \text{ V} \pm 5 \%$ ,  $V_{SS} = AV_{SS} = 0 \text{ V}$ ,  $3.0 \text{ V} \leq AVR+ - AVR-$ ,  $T_A = -40 \text{ }^\circ\text{C}$  to  $+85 \text{ }^\circ\text{C}$ )

| Parameter                     | Symbol    | Pin name   | Value        |              |              | Unit          | Remarks                                                                  |
|-------------------------------|-----------|------------|--------------|--------------|--------------|---------------|--------------------------------------------------------------------------|
|                               |           |            | Min.         | Typ.         | Max.         |               |                                                                          |
| Resolution                    | —         | —          | —            | —            | 10           | bit           |                                                                          |
| Conversion error              | —         | —          | —            | —            | $\pm 5.0$    | LSB           |                                                                          |
| Nonlinearity error            | —         | —          | —            | —            | $\pm 2.5$    | LSB           |                                                                          |
| Differential linearity error  | —         | —          | —            | —            | $\pm 1.9$    | LSB           |                                                                          |
| Zero transition voltage       | $V_{OT}$  | AN0 to AN7 | $AVRL - 3.5$ | $AVRL + 0.5$ | $AVRL + 4.5$ | mV            |                                                                          |
| Full scale transition voltage | $V_{FST}$ | AN0 to AN7 | $AVRH - 6.5$ | $AVRH - 1.5$ | $AVRH + 1.5$ | mV            |                                                                          |
| Conversion time               | —         | —          | —            | $352t_{CP}$  | —            | ns            |                                                                          |
| Sampling time                 | —         | —          | —            | $64t_{CP}$   | —            | ns            |                                                                          |
| Analog port input current     | $I_{AIN}$ | AN0 to AN7 | -1           | —            | +1           | $\mu\text{A}$ |                                                                          |
| Analog input voltage range    | $V_{AIN}$ | AN0 to AN7 | AVRL         | —            | AVRH         | V             |                                                                          |
| Reference voltage range       | —         | AVRH       | $AVRL + 2.7$ | —            | $AV_{CC}$    | V             |                                                                          |
|                               | —         | AVRL       | 0            | —            | $AVRH - 2.7$ | V             |                                                                          |
| Power supply current          | $I_A$     | $AV_{CC}$  | —            | 5            | —            | mA            |                                                                          |
|                               | $I_{AH}$  | $AV_{CC}$  | —            | —            | 5            | $\mu\text{A}$ | *                                                                        |
| Reference voltage current     | $I_R$     | AVRH       | —            | 400          | 600          | $\mu\text{A}$ | MB90594<br>MB90V590A<br>MB90V590G<br>MB90F594A<br>MB90F594G<br>MB90F591A |
|                               |           |            | —            | 140          | 600          | $\mu\text{A}$ | MB90594G<br>MB90591                                                      |
|                               | $I_{RH}$  | AVRH       | —            | —            | 5            | $\mu\text{A}$ | *                                                                        |
| Offset between input channels | —         | AN0 to AN7 | —            | —            | 4            | LSB           |                                                                          |

\*: When not operating A/D converter, this is the current ( $V_{CC} = AV_{CC} = AVRH = 5.0 \text{ V}$ ) when the CPU is stopped.

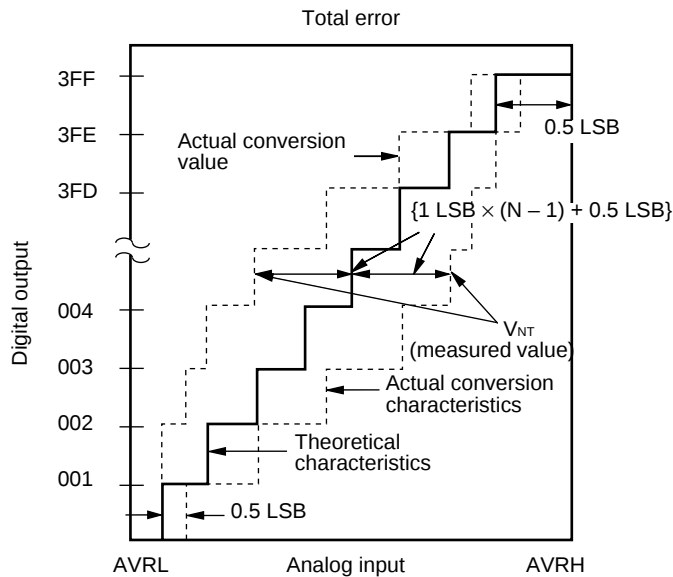
## 6. A/D Converter Glossary

**Resolution:** Analog changes that are identifiable with the A/D converter

**Linearity error:** The deviation of the straight line connecting the zero transition point ("00 0000 0000" ↔ "00 0000 0001") with the full-scale transition point ("11 1111 1110" ↔ "11 1111 1111") from actual conversion characteristics

**Differential linearity error:** The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value

**Total error:** The total error is defined as a difference between the actual value and the theoretical value, which includes zero-transition error/full-scale transition error and linearity error.



$$1 \text{ LSB} = (\text{Theoretical value}) \frac{\text{AVRH} - \text{AVRL}}{1024} [\text{V}]$$

$$V_{0T} (\text{Theoretical value}) = \text{AVRL} + 0.5 \text{ LSB} [\text{V}]$$

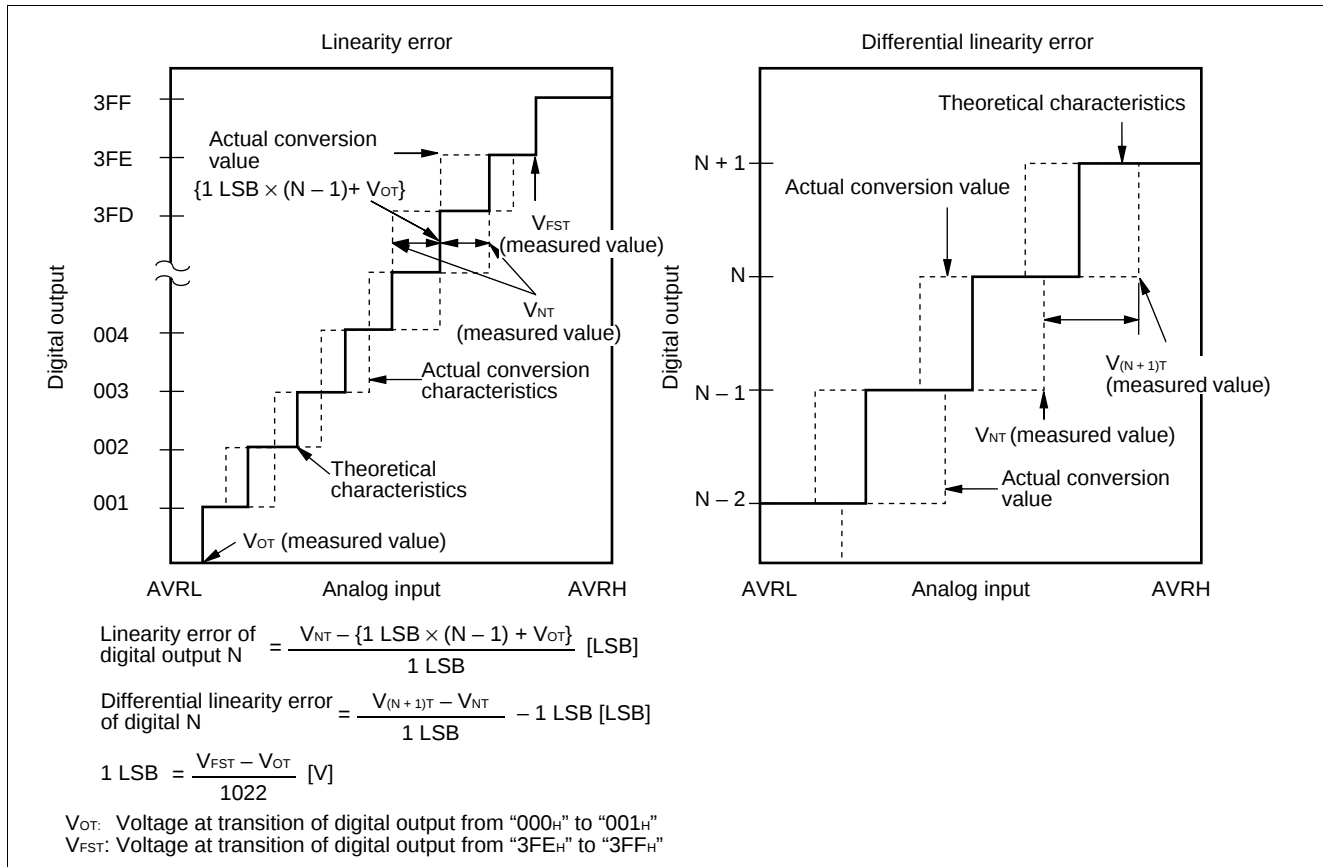
$$V_{FST} (\text{Theoretical value}) = \text{AVRH} - 1.5 \text{ LSB} [\text{V}]$$

$$\text{Total error for digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + 0.5 \text{ LSB}\}}{1 \text{ LSB}} [\text{LSB}]$$

$V_{NT}$ : Voltage at a transition of digital output from  $(N - 1)$  to  $N$

(Continued)

(Continued)



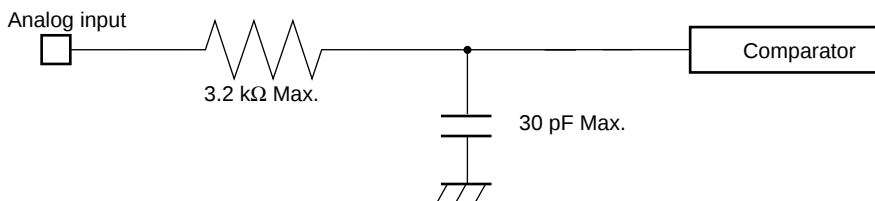
## 7. Notes on Using A/D Converter

Select the output impedance value for the external circuit of analog input according to the following conditions, :

- Output impedance values of the external circuit of 15 kΩ or lower are recommended.
- When capacitors are connected to external pins, the capacitance of several thousand times the internal capacitor value is recommended to minimized the effect of voltage distribution between the external capacitor and internal capacitor.

When the output impedance of the external circuit is too high, the sampling period for analog voltages may not be sufficient (sampling period = 4.00 μs @ machine clock of 16 MHz).

### • Equipment of analog input circuit model



Note: Listed values must be considered as standards.

### • Error

The smaller the  $|AVRH - AVRL|$ , the greater the error would become relatively.

# MB90590/590G Series

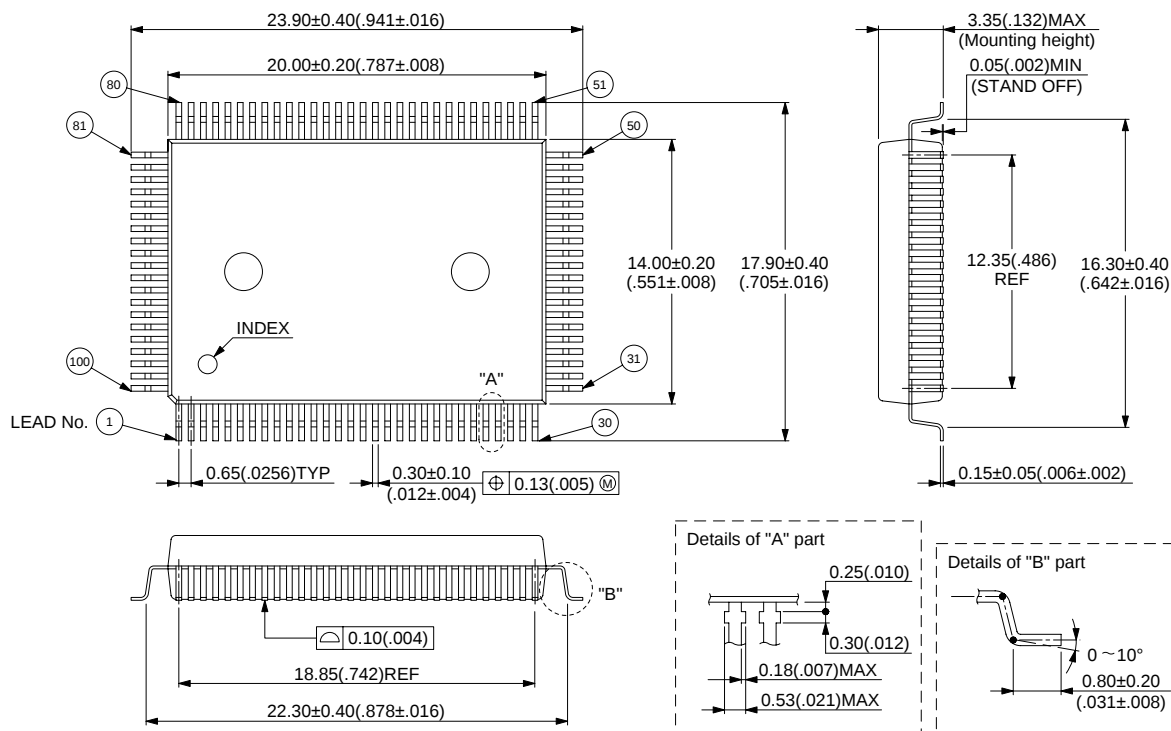
## ■ ORDERING INFORMATION

| Part number                                                                       | Package                               | Remarks        |
|-----------------------------------------------------------------------------------|---------------------------------------|----------------|
| MB90594PF<br>MB90591PF<br>MB90594GPF<br>MB90F594GPF<br>MB90F594APF<br>MB90F591APF | 100-pin Plastic QFP<br>(FPT-100P-M06) |                |
| MB90V590ACR<br>MB90V590GCR                                                        | 256-pin Ceramic PGA<br>(PGA-256C-A01) | For evaluation |

# MB90590/590G Series

## ■ PACKAGE DIMENSION

100-pin plastic QFP  
(FPT-100P-M06)



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Dimensions in mm (inches)

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