National Semiconductor

May 2003

LMH6624/LMH6626
Single/Dual Ultra Low Noise Wideband Operational Amplifier

General Description

The LMH6624/LMH6626 offer wide bandwidth (1.5GHz for single, 1.3GHz for dual) with very low input noise (0.92nV/$\sqrt{Hz}$, 2.3pA/$\sqrt{Hz}$) and ultra low dc errors (100µV V_{OS}, ±0.1µV/˚C drift) providing very precise operational amplifiers with wide dynamic range. This enables the user to achieve closed-loop gains of greater than 10, in both inverting and non-inverting configurations.

The LMH6624 (single) and LMH6626's (dual) traditional voltage feedback topology provide the following benefits: balanced inputs, low offset voltage and offset current, very low offset drift, 81dB open loop gain, 95dB common mode rejection ratio, and 88dB power supply rejection ratio.

The LMH6624/LMH6626 operate from ± 2.5V to ± 6V in dual supply mode and from +5V to +12V in single supply configuration.

LMH6624 is offered in SOT23-5 and SOIC-8 packages.

The LMH6626 is offered in SOIC-8 and MSOP-8 packages.

Features

V_S = ±6V, T_A = 25˚C, A_V = 20, (Typical values unless specified)

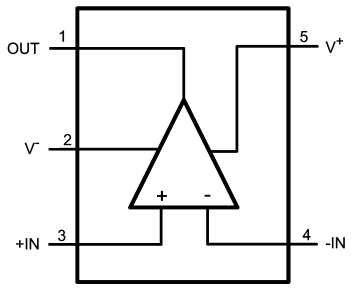
- Gain bandwidth (LMH6624) 1.5GHz
- Input voltage noise 0.92nV/$\sqrt{Hz}$
- Input offset voltage (limit over temp) 700uV
- Slew rate 350V/µs
- Slew rate (A_V = 10) 400V/µs
- HD2 @ f = 10MHz, R_L = 100Ω –63dBc
- HD3 @ f = 10MHz, R_L = 100Ω –80dBc
- Supply voltage range (dual supply) ±2.5V to ±6V
- Supply voltage range (single supply) +5V to +12V
- Improved replacement for the CLC425 (LMH6624)
- Stable for closed loop $|A_V| \geq 10$

Applications

- Instrumentation sense amplifiers
- Ultrasound pre-amps
- Magnetic tape & disk pre-amps
- Wide band active filters
- Professional Audio Systems
- Opto-electronics
- Medical diagnostic systems

Connection Diagrams

5-Pin SOT23



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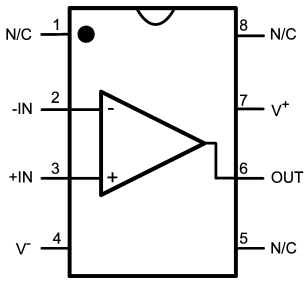
Top View

8–Pin SOIC



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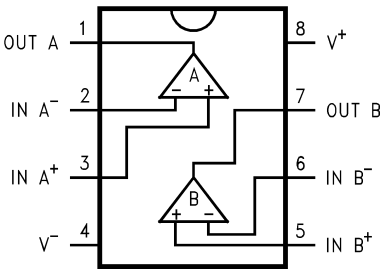
Top View

8–Pin SOIC/MSOP



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Top View

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance	
Human Body Model	2000V (Note 2)
Machine Model	200V (Note 9)
V_{IN} Differential	±1.2V
Supply Voltage (V^+ - V^-)	13.2V
Voltage at Input pins	V^+ +0.5V, V^- −0.5V
Soldering Information	
Infrared or Convection (20 sec.)	235˚C
Wave Soldering (10 sec.)	260˚C
Storage Temperature Range	−65˚C to +150˚C
Junction Temperature (Note 3), (Note 4)	+150˚C

Operating Ratings (Note 1)

Operating Temperature Range (Note 3), (Note 4)	−40˚C to +125˚C
Package Thermal Resistance (θ_{JA})(Note 4)	
SOIC-8	166˚C/W
SOT23–5	265˚C/W
MSOP-8	235˚C/W

±2.5V Electrical Characteristics

Unless otherwise specified, all limits guaranteed at T_A = 25˚C, V^+ = 2.5V, V^- = −2.5V, V_{CM} = 0V, A_V = +20, R_F = 500Ω, R_L = 100Ω. **Boldface** limits apply at the temperature extremes. See (Note 12).

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
Dynamic Performance						
f_{CL}	−3dB BW	V_O = 400mV$_{PP}$ (LMH6624)		90		MHz
		V_O = 400mV$_{PP}$ (LMH6626)		80		
SR	Slew Rate(Note 8)	V_O = 2V$_{PP}$, A_V = +20 (LMH6624)		300		V/µs
		V_O = 2V$_{PP}$, A_V = +20 (LMH6626)		290		
		V_O = 2V$_{PP}$, A_V = +10 (LMH6624)		360		
		V_O = 2V$_{PP}$, A_V = +10 (LMH6626)		340		
t_r	Rise Time	V_O = 400mV Step, 10% to 90%		4.1		ns
t_f	Fall Time	V_O = 400mV Step, 10% to 90%		4.1		ns
t_s	Settling Time 0.1%	V_O = 2V$_{PP}$ (Step)		20		ns
Distortion and Noise Response						
e_n	Input Referred Voltage Noise	f = 1MHz (LMH6624)		0.92		nV/$\sqrt{Hz}$
		f = 1MHz (LMH6626)		1.0		
i_n	Input Referred Current Noise	f = 1MHz (LMH6624)		2.3		pA/$\sqrt{Hz}$
		f = 1MHz (LMH6626)		1.8		
HD2	2nd Harmonic Distortion	f_C = 10MHz, V_O = 1V$_{PP}$, R_L 100Ω		−60		dBc
HD3	3rd Harmonic Distortion	f_C = 10MHz, V_O = 1V$_{PP}$, R_L 100Ω		−76		dBc
Input Characteristics						
V_{OS}	Input Offset Voltage	V_{CM} = 0V	−0.75 **−0.95**	−0.25	+0.75 **+0.95**	mV
	Average Drift (Note 7)	V_{CM} = 0V		±0.25		µV/˚C
I_{OS}	Input Offset Current	V_{CM} = 0V	−1.5 **−2.0**	−0.05	+1.5 **+2.0**	µA
	Average Drift (Note 7)	V_{CM} = 0V		2		nA/˚C
I_B	Input Bias Current	V_{CM} = 0V		13	+20 **+25**	µA
	Average Drift (Note 7)	V_{CM} = 0V		12		nA/˚C
R_{IN}	Input Resistance (Note 10)	Common Mode		6.6		MΩ
		Differential Mode		4.6		kΩ
C_{IN}	Input Capacitance (Note 10)	Common Mode		0.9		pF
		Differential Mode		2.0		
CMRR	Common Mode Rejection Ratio	Input Referred, V_{CM} = −0.5 to +1.9V **V_{CM} = −0.5 to +1.75V**	 87 **85**	 90		dB

±2.5V Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed at T_A = 25˚C, V^+ = 2.5V, V^- = −2.5V, V_{CM} = 0V, A_V = +20, R_F = 500Ω, R_L = 100Ω. **Boldface** limits apply at the temperature extremes. See (Note 12).

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
Transfer Characteristics						
A_{VOL}	Large Signal Voltage Gain	(LMH6624) R_L = 100Ω, V_O = −1V to +1V	75 **70**	79		dB
		(LMH6626) R_L = 100Ω, V_O = −1V to +1V	72 **67**	79		
X_t	Crosstalk Rejection	f = 1MHz (LMH6626)		−75		dB
Output Characteristics						
V_O	Output Swing	R_L = 100Ω	±1.1 **±1.0**	±1.5		V
		No Load	±1.4 **±1.25**	±1.7		
R_O	Output Impedance	f ≤ 100KHz		10		mΩ
I_{SC}	Output Short Circuit Current	(LMH6624) Sourcing to Ground ΔV_{IN} = 200mV (Note 3), (Note 11)	90 **75**	145		mA
		(LMH6624) Sinking to Ground ΔV_{IN} = −200mV (Note 3), (Note 11)	90 **75**	145		
		(LMH6626) Sourcing to Ground ΔV_{IN} = 200mV (Note 3),(Note 11)	60 **50**	120		
		(LMH6626) Sinking to Ground ΔV_{IN} = −200mV (Note 3),(Note 11)	60 **50**	120		
I_{OUT}	Output Current	(LMH6624) Sourcing, V_O = +0.8V Sinking, V_O = −0.8V		100		mA
		(LMH6626) Sourcing, V_O = +0.8V Sinking, V_O = −0.8V		75		
Power Supply						
PSRR	Power Supply Rejection Ratio	V_S = ±2.0V to ±3.0V	82 **80**	90		dB
I_S	Supply Current (per channel)	No Load		11.4	16 **18**	mA

±6V Electrical Characteristics

Unless otherwise specified, all limits guaranteed at T_A = 25˚C, V^+ = 6V, V^- = −6V, V_{CM} = 0V, A_V = +20, R_F = 500Ω, R_L = 100Ω. **Boldface** limits apply at the temperature extremes. See (Note 12).

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
Dynamic Performance						
f_{CL}	−3dB BW	V_O = 400mV$_{PP}$ (LMH6624)		95		MHz
		V_O = 400mV$_{PP}$ (LMH6626)		85		
SR	Slew Rate (Note 8)	V_O = 2V$_{PP}$, A_V = +20 (LMH6624)		350		V/µs
		V_O = 2V$_{PP}$, A_V = +20 (LMH6626)		320		
		V_O = 2V$_{PP}$, A_V = +10 (LMH6624)		400		
		V_O = 2V$_{PP}$, A_V = +10 (LMH6626)		360		
t_r	Rise Time	V_O = 400mV Step, 10% to 90%		3.7		ns

±6V Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed at T_A = 25˚C, V^+ = 6V, V^- = −6V, V_{CM} = 0V, A_V = +20, R_F = 500Ω, R_L = 100Ω. **Boldface** limits apply at the temperature extremes. See (Note 12).

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
t_f	Fall Time	V_O = 400mV Step, 10% to 90%		3.7		ns
t_s	Settling Time 0.1%	V_O = $2V_{PP}$ (Step)		18		ns
Distortion and Noise Response						
e_n	Input Referred Voltage Noise	f = 1MHz (LMH6624)		0.92		$nV/\sqrt{Hz}$
		f = 1MHz (LMH6626)		1.0		
i_n	Input Referred Current Noise	f = 1MHz (LMH6624)		2.3		$pA/\sqrt{Hz}$
		f = 1MHz (LMH6626)		1.8		
HD2	2nd Harmonic Distortion	f_C = 10MHz, V_O = $1V_{PP}$, R_L 100Ω		−63		dBc
HD3	3rd Harmonic Distortion	f_C = 10MHz, V_O = $1V_{PP}$, R_L 100Ω		−80		dBc
Input Characteristics						
V_{OS}	Input Offset Voltage	V_{CM} = 0V	−0.5 **−0.7**	±0.10	+0.5 **+0.7**	mV
	Average Drift (Note 7)	V_{CM} = 0V		±0.2		µV/˚C
I_{OS}	Input Offset Current Average Drift (Note 7)	(LMH6624) V_{CM} = 0V	−1.1 **−2.5**	0.05	1.1 **2.5**	µA
		(LMH6626) V_{CM} = 0V	−2.0 **−2.5**	0.1	2.0 **2.5**	
		V_{CM} = 0V		0.7		nA/˚C
I_B	Input Bias Current	V_{CM} = 0V		13	+20 **+25**	µA
	Average Drift (Note 7)	V_{CM} = 0V		12		nA/˚C
R_{IN}	Input Resistance (Note 10)	Common Mode		6.6		MΩ
		Differential Mode		4.6		kΩ
C_{IN}	Input Capacitance (Note 10)	Common Mode		0.9		pF
		Differential Mode		2.0		
CMRR	Common Mode Rejection Ratio	Input Referred, V_{CM} = −4.5 to +5.25V **V_{CM} = −4.5 to +5.0V**	 90 **87**	 95		dB
Transfer Characteristics						
A_{VOL}	Large Signal Voltage Gain	(LMH6624) R_L = 100Ω, V_O = −3V to +3V	77 **72**	81		dB
		(LMH6626) R_L = 100Ω, V_O = −3V to +3V	74 **70**	80		
X_t	Crosstalk Rejection	f = 1MHz (LMH6626)		−75		dB
Output Characteristics						
V_O	Output Swing	(LMH6624) R_L = 100Ω	±4.4 **±4.3**	±4.9		V
		(LMH6624) No Load	±4.8 **±4.65**	±5.2		
		(LMH6626) R_L = 100Ω	±4.3 **±4.2**	±4.8		
		(LMH6626) No Load	±4.8 **±4.65**	±5.2		
R_O	Output Impedance	f ≤ 100KHz		10		mΩ

±6V Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed at T_A = 25˚C, V^+ = 6V, V^- = −6V, V_{CM} = 0V, A_V = +20, R_F = 500Ω, R_L = 100Ω. **Boldface** limits apply at the temperature extremes. See (Note 12).

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
I_{SC}	Output Short Circuit Current	(LMH6624) Sourcing to Ground ΔV_{IN} = 200mV (Note 3), (Note 11)	100 **85**	156		mA
		(LMH6624) Sinking to Ground ΔV_{IN} = −200mV (Note 3), (Note 11)	100 **85**	156		
		(LMH6626) Sourcing to Ground ΔV_{IN} = 200mV (Note 3), (Note 11)	65 **55**	120		
		(LMH6626) Sinking to Ground ΔV_{IN} = −200mV (Note 3), (Note 11)	65 **55**	120		
I_{OUT}	Output Current	(LMH6624) Sourcing, V_O = +4.3V Sinking, V_O = −4.3V		100		mA
		(LMH6626) Sourcing, V_O = +4.3V Sinking, V_O = −4.3V		80		
Power Supply						
PSRR	Power Supply Rejection Ratio	V_S = ±5.4V to ±6.6V	82 **80**	88		dB
I_S	Supply Current (per channel)	No Load		12	16 **18**	mA

Note 1: Absolute maximum ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5kΩ in series with 100pF.

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150˚C.

Note 4: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: Average drift is determined by dividing the change in parameter at temperature extremes into the total temperature change.

Note 8: Slew rate is the slowest of the rising and falling slew rates.

Note 9: Machine Model, 0Ω in series with 200pF.

Note 10: Simulation results.

Note 11: Short circuit test is a momentary test. Output short circuit duration is 1.5ms.

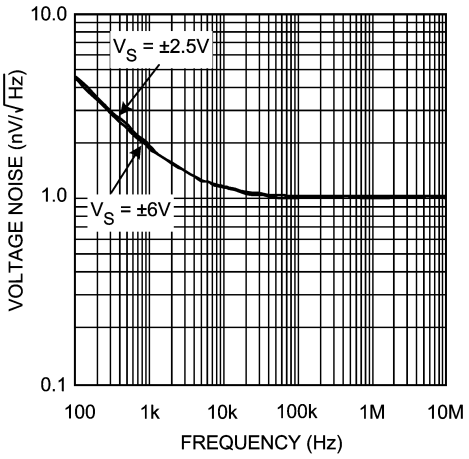
Note 12: Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$. Absolute maximum ratings indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.

Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
SOT23-5	LMH6624MF	A94A	1k Units Tape and Reel	MF05A
	LMH6624MFX		3k Units Tape and Reel	
SOIC-8	LMH6624MA	LMH6624MA	95 Units/Rail	M08A
	LMH6624MAX		2.5k Units Tape and Reel	
SOIC-8	LMH6626MA	LMH6626MA	95 Units/Rail	M08A
	LMH6626MAX		2.5k Units Tape and Reel	
MSOP-8	LMH6626MM	A98A	1k Units Tape and Reel	MUA08A
	LMH6626MMX		3.5k Units Tape and Reel	

Typical Performance Characteristics

Voltage Noise vs. Frequency



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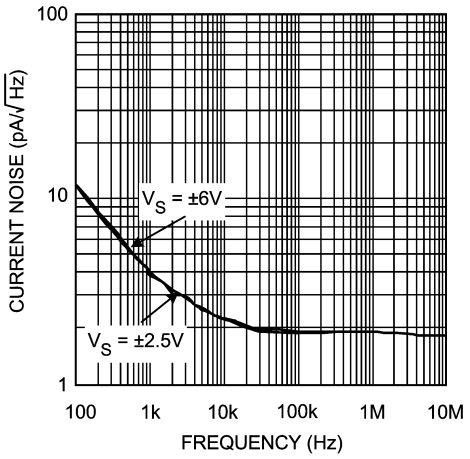
Current Noise vs. Frequency



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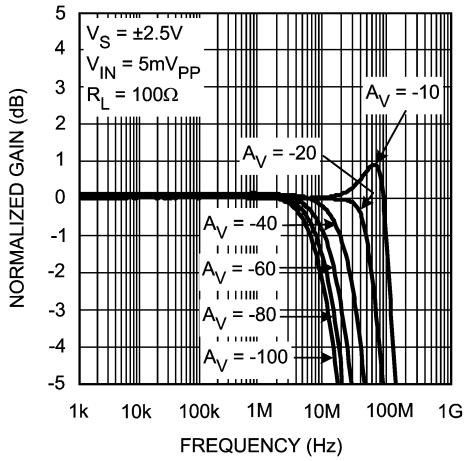
Inverting Frequency Response



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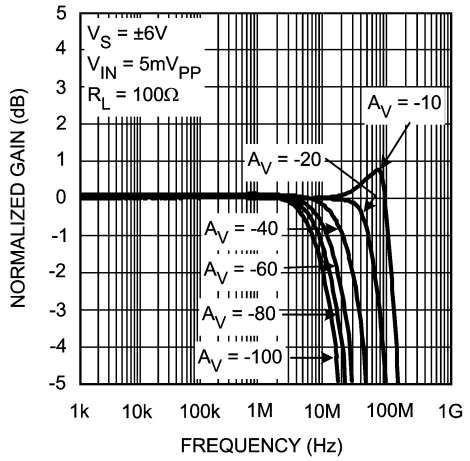
Inverting Frequency Response



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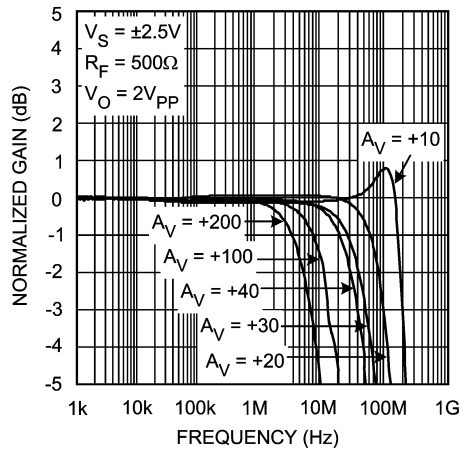
Non-Inverting Frequency Response



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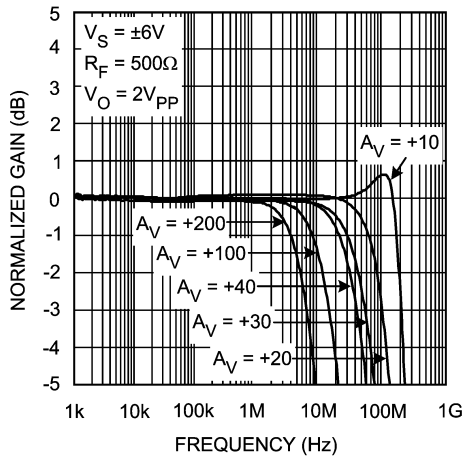
Non-Inverting Frequency Response



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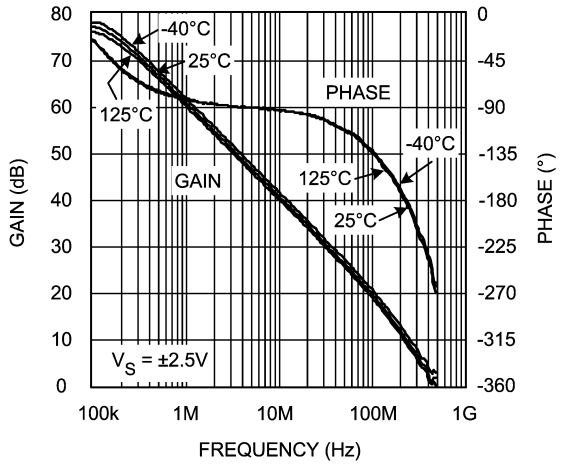
Typical Performance Characteristics (Continued)

Open Loop Frequency Response Over Temperature



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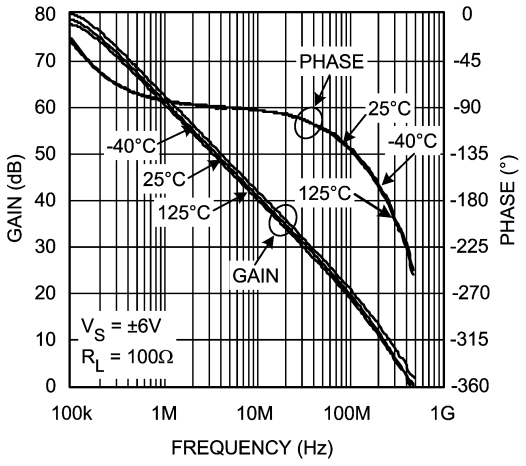
Open Loop Frequency Response Over Temperature



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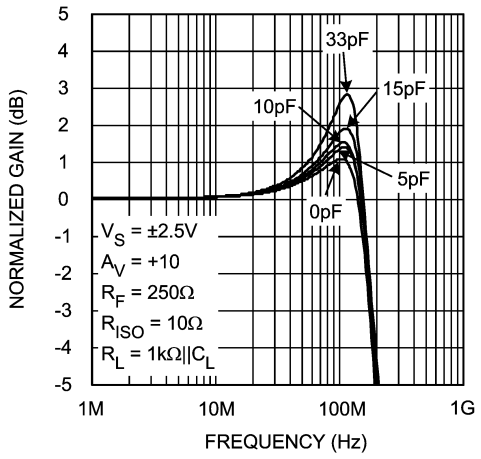
Frequency Response with Cap. Loading



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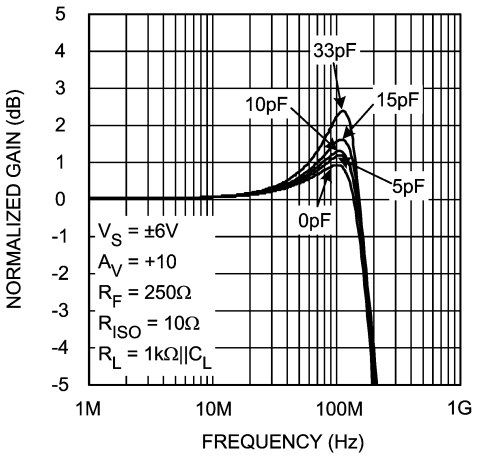

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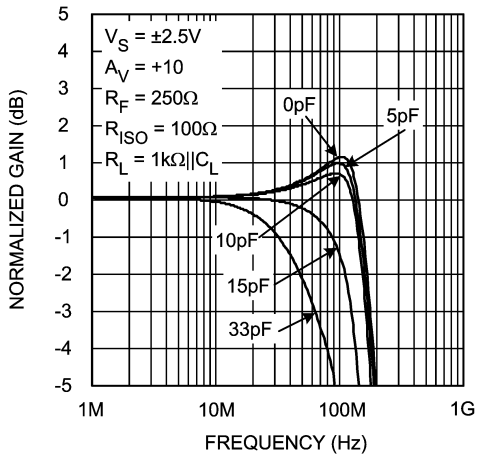

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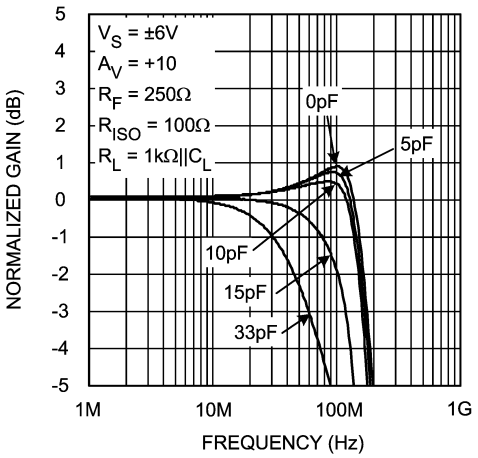

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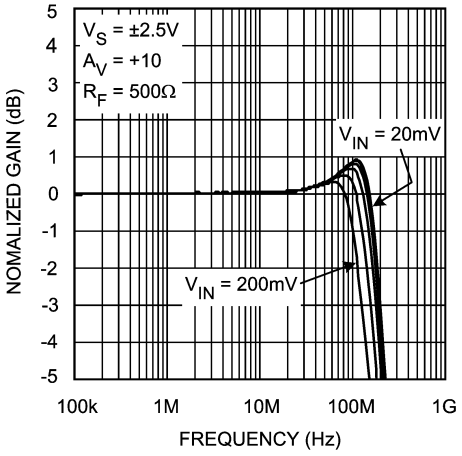
Typical Performance Characteristics (Continued)

Non-Inverting Frequency Response Varying V_{IN}



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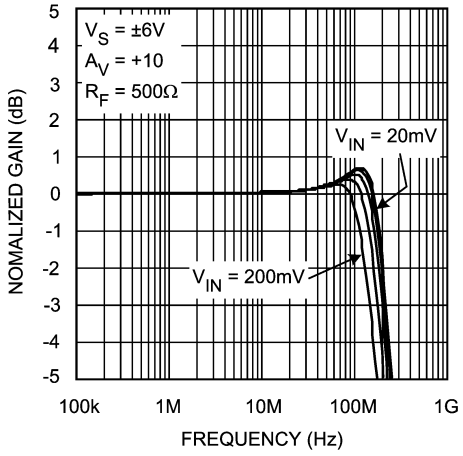
Non-Inverting Frequency Response Varying V_{IN}



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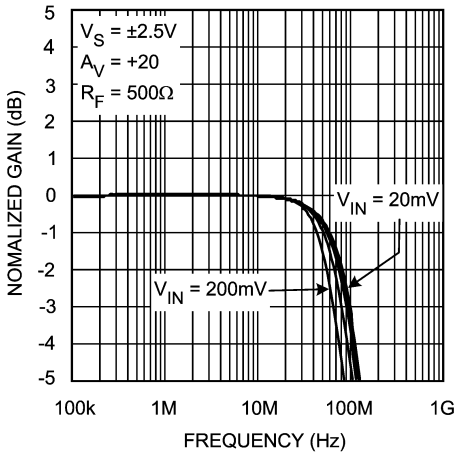
Non-Inverting Frequency Response Varying V_{IN} (LMH6624)



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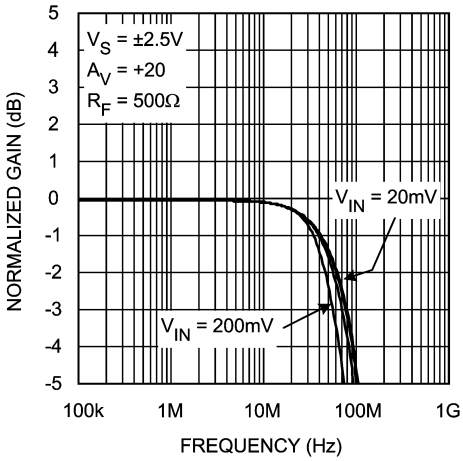
Non-Inverting Frequency Response Varying V_{IN} (LMH6626)



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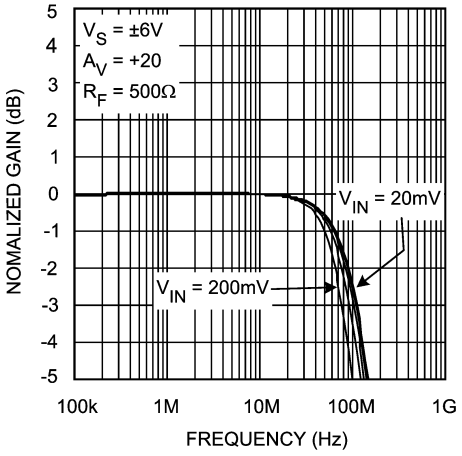
Non-Inverting Frequency Response Varying V_{IN} (LMH6624)



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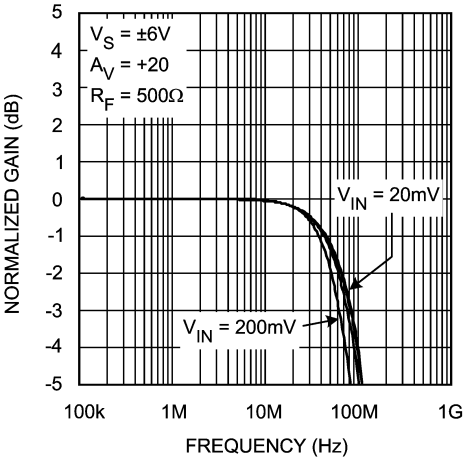
Non-Inverting Frequency Response Varying V_{IN} (LMH6626)



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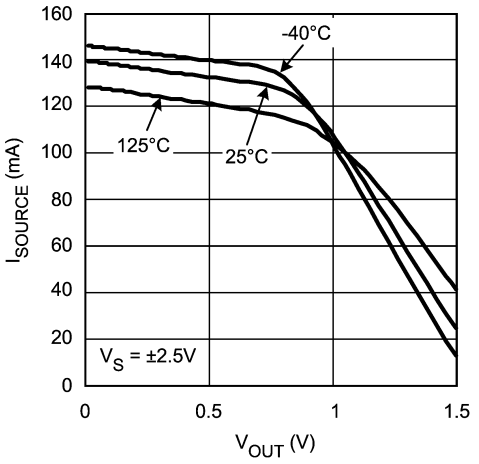
Typical Performance Characteristics (Continued)

Sourcing Current vs. V_{OUT} (LMH6624)



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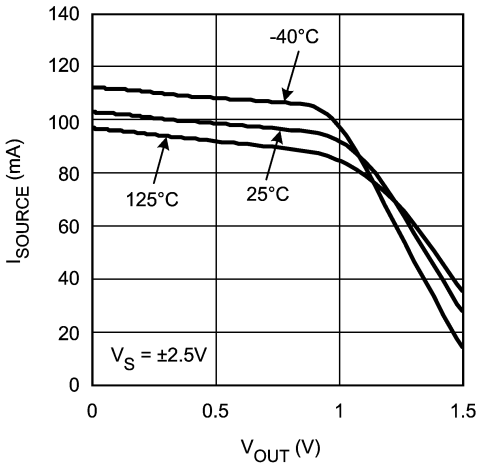
Sourcing Current vs. V_{OUT} (LMH6626)



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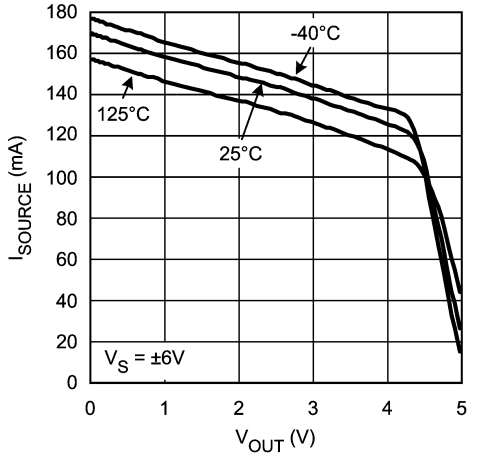
Sourcing Current vs. V_{OUT} (LMH6624)



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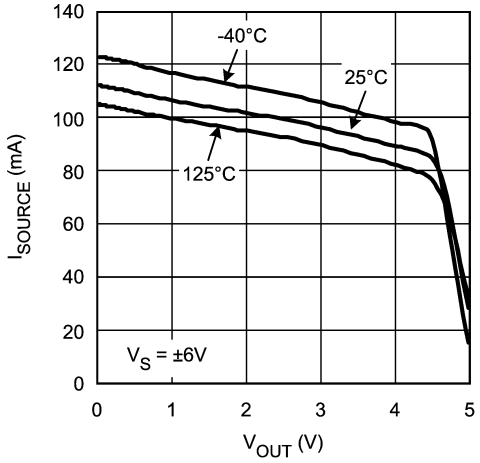
Sourcing Current vs. V_{OUT} (LMH6626)



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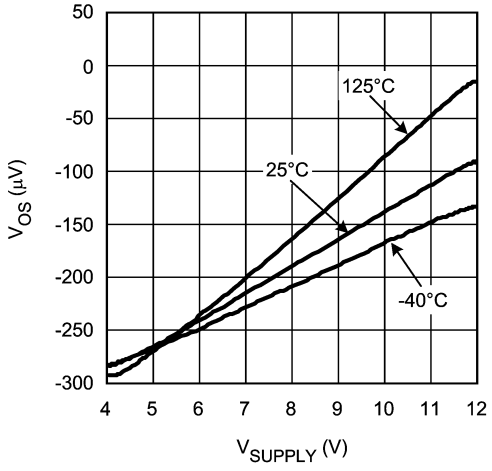
V_{OS} vs. V_{SUPPLY} (LMH6624)



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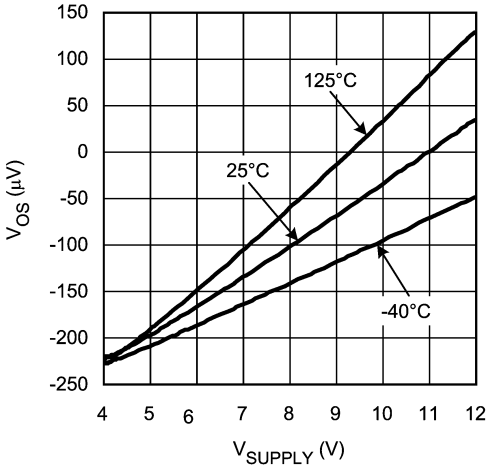
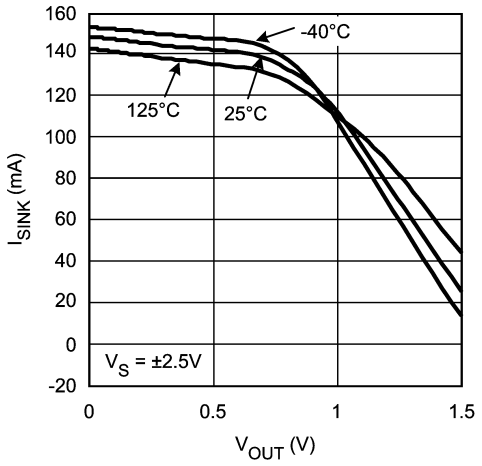
V_{OS} vs. V_{SUPPLY} (LMH6626)



20058968

Typical Performance Characteristics (Continued)

Sinking Current vs. V_{OUT} (LMH6624)



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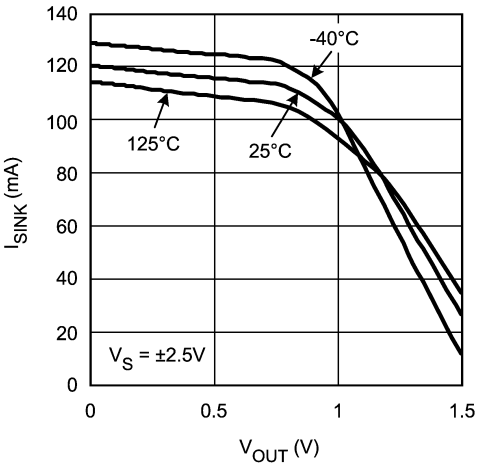
Sinking Current vs. V_{OUT} (LMH6626)



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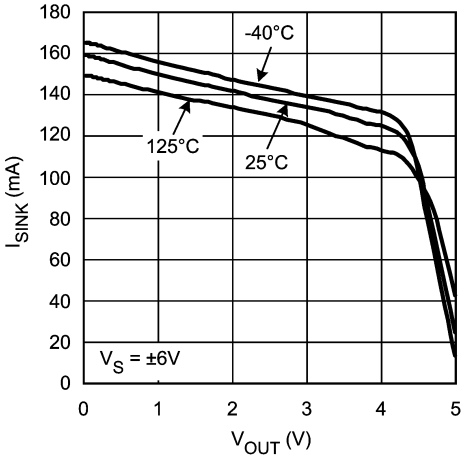
Sinking Current vs. V_{OUT} (LMH6624)



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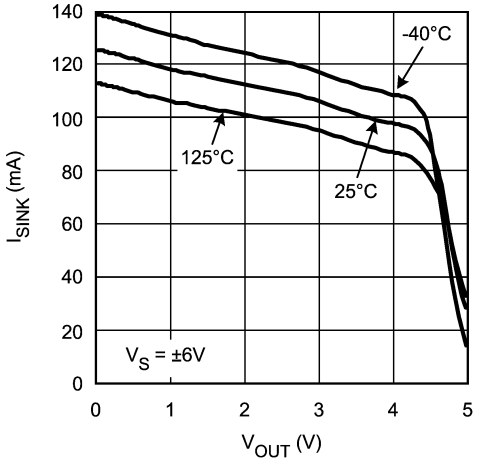
Sinking Current vs. V_{OUT} (LMH6626)



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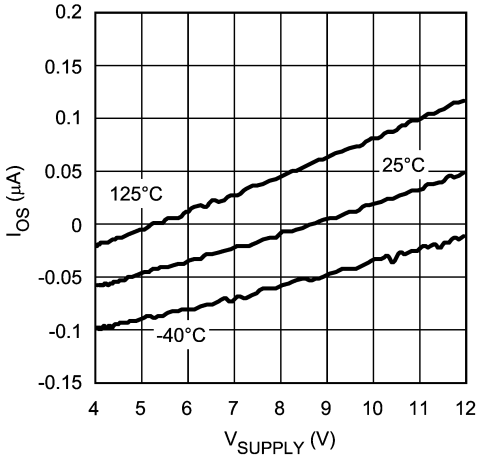
I_{OS} vs. V_{SUPPLY}



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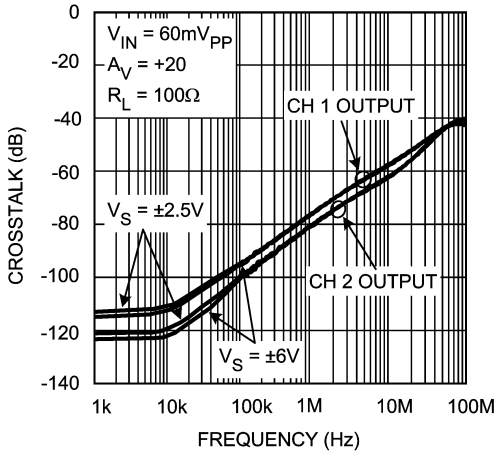
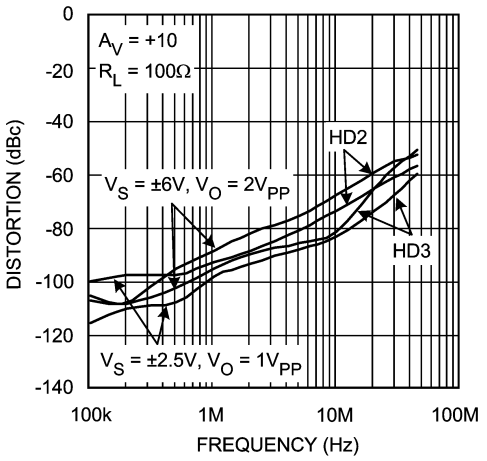
Crosstalk Rejection vs. Frequency (LMH6626)



20058979

Typical Performance Characteristics (Continued)

Distortion vs. Frequency



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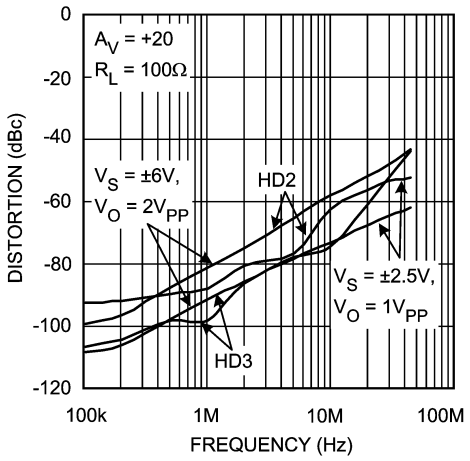
Distortion vs. Frequency



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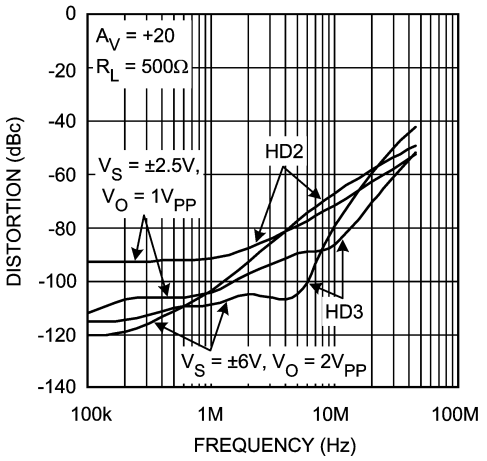
Distortion vs. Frequency



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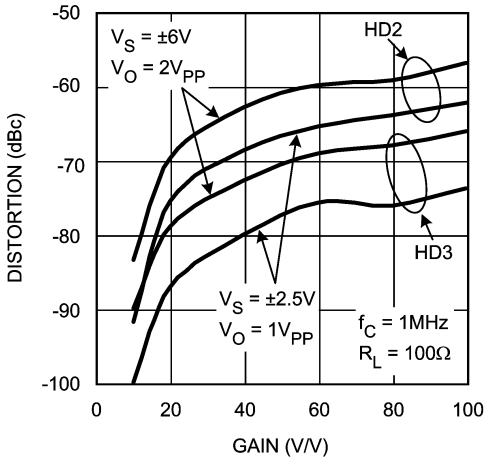
Distortion vs. Gain



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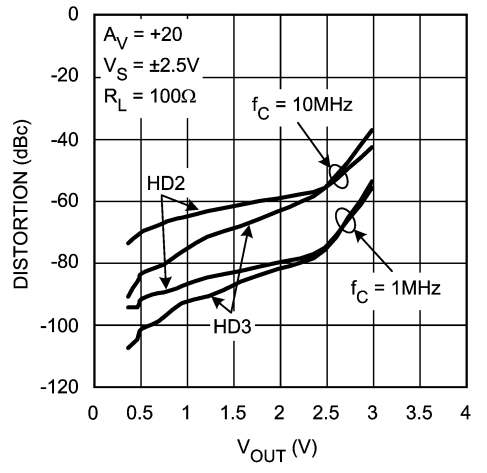
Distortion vs. V_{OUT} Peak to Peak



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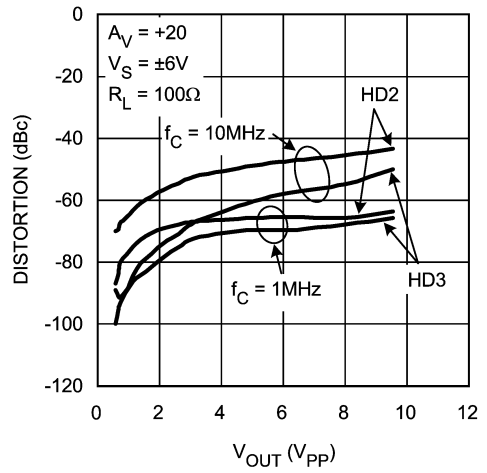
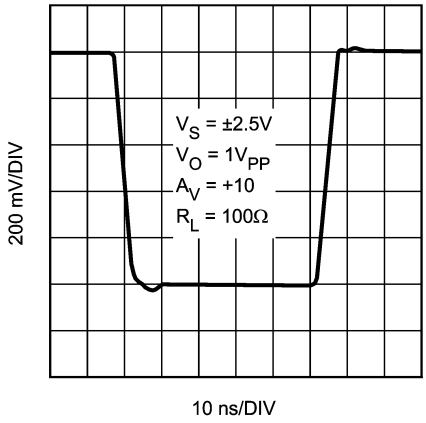
Distortion vs. V_{OUT} Peak to Peak



20058977

Typical Performance Characteristics (Continued)

Non-Inverting Large Signal Pulse Response



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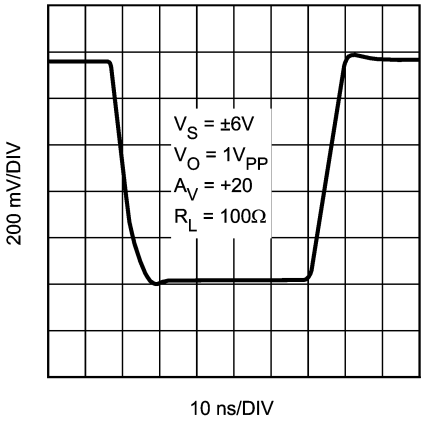
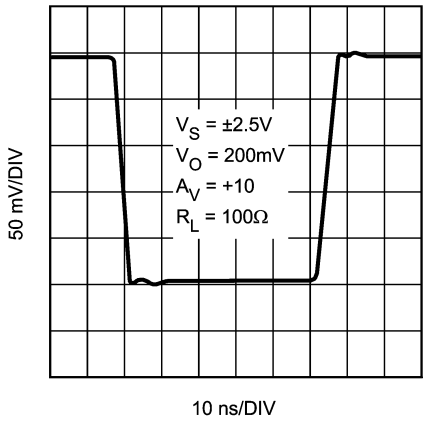
Non-Inverting Large Signal Pulse Response



20058974

Non-Inverting Small Signal Pulse Response



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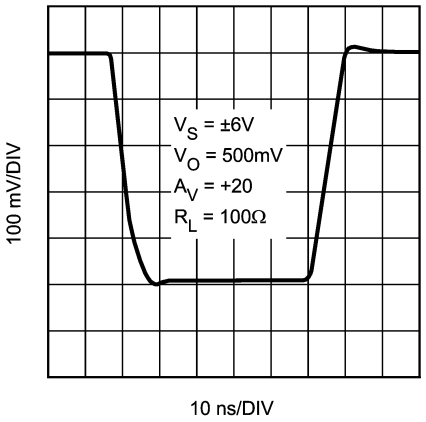
Non-Inverting Small Signal Pulse Response



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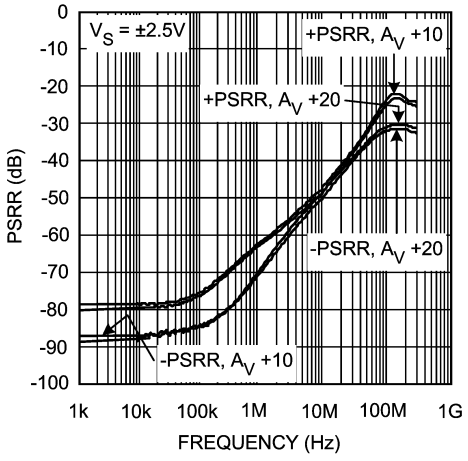
PSRR vs. Frequency



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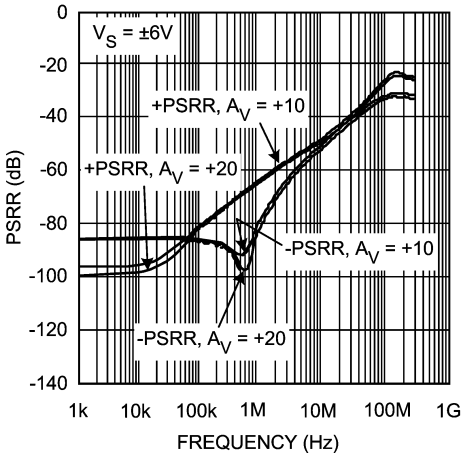
PSRR vs. Frequency



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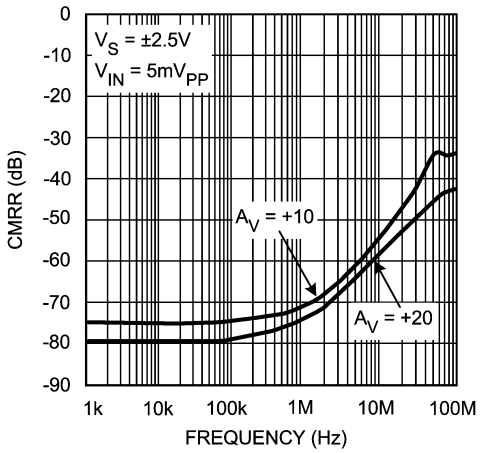
Typical Performance Characteristics (Continued)

Input Referred CMRR vs. Frequency



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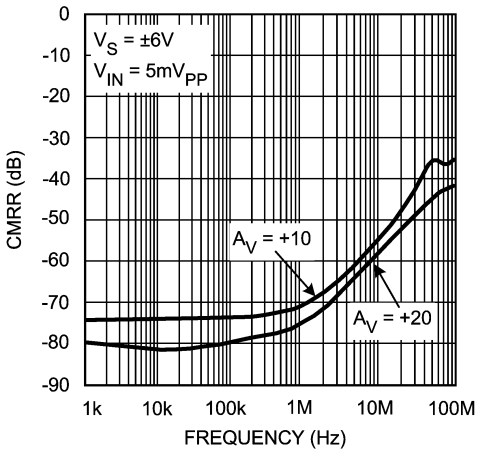
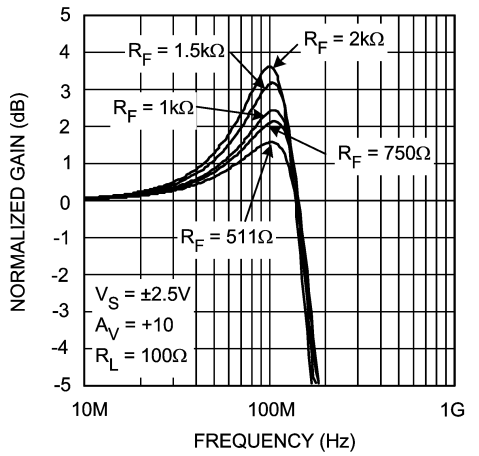
Input Referred CMRR vs. Frequency



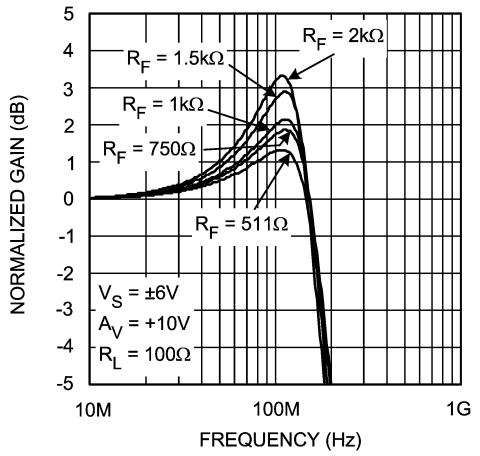
20058902

Amplifier Peaking with Varying R_F



20058983

Amplifier Peaking with Varying R_F



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Application Section

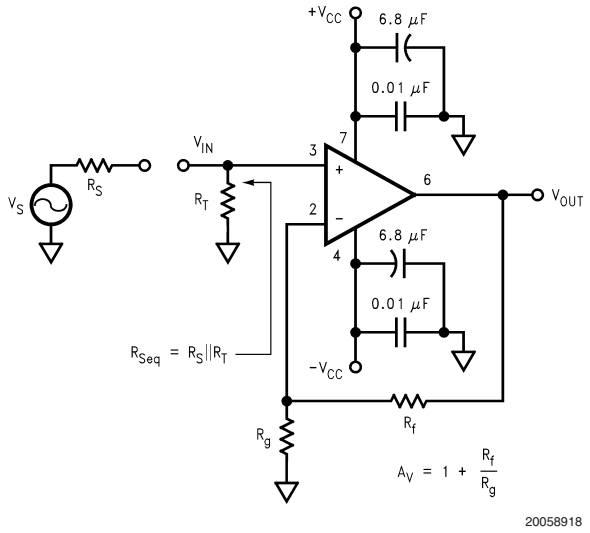


FIGURE 1. Non-Inverting Amplifier Configuration

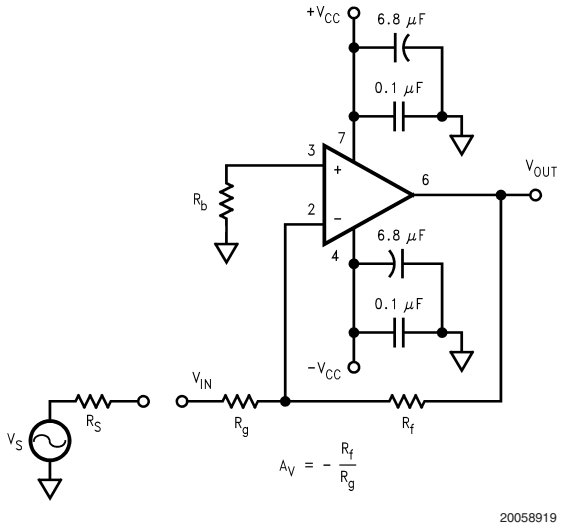


FIGURE 2. Inverting Amplifier Configuration

INTRODUCTION

The LMH6624/LMH6626 are very wide gain bandwidth, ultra low noise voltage feedback operational amplifiers. Their excellent performances enable applications such as medical diagnostic ultrasound, magnetic tape & disk storage and fiber-optics to achieve maximum high frequency signal-to-noise ratios. The set of characteristic plots in the "Typical Performance" section illustrates many of the performance trade offs. The following discussion will enable the proper selection of external components to achieve optimum system performance.

BIAS CURRENT CANCELLATION

To cancel the bias current errors of the non-inverting configuration, the parallel combination of the gain setting (R_g) and feedback (R_f) resistors should equal the equivalent source resistance (R_{seq}) as defined in *Figure 1*. Combining this constraint with the non-inverting gain equation also seen in *Figure 1*, allows both R_f and R_g to be determined explicitly from the following equations:

$$R_f = A_V R_{seq} \text{ and } R_g = R_f/(A_V-1)$$

When driven from a 0Ω source, such as the output of an op amp, the non-inverting input of the LMH6624/LMH6626 should be isolated with at least a 25Ω series resistor.

As seen in *Figure 2*, bias current cancellation is accomplished for the inverting configuration by placing a resistor (R_b) on the non-inverting input equal in value to the resistance seen by the inverting input ($R_f||(R_g+R_s)$). R_b should to be no less than 25Ω for optimum LMH6624/LMH6626 performance. A shunt capacitor can minimize the additional noise of R_b.

TOTAL INPUT NOISE vs. SOURCE RESISTANCE

To determine maximum signal-to-noise ratios from the LMH6624/LMH6626, an understanding of the interaction between the amplifier's intrinsic noise sources and the noise arising from its external resistors is necessary.

Figure 3 describes the noise model for the non-inverting amplifier configuration showing all noise sources. In addition to the intrinsic input voltage noise (e_n) and current noise ($i_n = i_n^+ = i_n^-$) source, there is also thermal voltage noise ($e_t = \sqrt{(4KTR)}$) associated with each of the external resistors. Equation 1 provides the general form for total equivalent input voltage noise density (e_{ni}). Equation 2 is a simplification of Equation 1 that assumes

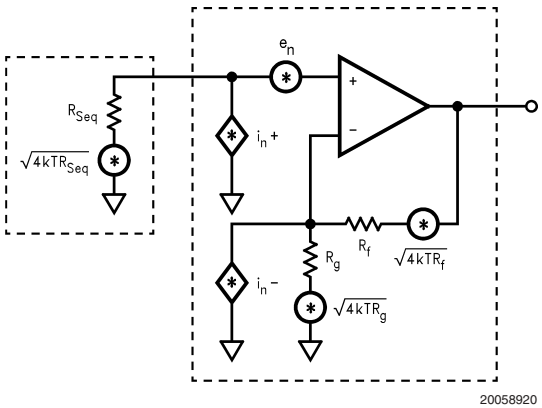


FIGURE 3. Non-Inverting Amplifier Noise Model

Application Section (Continued)

$$e_{ni} = \sqrt{e_n^2 + \left(i_{n+} R_{Seq}\right)^2 + 4kTR_{Seq} + \left(i_{n-}\left(R_f||R_g\right)\right)^2 + 4kT\left(R_f||R_g\right)} \quad (1)$$

$R_f||R_g = R_{seq}$ for bias current cancellation. *Figure 4* illustrates the equivalent noise model using this assumption. *Figure 5* is a plot of e_{ni} against equivalent source resistance (R_{seq}) with all of the contributing voltage noise source of Equation 2. This plot gives the expected e_{ni} for a given (R_{seq}) which assumes $R_f||R_g = R_{seq}$ for bias current cancellation. The total equivalent output voltage noise (e_{no}) is $e_{ni}*A_V$.

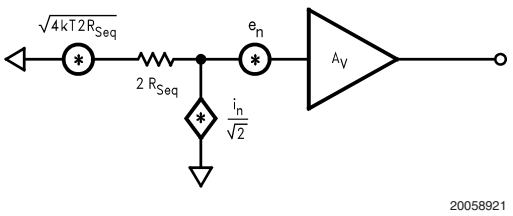


FIGURE 4. Noise Model with $R_f||R_g = R_{seq}$

$$e_{ni} = \sqrt{e_n^2 + 2(i_n R_{Seq})^2 + 4kT(2R_{Seq})} \quad (2)$$

As seen in *Figure 5*, e_{ni} is dominated by the intrinsic voltage noise (e_n) of the amplifier for equivalent source resistances below 33.5Ω. Between 33.5Ω and 6.43kΩ, e_{ni} is dominated by the thermal noise ($e_t = \sqrt{(4kT(2R_{seq}))}$ of the external resistor. Above 6.43kΩ, e_{ni} is dominated by the amplifier's current noise ($i_n = \sqrt{(2)}\ i_n R_{seq}$). When R_{seq} = 464Ω (ie., $e_n/\sqrt{(2)}\ i_n$) the contribution from voltage noise and current noise of LMH6624/LMH6626 is equal.. For example, configured with a gain of +20V/V giving a –3dB of 90MHz and driven from R_{seq} = 25Ω, the LMH6624 produces a total equivalent input noise voltage (e_{ni} x $\sqrt{Hz}$ 1.57*90MHz) of 16.5μV_{rms}.

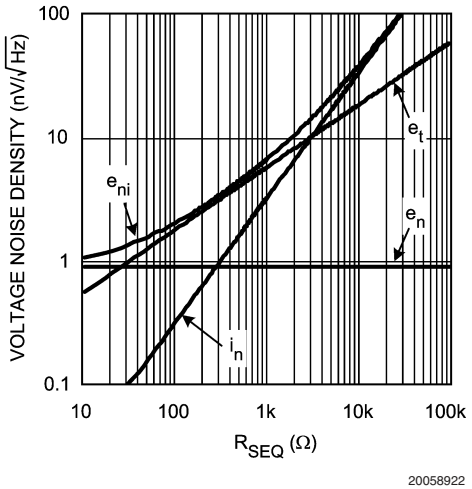


FIGURE 5. Voltage Noise Density vs. Source Resistance

If bias current cancellation is not a requirement, then $R_f||R_g$ need not equal R_{seq}. In this case, according to Equation 1, $R_f||R_g$ should be as low as possible to minimize noise. Results similar to Equation 1 are obtained for the inverting configuration of *Figure 2* if R_{seq} is replaced by R_b and R_g is replaced by $R_g + R_s$. With these substitutions, Equation 1 will yield an e_{ni} referred to the non-inverting input. Referring e_{ni} to the inverting input is easily accomplished by multiplying e_{ni} by the ratio of non-inverting to inverting gains.

NOISE FIGURE

Noise Figure (NF) is a measure of the noise degradation caused by an amplifier.

$$NF = 10LOG\left\{\frac{S_i / N_i}{S_o / N_o}\right\} = 10LOG\left\{\frac{e_{ni}^2}{e_t^2}\right\} \quad (3)$$

The Noise Figure formula is shown in Equation 3. The addition of a terminating resistor R_T, reduces the external thermal noise but increases the resulting NF. The NF is increased because R_T reduces the input signal amplitude thus reducing the input SNR.

$$NF = 10\ LOG\left[\frac{e_n^2 + i_n^2(R_{Seq}^2 + (R_f||R_g)^2) + 4KT\,(R_{Seq} + (R_f||R_g))}{4KT\,(R_{Seq} + (R_f||R_g))}\right] \quad (4)$$

The noise figure is related to the equivalent source resistance (R_{seq}) and the parallel combination of R_f and R_g. To minimize noise figure.

- Minimize $R_f||R_g$
- Choose the Optimum R_S (R_{OPT})

R_{OPT} is the point at which the NF curve reaches a minimum and is approximated by:

$$R_{OPT} \approx e_n/i_n$$

NON-INVERTING GAINS LESS THAN 10V/V

Using the LMH6624/LMH6626 at lower non-inverting gains requires external compensation such as the shunt compensation as shown in *Figure 6*. The compensation capacitors are chosen to reduce frequency response peaking to less than 1dB.

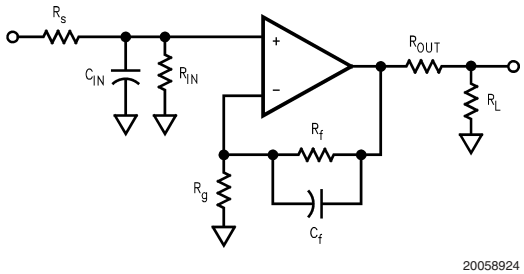


FIGURE 6. External Shunt Compensation

INVERTING GAINS LESS THAN 10V/V

The lag compensation of *Figure 7* will achieve stability for lower gains. It is best used for the inverting configuration because of its affect on the non-inverting input impedance.

Application Section (Continued)

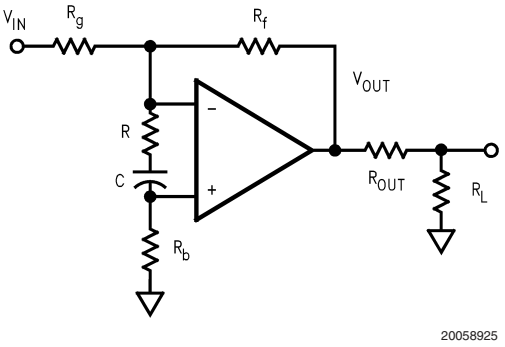


FIGURE 7. External Lag Compensation

SINGLE SUPPLY OPERATION

The LMH6624/LMH6626 can be operated with single power supply as shown in *Figure 8*. Both the input and output are capacitively coupled to set the DC operating point.

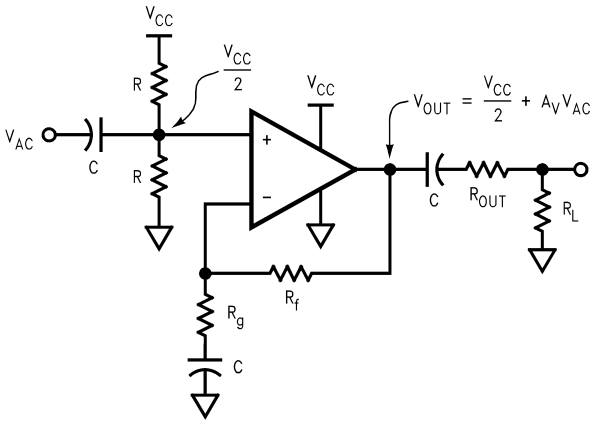


FIGURE 8. Single Supply Operation

LOW NOISE TRANSIMPEDANCE AMPLIFIER

Figure 9 implements a low-noise transimpedance amplifier commonly used with photo-diodes. The transimpedance gain is set by R_f. Equation 4 provides the total input current noise density (i_{ni}) equation for the basic transimpedance configuration and is plotted against feedback resistance (R_f) showing all contributing noise sources in *Figure 10*. This plot indicates the expected total equivalent input current noise density (i_{ni}) for a given feedback resistance (R_f). The total equivalent output voltage noise density (e_{no}) is i_{ni}*R_f.

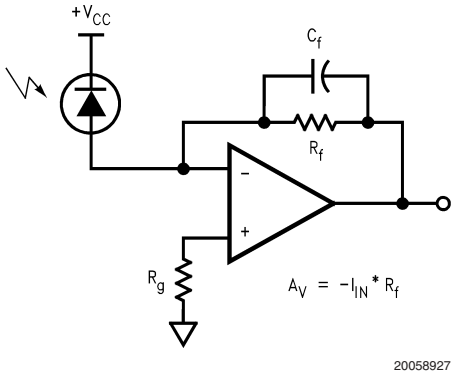


FIGURE 9. Transimpedance Amplifier Configuration

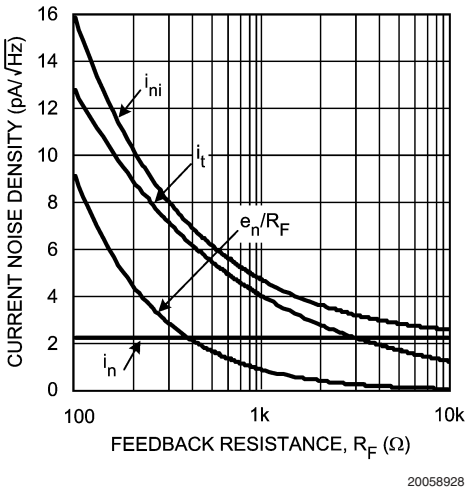


FIGURE 10. Current Noise Density vs. Feedback Resistance

$$i_{ni} = \sqrt{i_n^2 + \left(\frac{e_n}{R_f}\right)^2 + \frac{4kT}{R_f}} \quad (5)$$

LOW NOISE INTEGRATOR

The LMH6624/LMH6626 implement a deBoo integrator shown in *Figure 11*. Positive feedback maintains integration linearity. The LMH6624/LMH6626's low input offset voltage and matched inputs allow bias current cancellation and provide for very precise integration. Keeping R_G and R_S low helps maintain dynamic stability.

Application Section (Continued)

$$V_O \cong V_{IN} \frac{K_O}{sR_SC} \quad ; \quad K_O = 1 + \frac{R_F}{R_G}$$

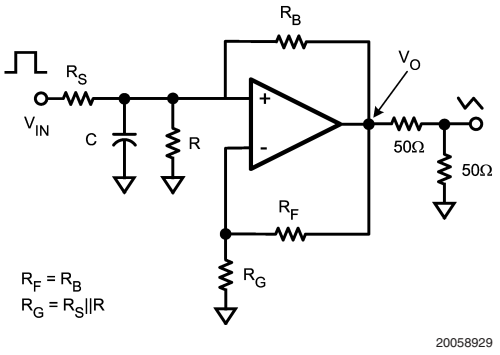


FIGURE 11. Low Noise Integrator

HIGH-GAIN SALLEN-KEY ACTIVE FILTERS

The LMH6624/LMH6626 are well suited for high gain Sallen-Key type of active filters. *Figure 12* shows the 2nd order Sallen-Key low pass filter topology. Using component predistortion methods discussed in OA-21 enables the proper selection of components for these high-frequency filters.

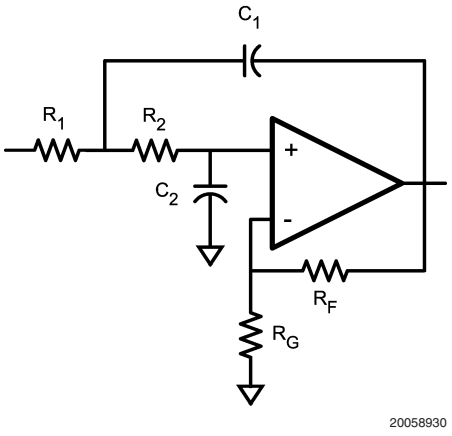
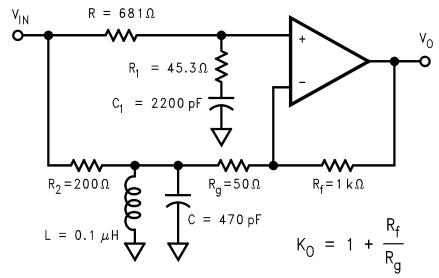


FIGURE 12. Sallen-Key Active Filter Topology

LOW NOISE MAGNETIC MEDIA EQUALIZER

The LMH6624/LMH6626 implement a high-performance low noise equalizer for such application as magnetic tape channels as shown in *Figure 13*. The circuit combines an integrator with a bandpass filter to produce the low noise equalization. The circuit's simulated frequency response is illustrated in *Figure 14*.



$$\frac{V_O}{V_{IN}} = K_O \left(\frac{sC_1R_1 + 1}{sC_1(R_1 + R) + 1} - \left(\frac{R_f}{R_f + R_g} \right) \frac{sLR_g}{s^2LCR_2R_g + sL(R_2 + R_g) + R_2R_g} \right)$$

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FIGURE 13. Noise Magnetic Media Equalizer

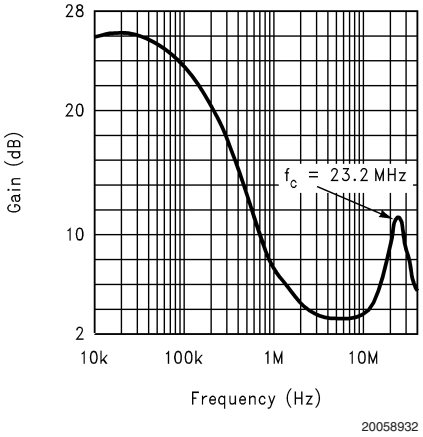


FIGURE 14. Equalizer Frequency Response

LAYOUT CONSIDERATION

National Semiconductor suggests the copper patterns on the evaluation boards listed below as a guide for high frequency layout. These boards are also useful as an aid in device testing and characterization. As is the case with all high-speed amplifiers, accepted-practice RF design technique on the PCB layout is mandatory. Generally, a good high frequency layout exhibits a separation of power supply and ground traces from the inverting input and output pins. Parasitic capacitances between these nodes and ground may cause frequency response peaking and possible circuit oscillations (see Application Note OA-15 for more information). Use high quality chip capacitors with values in the range of 1000pF to 0.1F for power supply bypassing. One terminal of each chip capacitor is connected to the ground plane and the other terminal is connected to a point that is as close as possible to each supply pin as allowed by the manufacturer's design rules. In addition, connect a tantalum capacitor with a value between 4.7μF and 10μF in parallel with the chip capacitor. Signal lines connecting the feedback and gain resistors should be as short as possible to minimize inductance and microstrip line effect. Place input and output termination resistors as close as possible to the input/output pins. Traces greater than 1 inch in length should be impedance matched to the corresponding load termination.

Application Section (Continued)

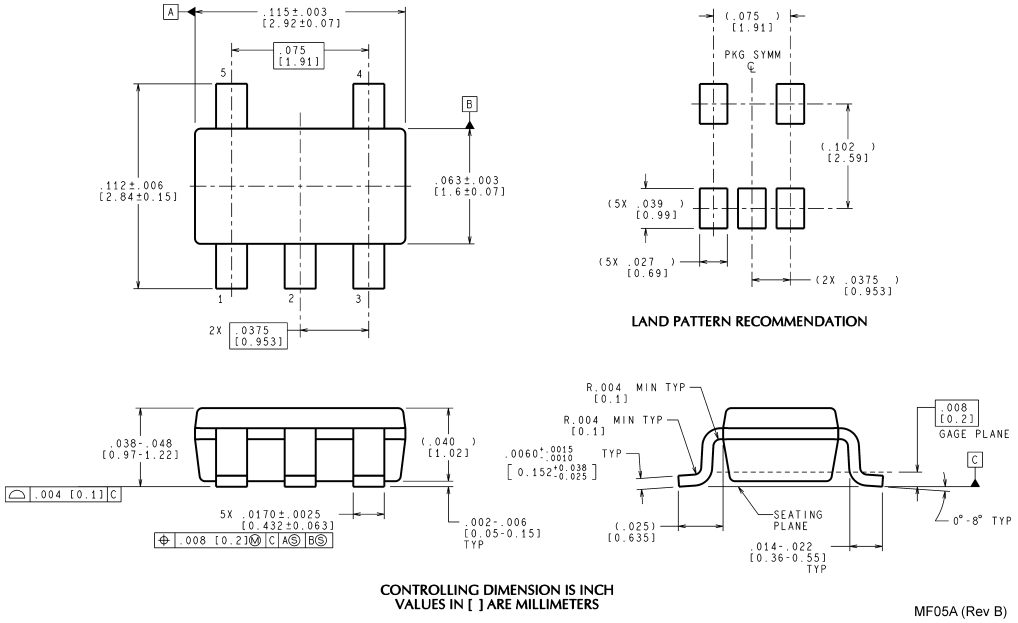
Symmetry between the positive and negative paths in the layout of differential circuitry should be maintained to minimize the imbalance of amplitude and phase of the differential signal.

These free evaluation boards are shipped when a device sample request is placed with National Semiconductor.

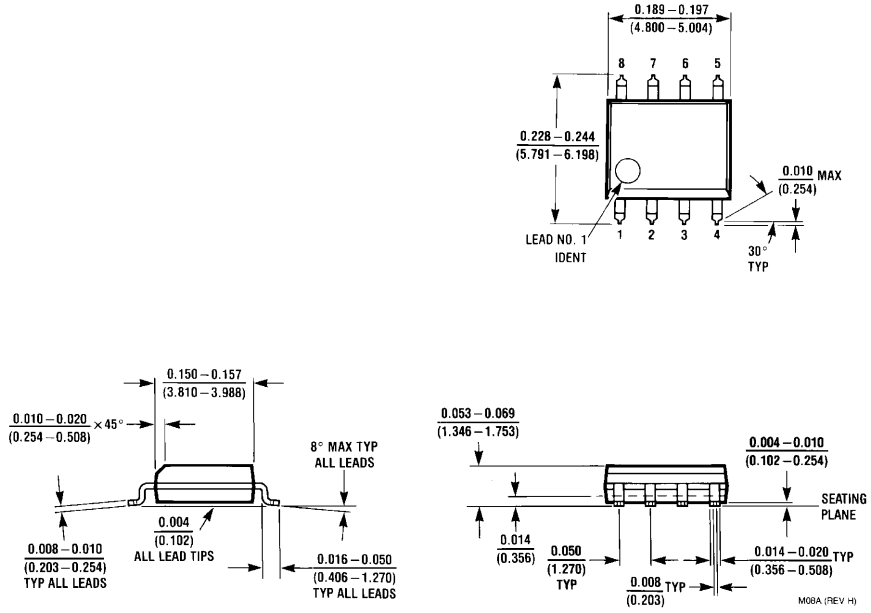
Component value selection is another important parameter in working with high speed/high performance amplifiers. Choosing external resistors that are large in value compared to the value of other critical components will affect the closed loop behavior of the stage because of the interaction of these resistors with parasitic capacitances. These parasitic capacitors could either be inherent to the device or be a by-product of the board layout and component placement. Moreover, a large resistor will also add more thermal noise to the signal path. Either way, keeping the resistor values low will diminish this interaction. On the other hand, choosing very low value resistors could load down nodes and will contribute to higher overall power dissipation and high distortion.

Device	Package	Evaluation Board Part Number
LMH6624MF	SOT23–5	CLC730216
LMH6624MA	SOIC-8	CLC730227
LMH6626MA	SOIC-8	CLC730036
LMH6626MM	MSOP-8	CLC730123

Physical Dimensions inches (millimeters) unless otherwise noted

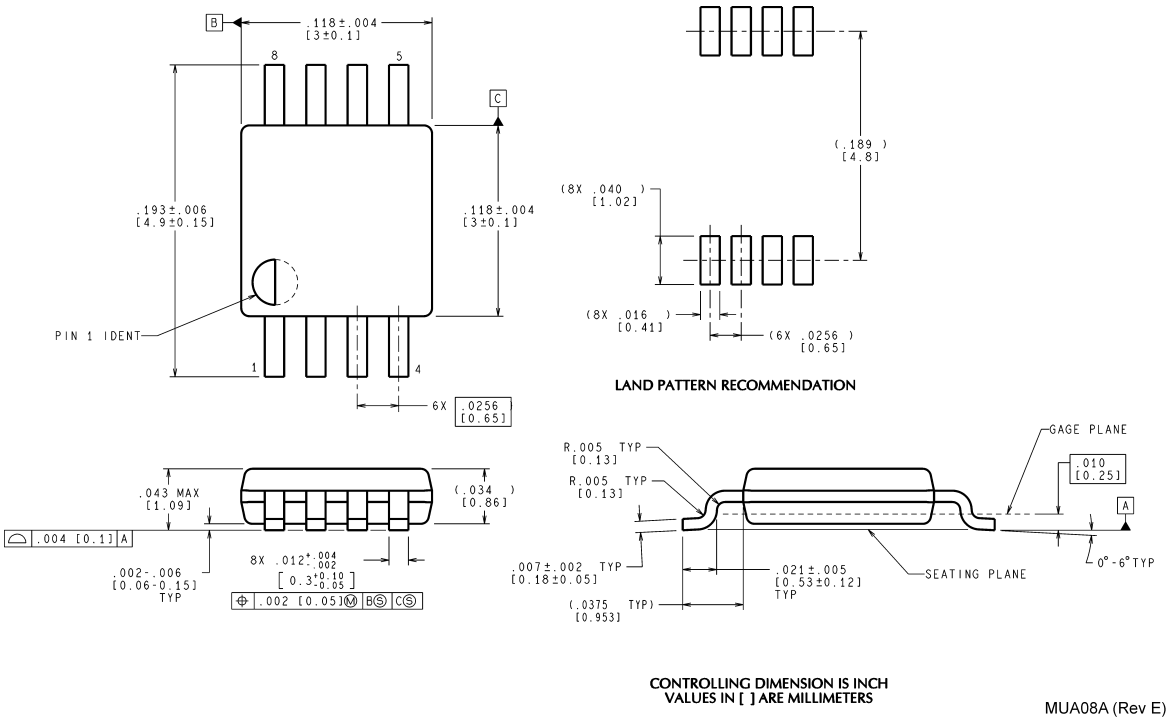


5-Pin SOT23
NS Package Number MF05A



8-Pin SOIC
NS Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



8-Pin MSOP
NS Package Number MUA08A

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