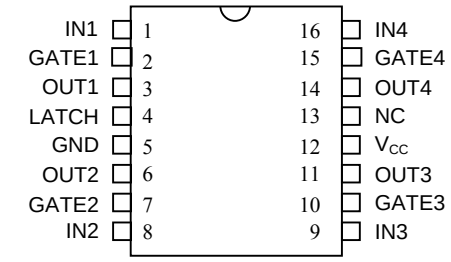
DS1640/DS1640C
Personal Computer Power FET

www.dalsemi.com

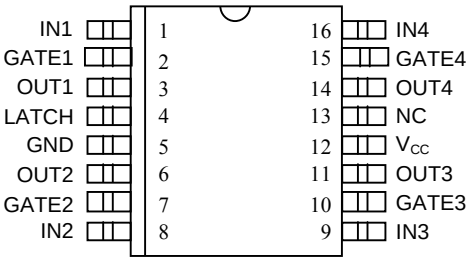
FEATURES

- Contains four P channel power FET switches that can each supply over 300 mA @ 0.2 volts drop
- Controlled directly from CMOS or TTL level signals
- Fast switching time of less than 10 µs at rated supply current
- 16-pin DIP or 16-pin SOIC surface mount package
- Positive logic signal turns each FET on and ground or low level signal turns each FET off
- Off condition allows less than 50 nA of current flow
- Low control gate capacitance of less than 5 pF
- FET gates can either follow inputs or be latched
- Designed for use with power supplies ranging from +3 to +5 volts

PIN ASSIGNMENT



16-Pin DIP (300-mil)
See Mech. Drawings Section



16-Pin DIP SOIC (300-mil)
See Mech. Drawings Section

PIN DESCRIPTION

V_{CC}	- +3 to +5 Volt Input
GND	- Ground
IN1-IN4	- FET Sources
OUT1-OUT4	- FET Drains
GATE1-GATE4	- FET Control Gates
NC	- No Connection
LATCH	- Gate Inputs Latch Control

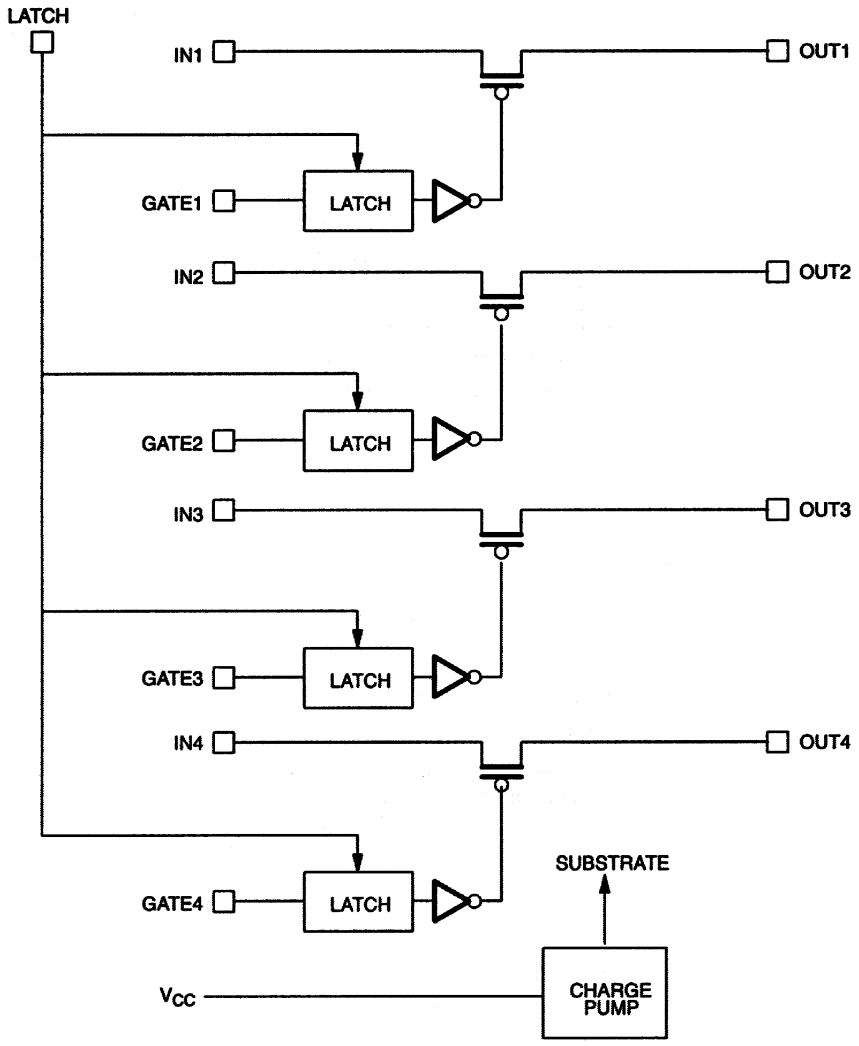
DESCRIPTION

The DS1640 contains four P channel power MOS FETs designed as switches to conserve power in personal computer systems. When connected to power management control units, power consuming devices like disk drives or display panel backlights can be routinely shut down to conserve battery or main power supply energy. The P channel power MOS FETs are individually controlled and are capable of handling 300 mA each continuously with less than 0.2 volts drop from input to output. The device requires a +3 Û +5 volt power supply input which is used to power internal logic and to operate a gate bias generator.

OPERATION

With +3 Û +5 volts applied between the V_{CC} pin and ground, any one of four inputs can be connected or disconnected from its respective output based on the bias applied to the control gate (see Figure 1). A set of four internal latches is controlled by the latch input. The logic levels passed to the FET gates are controlled by the gate inputs and latch pin status. When the latch pin is logic 0, the gate input levels are inverted and passed directly to the control gates, enabling the switches to be switched both independently and asynchronously. With a transition from logic 0 to logic 1 on the latch pin, the input levels present on the gate inputs are locked by the four internal latches, maintaining the corresponding FET gates at those levels. As long as the latch input is maintained at logic 1, the FET gate levels are maintained. When the latch input is returned to logic 0, the gate inputs again are inverted and passed to the FET control gates without being latched. A TTL or CMOS logic 1 turns a switch completely on and TTL or CMOS logic 0 turns a switch completely off. The four switches can be operated independently or two or more can be connected in parallel for added current carrying capability. The four switches contained within the DS1640 are not designed to be operated in a linear manner. When V_{CC} is not applied to the DS1640 or if V_{CC} is not within nominal limits, the output levels and current carrying capability of the four switches are not guaranteed. When all four gate inputs are off (logic 0) the device enters a low V_{CC} current standby mode because the onboard charge pump is turned off. The gate and latch inputs are CMOS-compatible throughout the entire V_{CC} range and are TTL-compatible when V_{CC} falls between 4.5 and 5.5V.

DS1640 BLOCK DIAGRAM Figure 1



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	3.0		5.5	V	1, 2
Logic 0 Input 3.0 V < V_{CC} < 4.5 V	V_{IL2}	-0.3		+0.5	V	
Logic 0 Input 4.5 V < V_{CC} < 5.0 V	V_{IL1}	-0.3		+0.8	V	1
Logic 1 Input 3.0 V < V_{CC} < 5.0 V	V_{IH}	2.0		V_{CC} +0.5	V	1, 7
Source Voltage	V_{SOURCE}			V_{CC} +0.5	V	1, 7

DC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC} = +5V + 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CC1}		0.3	1	mA	3
Supply Current	I_{CC2}		0.1	1	µA	4
Switch Off Leakage	I_{SL}			100	nA	
Switch On Resistance	R_{ON}		0.3	0.67	Ω	
Switch Current @ V_F = 200 mV	I_S			300	mA	5
Input Leakage	I_{IL}	-1		+1	µA	6
Gate Input Capacitance	C_G			5	pF	7

DC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC} = +5V + 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Switching Time (OFF → ON)	t_{STON}			10	µs	
Switching Time (ON → OFF)	t_{STOFF}			10	µs	
Minimum Time to Engage Latch	t_{LM}			50	ns	

NOTES:

1. All voltages are referenced to ground.

2. When V_{CC} is below minimum limits output levels are not guaranteed.

3. I_{CC1} is the supply current with one or more switches on.

4. I_{CC2} is when all switches are off and all inputs are within 0.5V of a supply rail.

5. Each switch is capable of carrying 300 mA maximum at 200 mV forward drop.

6. Input leakage applies to the four gate inputs and the latch input only.

7. Applies to each of four gate inputs and the latch input.

Dallas Semiconductor devices are built to the highest quality standards and manufactured for long term reliability. All DS1640 devices are made using the same quality materials and manufacturing methods. However, consumer versions of the DS1640 are not exposed to environmental stresses that some commercial device manufacturing flows require. Devices that are designated as consumer product have a "C" designator in the product number. For example, the DS1640C is a consumer grade product.