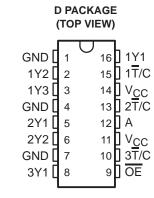
SCAS334A - DECEMBER 1992 - REVISED NOVEMBER 1995

- Low Output Skew for Clock-Distribution and Clock-Generation Applications
- TTL-Compatible Inputs and Outputs
- Distributes One Clock Input to Six Clock Outputs
- Polarity Control Selects True or Complementary Outputs
- Distributed V<sub>CC</sub> and GND Pins Reduce Switching Noise
- High-Drive Outputs (-48-mA I<sub>OH</sub>, 48-mA I<sub>OL</sub>)
- State-of-the-Art EPIC-IIB™ BiCMOS Design Significantly Reduces Power Dissipation
- Packaged in Plastic Small-Outline Package



### description

The CDC391 contains a clock-driver circuit that distributes one input signal to six outputs with minimum skew for clock distribution. Through the use of the polarity-control  $(\overline{T}/C)$  inputs, various combinations of true and complementary outputs can be obtained. The output-enable  $(\overline{OE})$  input is provided to disable the outputs to a high-impedance state.

The CDC391 is characterized for operation from −40°C to 85°C.

**FUNCTION TABLE** 

	INPUTS		OUTPUT
OE	T/C	Α	Υ
Н	Х	Χ	Z
L	L	L	L
L	L	Н	Н
L	Н	L	Н
L	Н	Н	L

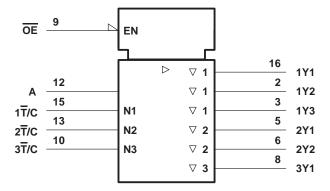


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

EPIC-IIB is a trademark of Texas Instruments Incorporated

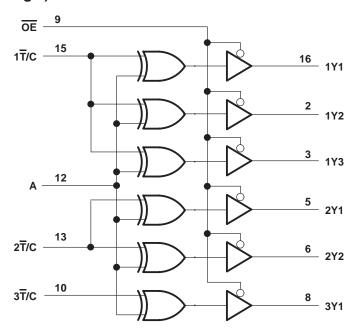


# logic symbol†



<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)





SCAS334A - DECEMBER 1992 - REVISED NOVEMBER 1995

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

S	upply voltage range, V <sub>CC</sub>		$\dots$ $-0.5$ V to 7 V
Ir	put voltage range, V <sub>I</sub> (see Note 1)		$\dots$ $-0.5$ V to 7 V
V	oltage range applied to any output in the high state or power-off state, VO	0.5	$V \text{ to V}_{CC} + 0.5 \text{ V}$
C	urrent into any output in the low state, IO		96 mA
Ir	put clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)		–18 mA
C	utput clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)		50 mA
Ν	aximum power dissipation at $T_A = 55^{\circ}C$ (in still air) (see Note 2)		0.77 W
S	torage temperature range, T <sub>stg</sub>		-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

## recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.75	5	5.25	V
VIH	High-level input voltage	2			V
V <sub>IL</sub>	Low-level input voltage			0.8	V
VI	Input voltage	0		VCC	V
I <sub>OH</sub>	High-level output current			-48	mA
I <sub>OL</sub>	Low-level output current			48	mA
Δt/Δν	Input transition rise or fall rate			5	ns/V
fclock	Input clock frequency			100	MHz
TA	Operating free-air temperature	-40		85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN -	TYP‡ M	ΑХ	UNIT
VIK	$V_{CC} = 4.75 \text{ V},$	$I_{I} = -18 \text{ mA}$			_	1.2	V
Voн	$V_{CC} = 4.75 \text{ V},$	$I_{OH} = -48 \text{ mA}$		2			V
V <sub>OL</sub>	$V_{CC} = 4.75 \text{ V},$	$I_{OL} = 48 \text{ mA}$				0.5	V
lj	$V_{CC} = 5.25 \text{ V},$	$V_I = V_{CC}$ or GND				±1	μΑ
loz	$V_{CC} = 5.25 \text{ V},$	$V_O = V_{CC}$ or GND			±	50	μΑ
ΙΟ <sup>§</sup>	$V_{CC} = 5.25 \text{ V},$	V <sub>O</sub> = 2.5 V		-15	-1	00	mA
			Outputs high			-100 10	
ICC	$V_{CC} = 5.25 \text{ V},$ $V_{I} = V_{CC} \text{ or GND}$	$I_{O} = 0$ ,	Outputs low			40	mA
	AL = ACC OL GIAD	Outputs disabled	10				
C <sub>i</sub>	V <sub>I</sub> = 2.5 V or 0.5 V				3		pF
Co	V <sub>O</sub> = 2.5 V or 0.5 V				5		pF

<sup>‡</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .



<sup>2.</sup> The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 300 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

<sup>§</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

# CDC391 1-LINE TO 6-LINE CLOCK DRIVER WITH SELECTABLE POLARITY AND 3-STATE OUTPUTS

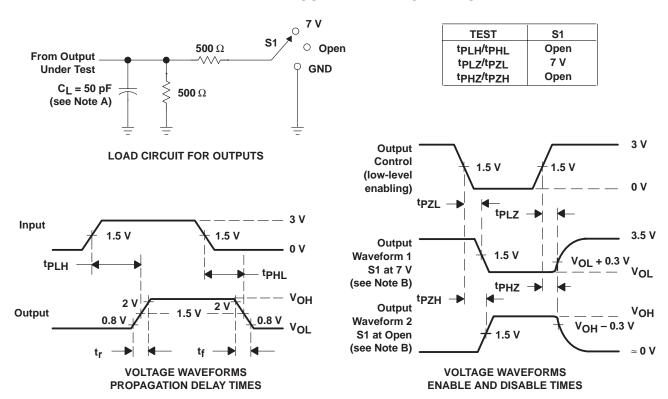
SCAS334A - DECEMBER 1992 - REVISED NOVEMBER 1995

# switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t <sub>PLH</sub>	А	Any Y	1.5	5	no
t <sub>PHL</sub>		Any f	1.5	5	ns
t <sub>PLH</sub>	T/C	Any Y	1.5	5	
<sup>t</sup> PHL	1/C		1.5	5	ns
<sup>t</sup> PZH	ŌĒ	Any Y	1.5	5	no
tPZL		Ally f	3	7	ns
t <sub>PHZ</sub>	ŌĒ	Any Y		5	no
t <sub>PLZ</sub>	OE .	Ally f		5	ns
* * * *	^	Any Y (same phase)		0.5	no
<sup>t</sup> sk(o)	Α	Any Y (any phase)		1	ns
<sup>t</sup> sk(p)	Α	Any Y		1	ns
t <sub>r</sub>				1.5	ns
t <sub>f</sub>				1.5	ns



### PARAMETER MEASUREMENT INFORMATION

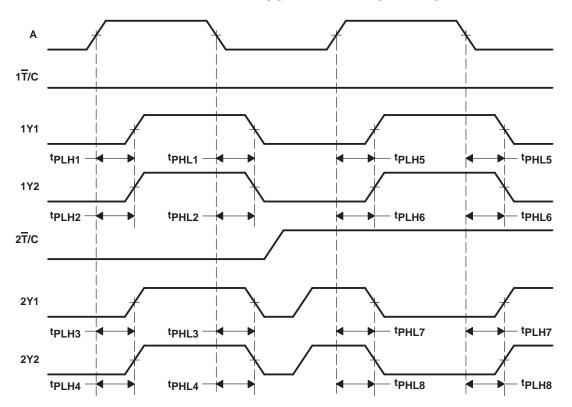


NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_Q = 50 \ \Omega$ ,  $t_f \leq 2.5 \ ns$ .
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

### PARAMETER MEASUREMENT INFORMATION



- NOTES: A. Output skew,  $t_{Sk(0)}$ , from A to any Y (same phase), can be measured only between outputs for which the respective polarity-control inputs  $(\overline{T}/C)$  are at the same logic level. It is calculated as the greater of:
  - The difference between the fastest and slowest of tpLH from A↑ to any Y (e.g., tpLHn, n = 1 to 4; or tpLHn, n = 5 to 6)
  - The difference between the fastest and slowest of tPHL from A↓ to any Y (e.g., tPHLn, n = 1 to 4; or tPHLn, n = 5 to 6)
  - The difference between the fastest and slowest of tp<sub>LH</sub> from A↓ to any Y (e.g., tp<sub>LHn</sub>, n = 7 to 8)
  - The difference between the fastest and slowest of tp<sub>HL</sub> from A↑ to any Y (e.g., tp<sub>HLn</sub>, n = 7 to 8)
  - B. Output skew,  $t_{sk(0)}$ , from A to any Y (any phase), can be measured between outputs for which the respective polarity-control inputs  $(\overline{T}/C)$  are at the same or different logic levels. It is calculated as the greater of:
    - The difference between the fastest and slowest of tp<sub>LH</sub> from A<sup>↑</sup> to any Y or tp<sub>HL</sub> from A<sup>↑</sup> to any Y (e.g., tp<sub>LHn</sub>, n = 1 to 4; or tp<sub>LHn</sub>, n = 5 to 6, and tp<sub>HLn</sub>, n = 7 to 8)
    - The difference between the fastest and slowest of tp<sub>HL</sub> from A↓ to any Y or tp<sub>LH</sub> from A↓ to any Y (e.g., tp<sub>HLn</sub>, n = 1 to 4; or tp<sub>HLn</sub>, n = 5 to 6, and tp<sub>LHn</sub>, n = 7 to 8)

Figure 2. Waveforms for Calculation of t<sub>sk(o)</sub>



#### **IMPORTANT NOTICE**

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.

Copyright © 1998, Texas Instruments Incorporated