

Data sheet acquired from Harris Semiconductor

SCHS124D

January 1998 - Revised September 2003

CD54HC74, CD74HC74, CD54HCT74, CD74HCT74

Dual D Flip-Flop with Set and Reset Positive-Edge Trigger

Features

- · Hysteresis on Clock Inputs for Improved Noise Immunity and Increased Input Rise and Fall Times
- Asynchronous Set and Reset
- Complementary Outputs
- Buffered Inputs
- Typical $f_{MAX} = 50MHz$ at $V_{CC} = 5V$, $C_L = 15pF$, $T_{A} = 25^{\circ}C$
- Fanout (Over Temperature Range)
 - Standard Outputs..... 10 LSTTL Loads - Bus Driver Outputs 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
 - 2V to 6V Operation
 - High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at $V_{CC} = 5V$
- HCT Types
 - 4.5V to 5.5V Operation
 - Direct LSTTL Input Logic Compatibility, V_{IL} = 0.8V (Max), V_{IH} = 2V (Min)
 - CMOS Input Compatibility, $\text{I}_{\text{I}} \leq 1 \mu \text{A}$ at $\text{V}_{\text{OL}}, \, \text{V}_{\text{OH}}$

Description

The 'HC74 and 'HCT74 utilize silicon gate CMOS technology to achieve operating speeds equivalent to LSTTL parts. They exhibit the low power consumption of standard CMOS integrated circuits, together with the ability to drive 10 LSTTL

This flip-flop has independent DATA, SET, RESET and CLOCK inputs and Q and \overline{Q} outputs. The logic level present at the data input is transferred to the output during the positive-going transition of the clock pulse. SET and RESET are independent of the clock and are accomplished by a low level at the appropriate input.

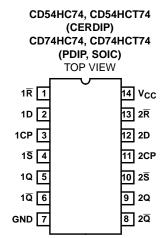
The HCT logic family is functionally as well as pin compatible with the standard LS logic family.

Ordering Information

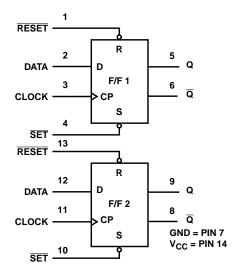
PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC74F3A	-55 to 125	14 Ld CERDIP
CD54HCT74F3A	-55 to 125	14 Ld CERDIP
CD74HC74E	-55 to 125	14 Ld PDIP
CD74HC74M	-55 to 125	14 Ld SOIC
CD74HC74MT	-55 to 125	14 Ld SOIC
CD74HC74M96	-55 to 125	14 Ld SOIC
CD74HCT74E	-55 to 125	14 Ld PDIP
CD74HCT74M	-55 to 125	14 Ld SOIC
CD74HCT74MT	-55 to 125	14 Ld SOIC
CD74HCT74M96	-55 to 125	14 Ld SOIC

NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel. The suffix T denotes a small-quantity reel of

Pinout



Functional Diagram



TRUTH TABLE

	INP	OUTPUTS				
SET	RESET	СР	D	Q	Q	
L	Н	X	Х	Н	L	
Н	L	Х	Х	L	Н	
L	L	Х	Х	H (Note 1)	H (Note 1)	
Н	Н	↑	Н	Н	L	
Н	Н	1	L	L	Н	
Н	Н	L	Х	Q0	Q0	

H= High Level (Steady State)

L= Low Level (Steady State)

X= Don't Care

↑= Low-to-High Transition

Q0 = the level of Q before the indicated input conditions were established.

1. This configuration is nonstable, that is, it will not persist when set and reset inputs return to their inactive (high) level.

Absolute Maximum Ratings

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
E (PDIP) Package	80
M (SOIC) Package	86
Maximum Junction Temperature (Hermetic Package or D	
Maximum Junction Temperature (Plastic Package)	150 ^o C
Maximum Storage Temperature Range65	5°C to 150°C
Maximum Lead Temperature (Soldering 10s)	300°C
(SOIC - Lead Tips Only)	

Operating Conditions

Temperature Range (T _A)55°C to 125°C
Supply Voltage Range, V _{CC}
HC Types2V to 6\
HCT Types
DC Input or Output Voltage, V _I , V _O 0V to V _C (
Input Rise and Fall Time
2V
4.5V 500ns (Max
6V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

		1	ST ITIONS			25°C		-40°C T	O 85°C	-55°C T	O 125°C	
PARAMETER	SYMBOL	V _I (V)	I _O (mA)	V _{CC} (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
HC TYPES												
High Level Input	V _{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
Voltage				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	٧
Low Level Input Voltage	V _{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	٧
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	٧
High Level Output	V _{OH}	V _{IH} or	-0.02	2	1.9	-	-	1.9	-	1.9	-	٧
Voltage CMOS Loads		V_{IL}		4.5	4.4	-	-	4.4	-	4.4	-	V
				6	5.9	-	-	5.9	-	5.9	-	٧
High Level Output			-	-	-	-	-	-	-	-	-	٧
Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output	V _{OL}	V _{IH} or	0.02	2	-	-	0.1	-	0.1	-	0.1	٧
Voltage CMOS Loads		V _{IL}		4.5	-	-	0.1	-	0.1	-	0.1	V
				6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output			-	-	-	-	-	-	-	-	-	V
Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	1	-	0.26	-	0.33	-	0.4	٧
Input Leakage Current	lı	V _{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	μА

DC Electrical Specifications (Continued)

			ST ITIONS			25°C		-40°C TO 85°C		-55°C TO 125°C		
PARAMETER	SYMBOL	V _I (V)	I _O (mA)	V _{CC} (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
Quiescent Device Current	Icc	V _{CC} or GND	0	6	-	-	4	-	40	-	80	μА
HCT TYPES												
High Level Input Voltage	V _{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V _{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V _{OH}	V _{IH} or V _{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V _{OL}	V _{IH} or V _{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I _I	V _{CC} and GND	-	5.5	-		±0.1	-	±1	-	±1	μА
Quiescent Device Current	Icc	V _{CC} or GND	0	5.5	-	-	4	-	40	-	80	μА
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI _{CC} (Note 3)	V _{CC} - 2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μΑ

NOTE:

HCT Input Loading Table

INPUT	UNIT LOADS
D	0.5
R	0.5
СР	0.7
S	0.75

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Specifications table, e.g., $360\mu A$ max at $25^{\circ}C$.

Prerequisite For Switching Specifications

		TEST	v _{cc}		25°C		-40°C TO 85°C		-55°C TO 125°C		
PARAMETER	SYMBOL	CONDITIONS	(V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
HC TYPES											
Data to CP Setup Time	tsu	-	2	60	ı	1	75	-	90	-	ns
(Figure 5)			4.5	12	-	-	15	-	18	-	ns
			6	10	-	-	13	-	15	-	ns

^{3.} For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

Prerequisite For Switching Specifications (Continued)

		TEST	v _{cc}		25°C		-40°C T	O 85°C	-55°C T	O 125°C	
PARAMETER	SYMBOL	CONDITIONS	(V)	MIN	TYP	МАХ	MIN	MAX	MIN	MAX	UNITS
Hold Time (Figure 5)	t _H	-	2	3	-	-	3	-	3	-	ns
			4.5	3	-	-	3	-	3	-	ns
			6	3	-	-	3	-	3	-	ns
Removal Time \overline{R} , \overline{S} , to CP	t _{REM}	-	2	30	-	-	40	-	45	-	ns
(Figure 5)			4.5	6	-	-	8	-	9	-	ns
			6	5	-	-	7	-	8	-	ns
Pulse Width \overline{R} , \overline{S} (Figure 1)	t _W	-	2	80	-	-	100	-	120	-	ns
			4.5	16	-	-	20	-	24	-	ns
			6	14	-	-	17	-	20	-	ns
Pulse Width CP (Figure 1)	t _W	-	2	80	-	-	100	-	120	-	ns
			4.5	16	-	-	20	-	24	-	ns
			6	14	-	-	17	-	20	-	ns
CP Frequency	f _{MAX}	-	2	6	-	-	5	-	4	-	MHz
			4.5	30	-	-	25	-	20	-	MHz
			6	35	-	-	29	-	23	-	MHz
HCT TYPES											
Data to CP Setup Time (Figure 6)	t _{SU}	-	4.5	12	-	-	15	-	18	-	ns
Hold Time (Figure 6)	t _H	-	4.5	3	-	-	3	-	3	-	ns
Removal Time \overline{R} , \overline{S} , to CP (Figure 6)	^t REM	-	4.5	6	-	-	8	-	9	-	ns
Pulse Width R, S (Figure 2)	t _W	-	4.5	16	-	-	20	-	24	-	ns
Pulse Width CP (Figure 2)	t _W	-	4.5	18	-	-	23	-	27	-	ns
CP Frequency	f _{MAX}	-	4.5	25	-	-	20	-	16	-	MHz

Switching Specifications Input t_r , $t_f = 6ns$

		TEST	v _{cc}		25°C		-40°C T	O 85°C	-55°C TO 125°C		
PARAMETER	SYMBOL	CONDITIONS	(8)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
HC TYPES											
Propagation Delay,	t _{PLH} , t _{PHL}	C _L = 50pF	2	1	ı	175	-	220	-	265	ns
CP to Q, Q (Figure 3)		C _L = 50pF	4.5	ı	ı	35	1	44	-	53	ns
		C _L = 15pF	5	-	14	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	30	-	37	-	45	ns
Propagation Delay,	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	200	-	250	-	300	ns
$\overline{\mathbb{R}}$, $\overline{\mathbb{S}}$ to \mathbb{Q} , $\overline{\mathbb{Q}}$ (Figure 3)		C _L = 50pF	4.5	-	-	40	-	50	-	60	ns
		C _L = 15pF	5	-	17	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	34	-	43	-	51	ns
Transition Time (Figure 3)	t _{TLH} , t _{THL}	C _L = 50pF	2	-	-	75	-	95	-	110	ns
		C _L = 50pF	4.5	-	-	15	-	19	-	22	ns
		C _L = 50pF	6	-	-	13	-	16	-	19	ns
Input Capacitance	Cl	-	-	-	ı	10	-	10	-	10	pF

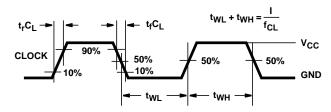
Switching Specifications Input t_r , $t_f = 6ns$ (Continued)

		TEST	v _{cc}		25°C		-40°C T	O 85°C	-55°C TO 125°C		
PARAMETER	SYMBOL	CONDITIONS	(V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
CP Frequency	f _{MAX}	CL = 15pF	5	-	50	-	-	-	-	-	MHz
Power Dissipation Capacitance (Notes 4, 5)	C _{PD}	-	5	-	25	-	-	-	-	-	pF
HCT TYPES	•	•			•						
Propagation Delay, CP to Q, \overline{Q} (Figure 4)	t _{PLH} , t _{PHL}	C _L = 50pF	4.5	-	-	35	-	44	-	53	ns
Propagation Delay, R, S to Q, Q (Figure 4)	t _{PHL} , t _{PLH}	CL = 50pF	4.5	-	-	40	-	50	-	60	ns
Transition Time (Figure 4)	t _{TLH} , t _{THL}	C _L = 50pF	4.5	-	-	15	-	19	-	22	ns
Input Capacitance	CI	-	-	-	-	10	-	10	-	10	pF
CP Frequency	f _{MAX}	CL = 15pF	5	-	50	-	-	-	-	-	MHz
Power Dissipation Capacitance (Notes 4, 5)	C _{PD}	-	5	-	30	-	-	-	-	-	pF

NOTES:

- 4. C_{PD} is used to determine the dynamic power consumption, per flip-flop.
- 5. $P_D = C_{PD} \, V_{CC}^2 \, f_i + \Sigma \, (C_L \, V_{CC}^2 \, f_o)$ where f_i = input frequency, f_o = output frequency, C_L = output load capacitance, V_{CC} = supply voltage.

Test Circuits and Waveforms



NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX} , input duty cycle = 50%.

FIGURE 1. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH

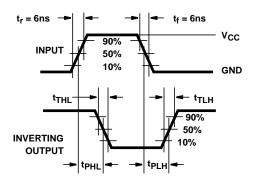
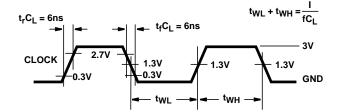


FIGURE 3. HC AND HCU TRANSITION TIMES AND PROPAGA-TION DELAY TIMES, COMBINATION LOGIC



NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX} , input duty cycle = 50%.

FIGURE 2. HCT CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH

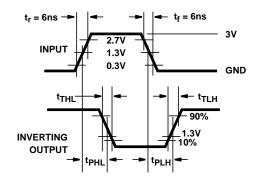


FIGURE 4. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

Test Circuits and Waveforms (Continued)

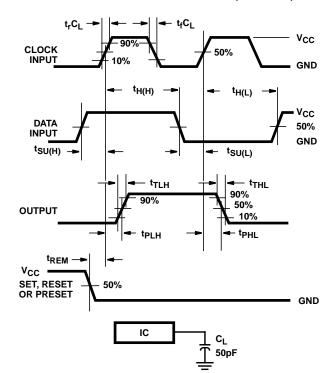


FIGURE 5. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

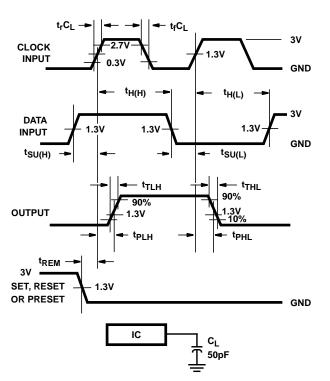


FIGURE 6. HCT SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS





28-Feb-2005

PACKAGING INFORMATION

Orderable D	Device S	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-86853	01CA	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
CD54HC7	74F	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
CD54HC74	4F3A .	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
CD54HCT	74F	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
CD54HCT7	4F3A	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
CD74HC7	74E	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD74HC7	74M	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD74HC74	1M96	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD74HC7	4MT	ACTIVE	SOIC	D	14	250	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD74HCT	74E .	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD74HCT	74M	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD74HCT7	4M96	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD74HCT7	74MT	ACTIVE	SOIC	D	14	250	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

None: Not yet available Lead (Pb-Free).

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

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14 LEADS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



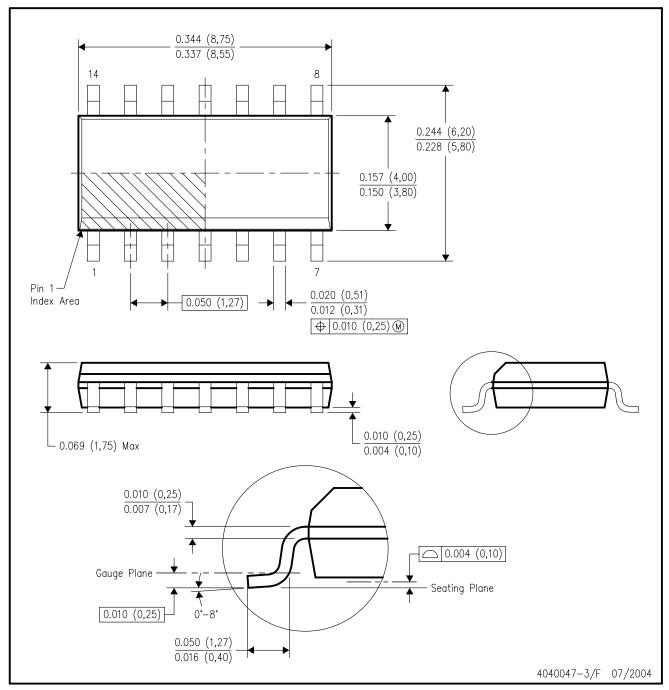
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-012 variation AB.



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