

MITSUBISHI LSI's **M5M5165P, FP-70, -10, -12, -15, -70L, -10L, -12L, -15L** **65536-BIT (8192-WORD BY 8-BIT) CMOS STATIC RAM**

DESCRIPTION

The M5M5165P, FP is a 65536-bit CMOS static RAM organized as 8192 words by 8 bits which is fabricated using high-performance double polysilicon CMOS technology. The use of resistive load NMOS cells and CMOS periphery result in a high-density and low-power static RAM. It is ideal for the memory systems which require simple interface.

The stand-by current is low enough for a battery back-up application.

FEATURES

Type	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
M5M5165P, FP-70	70ns	50mA	2mA
M5M5165P, FP-10	100ns		
M5M5165P, FP-12	120ns		
M5M5165P, FP-15	150ns		
M5M5165P, FP-70L	70ns	20 μ A	(V _{CC} =5.5V)
M5M5165P, FP-10L	100ns		
M5M5165P, FP-12L	120ns		
M5M5165P, FP-15L	150ns		

- Single +5V Power Supply
- Fully Static Operation: No Clocks, No Refresh
- Data-Hold on +2V Power Supply
- Directly TTL Compatible: All Inputs and Outputs
- Three-State Outputs: OR-tie Capability
- Simple Memory Expansion by $\overline{S}_1$, S_2
- $\overline{OE}$ Prevents Data Contention in The I/O Bus
- Common Data I/O

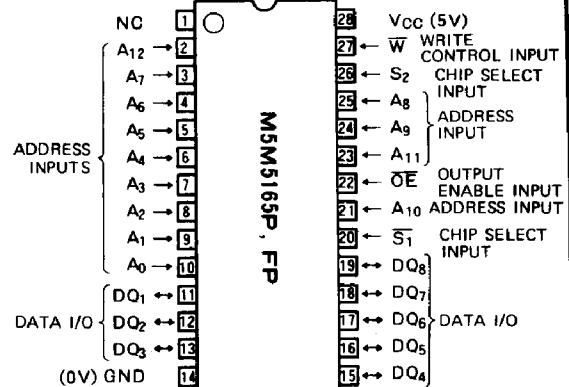
APPLICATION

Small Capacity Memory Units.

FUNCTION

The operation mode of the M5M5165P, FP is determined by a combination of the device control inputs $\overline{S}_1$, S_2 , $\overline{W}$

PIN CONFIGURATION (TOP VIEW)



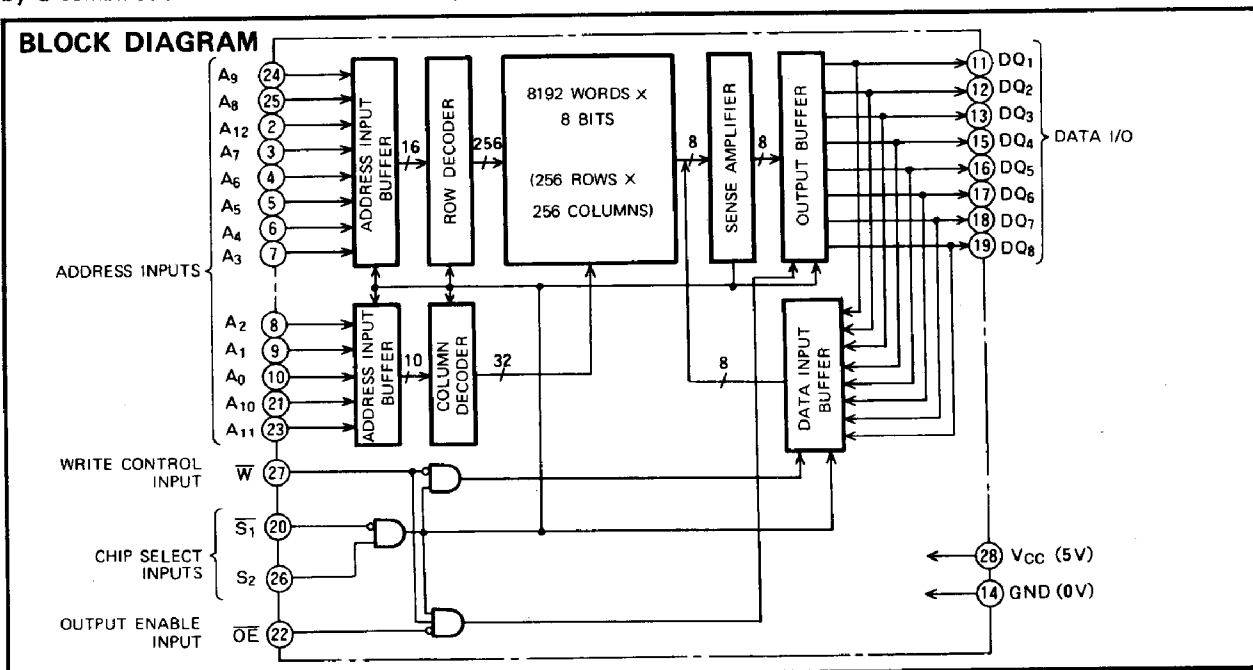
Outline 28P4 (DIP)
28P2W-C (SOP)

and $\overline{OE}$. Each mode is summarized in the function table. (see next page)

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S}_1$ and the high level S_2 . The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{S}_1$ or S_2 , whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The Output enable input $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S}_1$ and S_2 are in an active state ($\overline{S}_1=L$,

BLOCK DIAGRAM



M5M5165P, FP-70, -10, -12, -15, -70L, -10L, -12L, -15L

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$S_2 = H$)

When setting $\overline{S_1}$ at a high level or S_2 at a low level, the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{S_1}$ and S_2 . The power supply current is reduced as low as the stand-by current which is specified as I_{CC3} or I_{CC4} , and the memory data can be held at +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\overline{S_1}$	S_2	$\overline{W}$	$\overline{OE}$	Mode	DQ	I_{CC}
X	L	X	X	Non selection	high-impedance	Standby
H	X	X	X	Non selection	high-impedance	Standby
L	H	L	X	Write	D_{IN}	Active
L	H	H	L	Read	D_{OUT}	Active
L	H	H	H		high-impedance	Active

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	-0.3 ~ 7	V
V_I	Input voltage		-0.3 ~ $V_{CC} + 0.3$	V
V_O	Output voltage		0 ~ V_{CC}	V
P_d	Power dissipation	$T_a = 25^\circ\text{C}$	700	mW
T_{opr}	Operating temperature		0 ~ 70	$^\circ\text{C}$
T_{stg}	Storage temperature		-65 ~ 150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High input voltage		2.2		$V_{CC} + 0.3$	V
V_{IL}	Low input voltage		-0.3		0.8	V
V_{OH}	High output voltage	$I_{OH} = -1\text{mA}$	2.4			V
V_{OL}	Low output voltage	$I_{OL} = 2\text{mA}$			0.4	V
I_I	Input current	$V_I = 0 \sim V_{CC}$			± 1	μA
I_{OZH}	High level output current in off-state	$\overline{S_1} = V_{IH}$ or $S_2 = V_{IL}$ or $\overline{OE} = V_{IH}$ $V_{IO} = 0 \sim V_{CC}$			1	μA
I_{OZL}	Low level output current in off-state				-1	μA
I_{CC1}	Active supply current	$\overline{S_1} \leq 0.2$, $S_2 \geq V_{CC} - 0.2$ Output open Other inputs ≤ 0.2 or $\geq V_{CC} - 0.2$		30	45	mA
I_{CC2}	Active supply current	$\overline{S_1} = V_{IL}$ or $S_2 = V_{IH}$ Output open Other inputs = V_{IH}		35	50	mA
I_{CC3}	Stand-by supply current	① $S_2 \leq 0.2\text{V}$, Other inputs = $0 \sim V_{CC}$ ② $\overline{S_1} \geq V_{CC} - 0.2\text{V}$, $S_2 \geq V_{CC} - 0.2\text{V}$, Other inputs = $0 \sim V_{CC}$	P, FP		2	mA
			P, FP-L		20	μA
I_{CC4}	Stand-by supply current	$S_2 = V_{IL}$, $\overline{S_1} = V_{IH}$, Other inputs = $0 \sim V_{CC}$			3	mA
C_i	Input capacitance ($T_a = 25^\circ\text{C}$)	$V_I = \text{GND}$, $V_i = 25\text{mVrms}$, $f = 1\text{MHz}$			6	pF
C_o	Output capacitance ($T_a = 25^\circ\text{C}$)	$V_O = \text{GND}$, $V_O = 25\text{mVrms}$, $f = 1\text{MHz}$			8	pF

Note 1 Direction for current flowing into IC is indicated as positive (no mark)

2 Typical value is $V_{CC} = 5\text{V}$, $T_a = 25^\circ\text{C}$

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SWITCHING CHARACTERISTICS (T_a=0~70°C, V_{CC}=5V±10%, unless otherwise noted)

Read cycle

Symbol	Parameter	Limits												Unit
		M5M5165P,FP-70 M5M5165P,FP-70L			M5M5165P,FP-10 M5M5165P,FP-10L			M5M5165P,FP-12 M5M5165P,FP-12L			M5M5165P,FP-15 M5M5165P,FP-15L			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t _{CR}	Read cycle time	70			100			120			150			ns
t _a (A)	Address access time			70			100			120			150	ns
t _a (S ₁)	Chip select 1 access time			70			100			120			150	ns
t _a (S ₂)	Chip select 2 access time			70			100			120			150	ns
t _a (OE)	Output enable access time			35			50			60			70	ns
t _{dis} (S ₁)	Output disable time after $\overline{S_1}$ high			30			35			40			50	ns
t _{dis} (S ₂)	Output disable time after S ₂ low			30			35			40			50	ns
t _{dis} (OE)	Output disable time after OE high			30			35			40			50	ns
t _{en} (S ₁)	Output enable time after $\overline{S_1}$ low	5			10			10			10			ns
t _{en} (S ₂)	Output enable time after S ₂ high	5			10			10			10			ns
t _{en} (OE)	Output enable time after OE low	5			10			10			10			ns
t _v (A)	Data valid time after address change	20			20			20			20			ns

TIMING REQUIREMENTS (T_a=0~70°C, V_{CC}=5V±10%, unless otherwise noted)

Write cycle

Symbol	Parameter	Limits												Unit
		M5M5165P,FP-70 M5M5165P,FP-70L			M5M5165P,FP-10 M5M5165P,FP-10L			M5M5165P,FP-12 M5M5165P,FP-12L			M5M5165P,FP-15 M5M5165P,FP-15L			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t _{cw}	Write cycle time	70			100			120			150			ns
t _{w(w)}	Write pulse width	40			60			70			90			ns
t _{su(A)}	Address set up time	0			0			0			0			ns
t _{su(S)}	Chip select set up time	65			80			85			100			ns
t _{su(D)}	Data set up time	30			35			40			50			ns
t _{h(D)}	Data hold time	5			5			5			5			ns
t _{rec(w)}	Write recovery time	5			5			10			10			ns
t _{dis(w)}	Output disable time after $\overline{W}$ low	0		30			35			40			50	ns
t _{dis(OE)}	Output disable time after $\overline{OE}$ high	0		30			35			40			50	ns
t _{en(w)}	Output enable time after $\overline{W}$ high	5			10			10			10			ns
t _{en(OE)}	Output enable time after $\overline{OE}$ low	5			10			10			10			ns

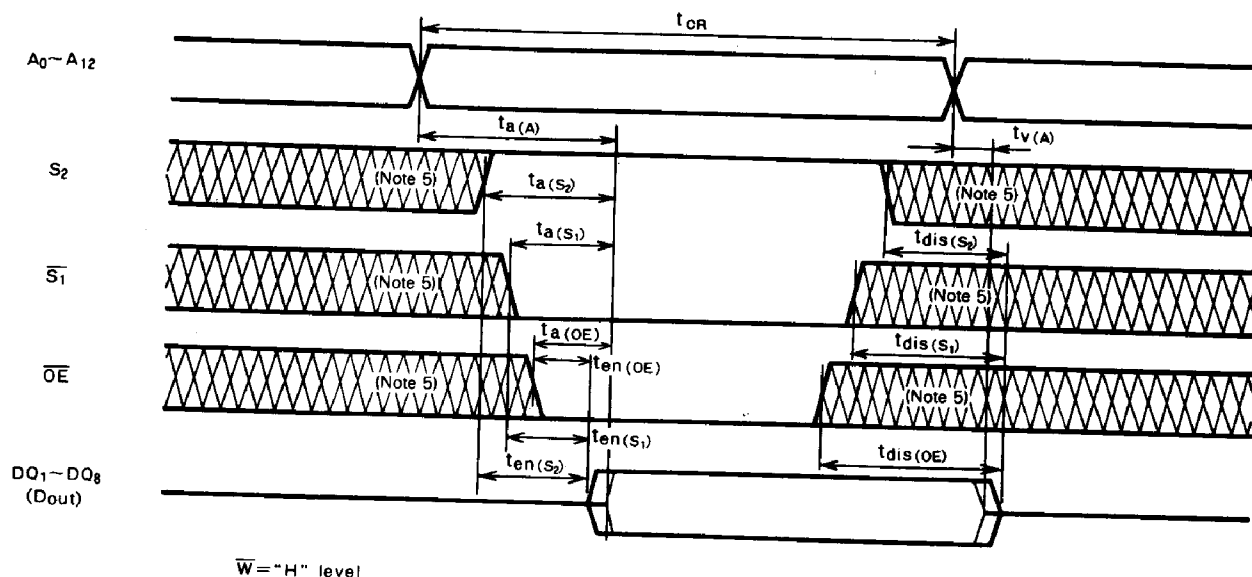
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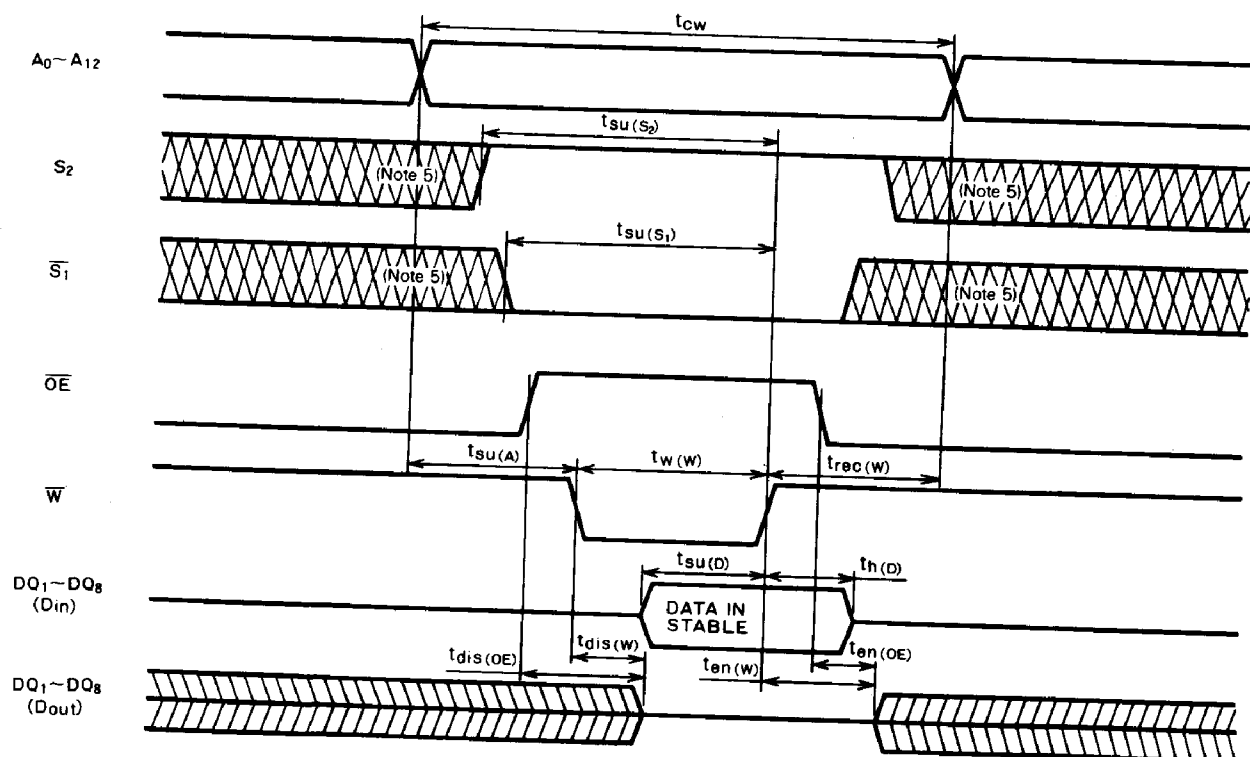
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TIMING DIAGRAM

Read cycle



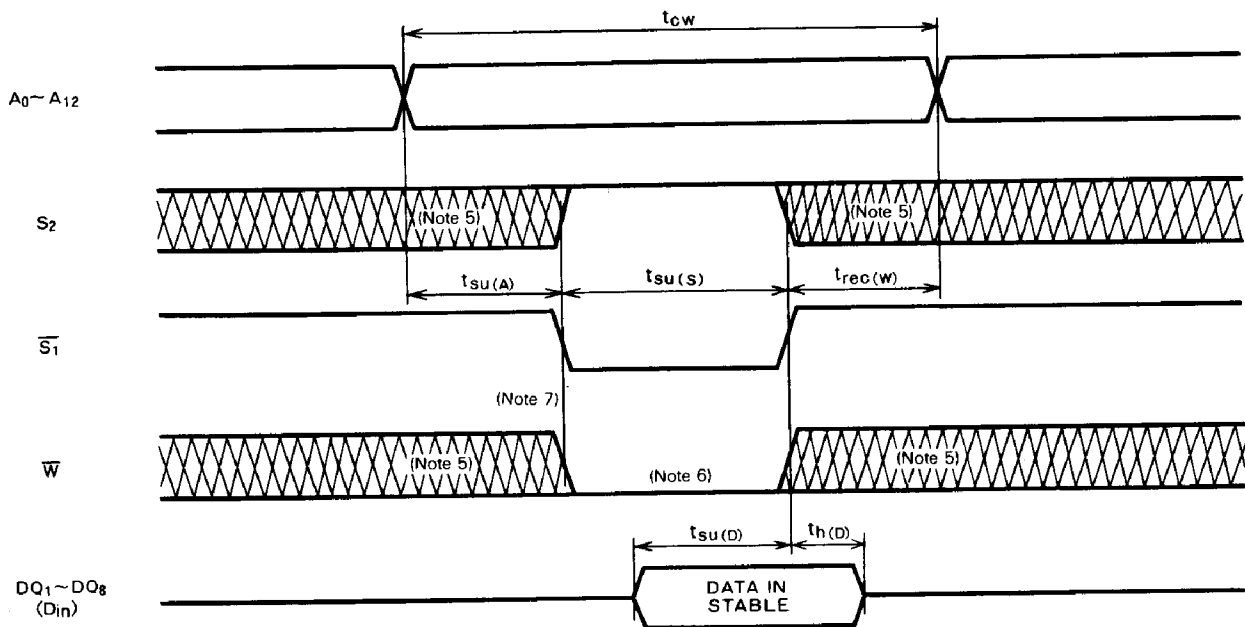
Write cycle ($\overline{W}$ control)



M5M5165P, FP-70, -10, -12, -15, -70L, -10L, -12L, -15L

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Write cycle (S control)



Note 4: Test condition

Input pulse level $V_{IH} = 2.4V$, $V_{IL} = 0.6V$

Input rise and fall time 10ns

Reference level $V_{OH} = V_{OL} = 1.5V$

Transition is measured $\pm 500mV$ from steady state voltage. (for t_{en} , t_{dis})

Output loads Fig. 1, $C_L = 100pF$ (P, FP-10, -12, -15, -10L, -12L, -15L)

$C_L = 30pF$ (P, FP-70, -70L)

$C_L = 5pF$ (for t_{en} , t_{dis})

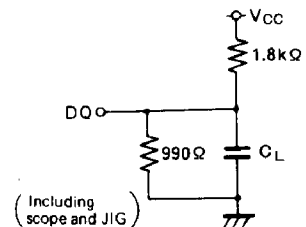


Fig. 1 Output load

Note 5: Hatching indicates the state is don't care.

6: Writing is executed while S_2 high overlaps S_1 and $\overline{W}$ low.

7: If $\overline{W}$ goes low simultaneously with or prior to S_1 low or S_2 high, the output remains in the high-impedance state.

8: Don't apply inverted phase signal externally when DQ pin is in output mode.

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POWER DOWN CHARACTERISTICS

ELECTRICAL CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$V_{CC(PD)}$	Power down supply voltage		2			V
$V_I(\overline{S}_1)$	Chip select input $\overline{S}_1$	$2.2\text{V} \leq V_{CC(PD)}$	2.2			V
		$2\text{V} \leq V_{CC(PD)} \leq 2.2\text{V}$		$V_{CC(PD)}$		
$V_I(S_2)$	Chip select input S_2	$4.5\text{V} \leq V_{CC(PD)}$			0.8	V
		$V_{CC(PD)} < 4.5\text{V}$			0.2	
$I_{CC(PD)}$	Power down supply current	$V_{CC} = 3\text{V}$, Other inputs = 3V			2	mA
					10 *	μA

Note 3: When $\overline{S}_1$ is operated at 2.2V ($V_{IH \min}$) and the supply voltage is between 4.5V and 2.4V, supply current is defined as I_{CC4} .

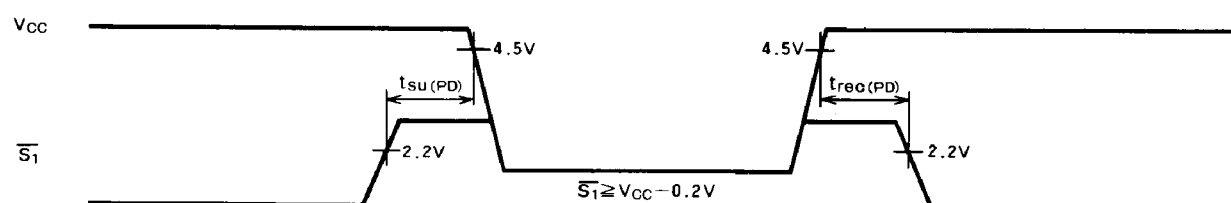
* : $I_{CC(PD)} = 1\mu\text{A}$ at $T_a = 25^\circ\text{C}$

TIMING REQUIREMENTS ($T_a = 0 \sim 70^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(PD)}$	Power down setup time		0			ns
$t_{rec(PD)}$	Power down recovery time		t_{CR}			ns

POWER DOWN CHARACTERISTICS

$\overline{S}_1$ control



S_2 control

