NEC

NPN SILICON TRANSISTOR
2SC3209

DESCRIPTION The 2SC3209 is designed for use in TV chroma output circuits and TV horizontal deflection output circuits.

FEATURES

- High voltage $V_{CEO} \geqq 300$ V
- High Electrostatic-Discharge-Resistant (E-B reverse bias, C=2 300 pF) V_{ESDR}: TYP. 1 000 V

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature . . . . −55 to +150 °C

Junction Temperature . . . . .150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

Total Power Dissipation . . . . .1.0 W

Maximum Voltages and Currents (T_a = 25 °C)

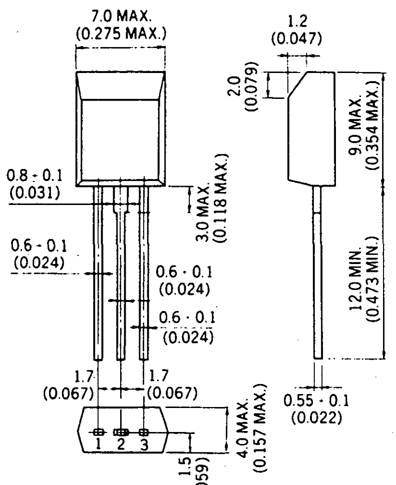
V_{CBO} Collector to Base Voltage . . . . 300 V

V_{CEO} Collector to Emitter Voltage . . . . . . 300 V

V_{EBO} Emitter to Base Voltage . . . . .5.0 V

I_C Collector Current . . . . 200 mA

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE} *	DC Current Gain	60	150	250		V_{CE} = 10 V, I_C = 10 mA
t_d	Delay Time			1.0	μs	V_{CC} = 30 V, I_C = 100 mA, I_{B1} = − I_{B2} = 10 mA
t_r	Rise Time			1.0	μs	
t_{stg}	Storage Time			2.0	μs	
t_f	Fall Time			1.0	μs	
f_T	Gain Bandwidth Product		50		MHz	V_{CE} = 30 V, I_E = −10 mA
V_{ESDR}	Electrostatic-Discharge-Resistant		1000		V	See Test Circuit
C_{ob}	Output Capacitance		2.8	3.5	pF	V_{CB} = 30 V, I_E = 0, f = 1.0 MHz
I_{CBO}	Collector Cutoff Current			100	nA	V_{CB} = 200 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			100	nA	V_{EB} = 5.0 V, I_C = 0
V_{BE} *	Base to Emitter Voltage	600	670	700	mV	V_{CE} = 10 V, I_C = 10 mA
$V_{CE(sat)}$ *	Collector Saturation Voltage		0.15	1.5	V	I_C = 50 mA, I_B = 5.0 mA
$V_{BE(sat)}$ *	Base Saturation Voltage		0.80	1.5	V	I_C = 50 mA, I_B = 5.0 mA

* Pulsed PW≦300 μs, duty cycle≦2 %

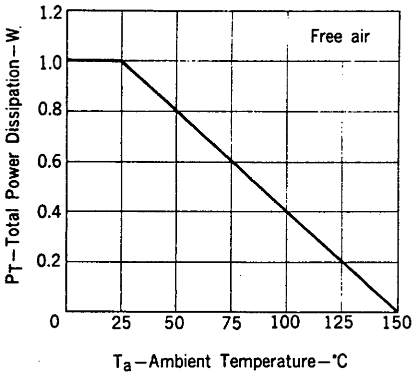
Classification of h_{FE1}

Rank	M	L	K
Range	60 – 120	100 – 200	160 – 250

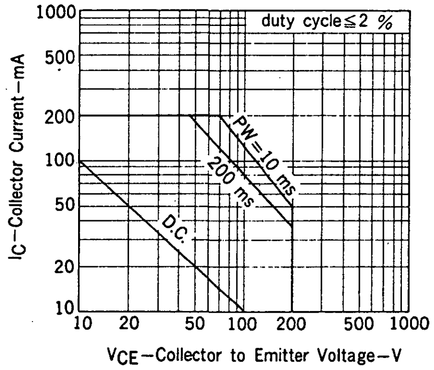
Test Conditions: V_{CE} = 10 V, I_C = 10 mA

TYPICAL CHARACTERISTICS ($T_a = 25\ ^\circ C$)

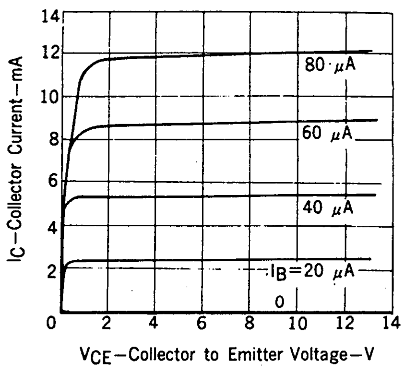
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



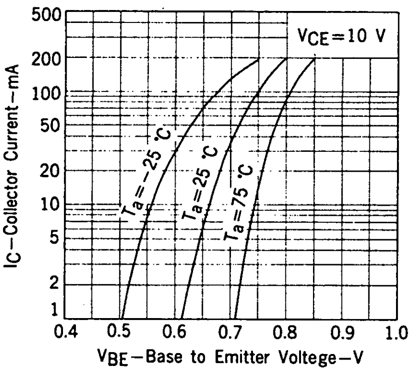
SAFE OPERATING AREAS (TRANSIENT THERMAL RESISTANCE METHOD)



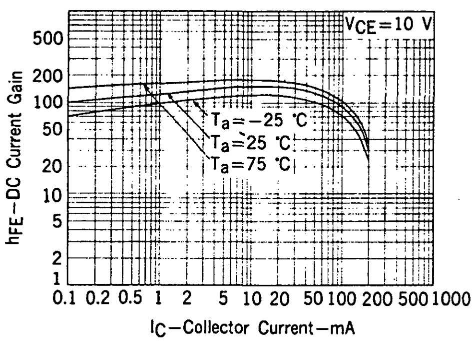
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



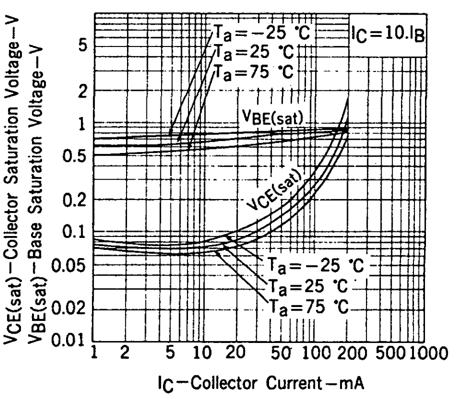
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



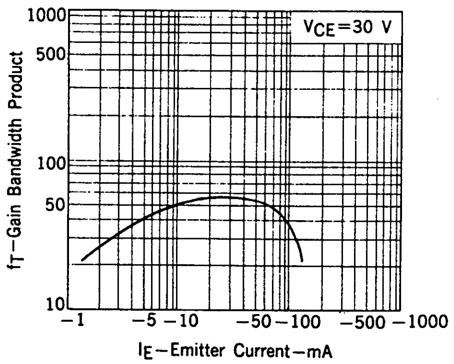
DC CURRENT GAIN vs. COLLECTOR CURRENT



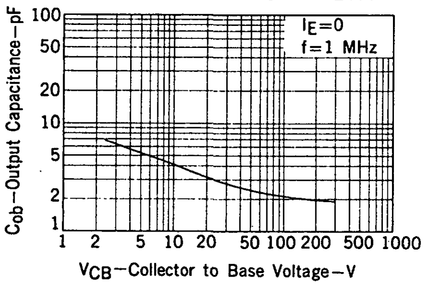
COLLECTOR SATURATION VOLTAGE, BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



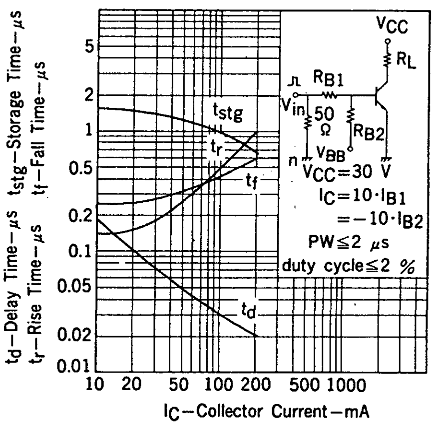
GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



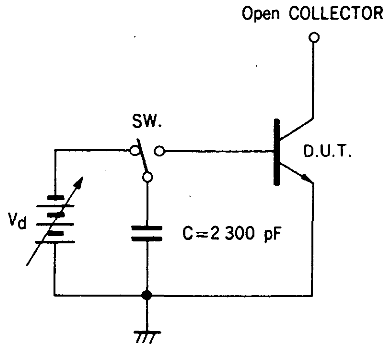
OUTPUT CAPACITANCE vs COLLECTOR TO BASE VOLTAGE



SWITCHING TIME vs. COLLECTOR CURRENT



ELECTROSTATIC-DISCHARGE-RESISTANT TEST CIRCUIT



TEST CONDITION

1) E-B reverse bias
2) C = 2 300 pF
3) Apply one shot pluse to D.U.T. (Transistor Under the Test) by SW.

JUDGEMENT

REJECT; BV_{EBO} waveform defect
As a result if D.U.T. is not rejected, apply higher voltage to capacitor and test again.