SDRAM DDR MODULE

256 MByte (32M x 72) DDR SDRAM
Registered 184 Pin DIMM Preliminary

General Description:

This memory module is a high performance 256 Megabyte Registered synchronous dynamic RAM module organized as 32M x 72 in a 184 pin Dual In-Line Memory Module (DIMM) package. The module utilizes eighteen (18) 16Mx8 DDR SDRAM devices in a TSOP II 400 mil package. A 256 Byte Serial EEPROM contains the module configuration information. The EEPROM can be configured to Jedec specifications.

These modules offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high rate with automatic column-address generation, interleave between internal banks in order to hide precharge time, and the capability to randomly change column address on each clock cycle during burst.

Features:

- High density: 256 MB (32M x 72) in two Banks
- Cycle time: 7.5ns (133 MHz)
  10ns (100 MHz)
- Data Rate: 266Mbit/sec/pin (133 MHz)
  200Mbit/sec/pin (100 MHz)
- CAS Latency: 2 (100MHz)
  2, 2.5 (133MHz)
- JEDEC Standard 184 Pin Registered SDRAM DDR DIMM
- PC1600/2100 Compliant
- Single power supply of 2.5V ± 10%
- Serial Presence Detect
- SSTL2 Compatible I/O and Clock
- SSTL2 Registered Control & Address Lines
- On-board Differential PLL Clock Driver
- Refresh Rate 15.6uSec
- Auto Precharge and Auto Refresh Modes handled by SDRAM Devices
- Programmable Burst Type, Burst Length and CAS Latency of SDRAM devices
- Internal Pipeline Operation
- Fully Synchronous – all signals registered on positive edge of system clock
- Data provided during Reads and Writes at twice the clock frequency
- Package Height: 1.20 inches

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Operating Features:

The SDRAM DDR DIMM utilizes a clock input for the synchronization. Each operation of the SDRAM is determined by commands and all operations are referenced to a positive clock edge. CAS Latency defines the delay from when a Read Command is registered on a rising clock edge to when the data from the Read Command becomes available at the outputs. The CAS latency is expressed in terms of clock cycles. This specific DIMM supports 2.5 and 2 clock cycles.

The burst mode is a very high-speed access mode utilizing an internal column address generator. Once a column address for the first access is set, following addresses are automatically generated by the internal column address counter.

All control and address signals are registered on-board and hence delayed by one cycle in arriving at the SDRAMs. The clock signal is distributed to all SDRAMs via a zero delay PLL driver. Note that the PLL must be given enough clock cycles to stabilize before any operation can be given (minimum stabilization time equal to 1 ms).

Absolute Maximum Ratings*:

Item	Symbol	Rating	Unit
V_{DD} Supply voltage Relative to V_{SS}	V_{DD}	-1V to +3.6V	V
V_{DDQ} Supply voltage Relative to V_{SS}	V_{DDQ}	-1V to +3.6V	V
V_{REF} and Inputs Relative to V_{SS}	$V_{REF,}$ V_{IN}	-1V to +3.6V	V
I/O Voltage Relative to V_{SS}	$V_{I/O}$	-0.5V to V_{DD} +0.5V	V
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	-55 to +150	°C
Short circuit output current	I_{out}	50	mA

* Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions:

(Voltage referenced to V_{SS} =0V ,T_A = 0 to 70 °C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	2.3	2.5	2.7	V
I/O Supply voltage	V_{DDQ}	2.3	2.5	2.7	V
I/O Reference Voltage	V_{REF}	0.49x V_{DD}	1.25	0.51x V_{DD}	V
I/O Termination Voltage	V_{TT}	V_{REF} -0.04	V_{REF}	V_{REF} +0.04	V
Input high Voltage	V_{IH}	V_{REF} +0.18	-	V_{DD} +0.3	V
Input low Voltage	V_{IL}	-0.3	-	V_{REF} -0.18	V
Clock Input Voltage	V_{IN}	-0.3	-	V_{DDQ} +0.3	V
Clock Differential Voltage	V_{ID}	0.36	-	V_{DDQ} +0.6	V
Clock Crossing Point Voltage	V_{IX}	1.15	-	1.35	V
Input and Output Leakage	I_I , I_{OZ}	-5	-	5	uA
Output High and Low Currents	I_{OH} , I_{OL}	-16.8 , +16.8	-	-	mA

Capacitance:

(TA=25°C, Vcc=2.5V±0.2V)

Parameter	Symbol	Max.	Unit
Input capacitance (CK, CK\)	C_{I1}	3	PF
Input/Output capacitance (DQs, DQSs, DMs,CBs)	C_{IO}	13	PF
Input capacitance (All other input-only pins)	C_{I2}	4	PF

DIMM Pinout:

No.	Designation	No.	Designation	No.	Designation	No.	Designation	No.	Designation
1	VREF	43	A1	85	VDD	127	DQ29	169	DM6/DQS15
2	DQ0	44	CB0	86	DQS7	128	VDDQ	170	DQ54
3	VSS	45	CB1	87	DQ58	129	DM3/DQS12	171	DQ55
4	DQ1	46	VDD	88	DQ59	130	A3	172	VDDQ
5	DQS0	47	DQS8	89	VSS	131	DQ30	173	NC
6	DQ2	48	A0	90	NC	132	VSS	174	DQ60
7	VDD	49	CB2	91	SDA	133	DQ31	175	DQ61
8	DQ3	50	VSS	92	SCL	134	CB4	176	VSS
9	NC	51	CB3	93	VSS	135	CB5	177	DM7/DQS16
10	RESET/	52	BA1	94	DQ4	136	VDDQ	178	DQ62
11	VSS	53	DQ32	95	DQ5	137	CK0	179	DQ63
12	DQ8	54	VDDQ	96	VDDQ	138	CK0	180	VDDQ
13	DQ9	55	DQ33	97	DM0/DQS9	139	VSS	181	SA0
14	DQS1	56	DQS4	98	DQ6	140	DM8/DQS17	182	SA1
15	VDDQ	57	DQ34	99	DQ7	141	A10	183	SA2
16	DU (CK1)	58	VSS	100	VSS	142	CB6	184	VDDSPD
17	DU (CK1)/	59	BA0	101	NC	143	VDDQ		
18	VSS	60	DQ35	102	NC	144	CB7		
19	DQ10	61	DQ40	103	A13	145	VSS		
20	DQ11	62	VDDQ	104	VDDQ	146	DQ36		
21	CCKE0	63	WE/	105	DQ12	147	DQ37		
22	VDDQ	64	DQ41	106	DQ13	148	VDD		
23	DQ16	65	CAS/	107	DM1/DQS10	149	DM4/DQS13		
24	DQ17	66	VSS	108	VDD	150	DQ38		
25	DQS2	67	DQS5	109	DQ14	151	DQ39		
26	VSS	68	DQ42	110	DQ15	152	VSS		
27	A9	69	DQ43	111	CKE1	153	DQ44		
28	DQ18	70	VDD	112	VDDQ	154	RAS/		
29	A7	71	NC, S2/	113	BA2	155	DQ45		
30	VDDQ	72	DQ48	114	DQ20	156	VDDQ		
31	DQ19	73	DQ49	115	A12	157	S0/		
32	A5	74	VSS	116	VSS	158	S1/		
33	DQ24	75	DU (CK2)/	117	DQ21	159	DM5/DQS14		
34	VSS	76	DU (CK2)	118	A11	160	VSS		
35	DQ25	77	VDDQ	119	DM2/DQS11	161	DQ46		
36	DQS3	78	DQS6	120	VDD	162	DQ47		
37	A4	79	DQ50	121	DQ22	163	NC,S3/		
38	VDD	80	DQ51	122	A8	164	VDDQ		
39	DQ26	81	VSS	123	DQ23	165	DQ52		
40	DQ27	82	VDDID	124	VSS	166	DQ53		
41	A2	83	DQ56	125	A6	167	NC/FETEN		
42	VSS	84	DQ57	126	DQ28	168	VDD		

DC Characteristics:

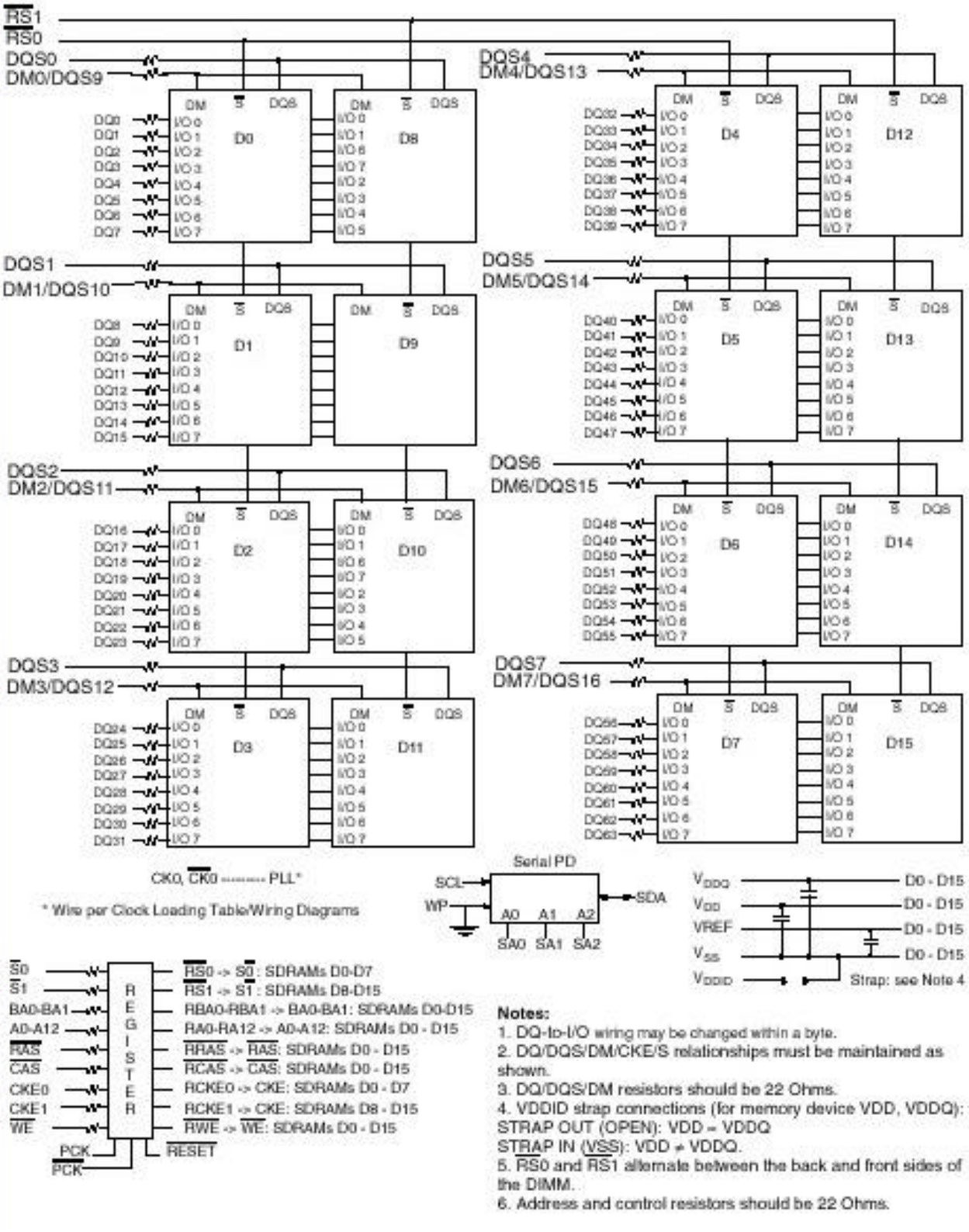
(V_{DD}, V_{DDQ} = 2.5V±0.2V, V_{SS}=0V, T_A=0 to + 70°C)

Parameter[1]	Symbol	133MHz Max.	100MHz Max.	Unit
Operating current (No Burst, T_{CK}=min. T_{RC}=min.)	I_{CC1}	TBD	TBD	mA
Precharge Standby Current (CKE=V_{IL}, T_{CK} = min. Bank idle) (CKE=V_{IH}, T_{CK} = min. Bank idle)	I_{CC2}	90 900	90 900	mA
Active Standby Current (CKE=V_{IL}, T_{CK} = min.) (CKE=V_{IH}, T_{CK} = min.)	I_{CC3}	126 900	126 720	mA
Burst Mode Current (t_{CK}=min.)	I_{CC4}	TBD	TBD	mA
Refresh Current (per DIMM) (t_{CK}=min., t_{RFC}=min., t_{RRD}=min., Auto Refresh)	I_{CC5}	TBD	TBD	mA
Self Refresh Current (CKE=V_{IL})	I_{CC7}	36	54	mA

AC Electrical Characteristics:

(TA=0°C to +70°C, V_{CC}=2.5V±0.2V, V_{SS}=0V)

Parameter	Symbol	133MHz Min.	133MHz Max.	100MHz Min.	100MHz Max.	Unit
Row to row active delay	t_{RRD}	15	-	20	-	ns
RAS to CAS delay (CL=2.5) (CL=2)	t_{RCD}	20 15	- -	- 20	- -	ns
Row precharge time (CL=2.5) (CL=2)	t_{RP}	20 15	- -	- 20	- -	ns
Row active time	t_{RAS}	45	120K	50	120K	ns
Row cycle time (CL=2.5) (CL=2)	t_{RC}	 65 60	 - -	 - 70	 - -	ns
Access Window of DQS from CLK, CLK\	t_{DQSCK}	-0.75	+0.75	-0.8	+0.8	ns
DQS Input High Pulse Width	t_{DQSH}	0.35	-	0.35	-	clk
DQS Input Low Pulse Width	t_{DQSL}	0.35	-	0.35	-	clk
Refresh to Refresh command period	t_{REFC}	-	140.6	-	140	clk
Access Window of DQs from CLK	t_{AC}	-0.75	+0.75	-0.8	+0.8	ns
Clock Cycle Time	t_{CK}	7.5		10		ns
Auto Refresh command period (CL=2.5) (CL=2)	t_{RFC}	 75 67	 - -	 - 80	 - -	ns
Clock High Pulse Width	t_{CH}	0.45	0.55	0.45	0.55	clk
Clock Low Pulse Width	t_{CL}	0.45	0.55	0.45	0.55	clk
Address Input Setup Time	t_{IS}	1	-	1.1	-	ns
Address Input Hold Time	t_{IH}	1	-	1.1	-	ns
Input Data Hold Time	t_{DH}	0.5	-	0.6	-	ns
Input Data Setup Time	t_{DS}	0.5	-	0.6	-	ns



Notes:

1. DQ-to-I/O wiring may be changed within a byte.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ/DQS/DM resistors should be 22 Ohms.
4. VDDID strap connections (for memory device VDD, VDDQ): STRAP OUT (OPEN): VDD = VDDQ
   STRAP IN (VSS): VDD ≠ VDDQ.
5. RS0 and RS1 alternate between the back and front sides of the DIMM.
6. Address and control resistors should be 22 Ohms.

Part Number:

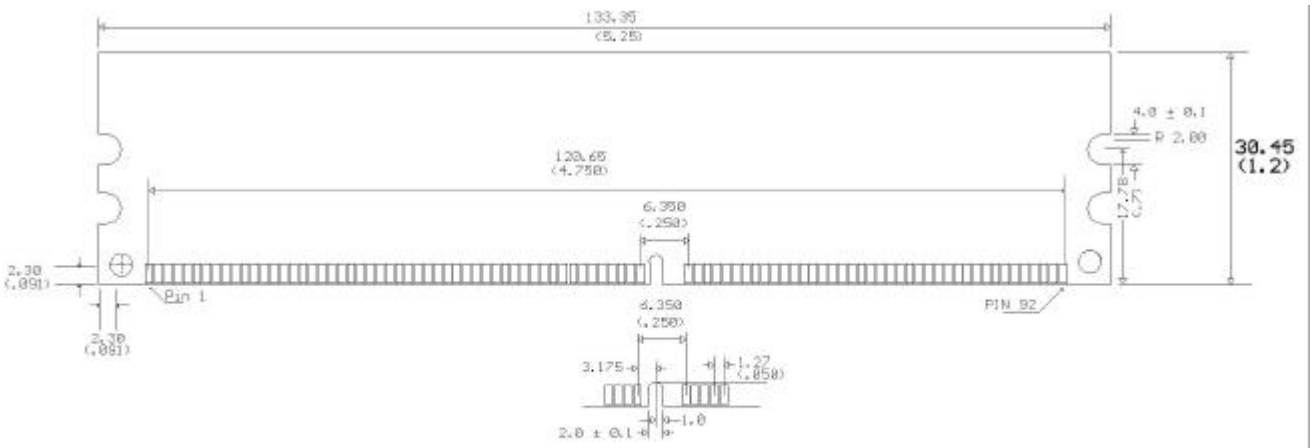
KT3272DSN*s*R-*xx*V2LC*nn*

Part Number Decoder:

s = Clock		xx = DRAM		nn = CAS Latency	
3 =	133MHz	14 =	Samsung	20 =	2
0 =	100MHz	04 =	Elpida	25 =	2.5
		06 =	Hynix		
		07 =	Micron		
		09 =	Mosel		
		15 =	Infineon		
		17 =	Nanya		
		00 =	Non-specific		

Please contact Kentron Technologies for more information.

Package Description:



Note: All dimensions in millimeters (inches)

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