FAIRCHILD SEMICONDUCTOR®

February 2006

FDS9412A
N-Channel PowerTrench® MOSFET
30V, 8A, 21mΩ

General Description

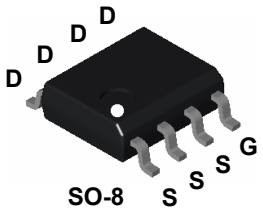
This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge ,low $r_{DS(on)}$ and fast switching speed.

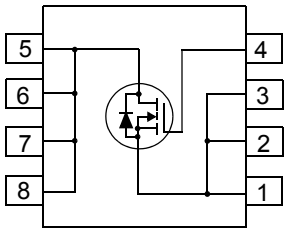
Features

- Max $r_{DS(on)}$ = 21mΩ at V_{GS} = 10V, I_D = 8A
- Max $r_{DS(on)}$ = 25mΩ at V_{GS} = 4.5V, I_D = 6.6A
- Low gate charge
- RoHS Compliant

Application

- DC/DC converters





MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current -Continuous (T_A = 25°C, V_{GS} = 10V, $R_{\theta JA}$ = 50°C/W)	8	A
	-Continuous (T_A = 25°C, V_{GS} = 4.5V, $R_{\theta JA}$ = 50°C/W)	6.6	
	-Pulsed	30	A
E_{AS}	Single Pulse Avalanche Energy (Note 3)	54	mJ
P_D	Power dissipation	2.5	W
T_J, T_{STG}	Operating and Storage Temperature	-55 to 150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance , Junction to Case (Note 1)	25	°C/W
$R_{\theta JA}$	Thermal Resistance , Junction to Ambient (Note 1a)	50	°C/W

Package Marking and Ordering Information

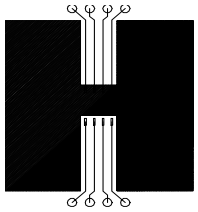
Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDS9412A	FDS9412A	SO-8	330mm	12mm	2500 units

Electrical Characteristics T_J = 25°C unless otherwise noted

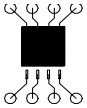
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250μA, referenced to 25°C		22		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24V, V_{GS} = 0V			1	μA
		T_J = 150°C			250	
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20V			±100	μA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA	1.2	1.9	2.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250μA, referenced to 25°C		-5.8		mV/°C
$r_{DS(on)}$	Drain to Source On Resistance	V_{GS} =10V , I_D = 8A		14	21	mΩ
		V_{GS} = 4.5V, I_D = 6.6A		18	25	
		V_{GS} = 10V, I_D = 8A, T_J = 150°C		20	30	
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} =15V, V_{GS} = 0V, f = 1MHz		740	985	pF
C_{oss}	Output Capacitance			150	200	pF
C_{rss}	Reverse Transfer Capacitance			95	145	pF
R_G	Gate Resistance	f = 1MHz		3		Ω
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 15V, I_D = 1A, V_{GS} = 10V, R_{GS} = 6Ω		5	10	ns
t_r	Rise Time			13	23	ns
$t_{d(off)}$	Turn-Off Delay Time			13	24	ns
t_f	Fall Time			12	22	ns
Q_g	Total Gate Charge at 10V	V_{GS} = 0V to 10V, V_{DD} = 15V, I_D = 8A, I_G = 1.0mA		14	20	nC
Q_g	Total Gate Charge at 5V	V_{GS} = 0V to 5V		8	12	nC
Q_{gs}	Gate to Source Gate Charge			2.3		nC
Q_{gd}	Gate to Drain “Miller” Charge			3.0		nC
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Voltage	V_{GS} = 0V, I_S = 8A		0.85	1.25	V
		V_{GS} = 0V, I_S = 2.1A		0.76	1.0	V
t_{rr}	Reverse Recovery Time	I_F = 8A, di/dt = 100A/μs		18	27	ns
Q_{rr}	Reverse Recovery Charge	I_F = 8A, di/dt = 100A/μs		9.6	14	nC

Notes:

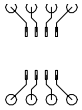
1: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 50°C/W when mounted on a 1 in^2 pad of 2 oz copper



b)105°C/W when mounted on a .04 in^2 pad of 2 oz copper



c) 125°C/W when mounted on a minimun pad

Scale 1 : 1 on letter size paper

2: Pulse Test:Pulse Width <300μs, Duty Cycle <2.0%.

3: Starting T_J = 25°C, L = 3mH, I_{AS} = 6A, V_{DD} = 30V, V_{GS} = 10V.

Typical Characteristics T_J = 25°C unless otherwise noted

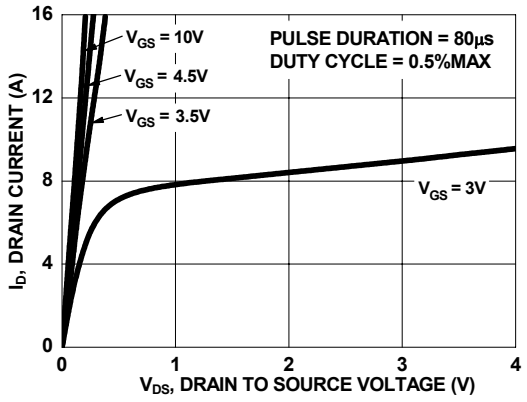


Figure 1. On Region Characteristics

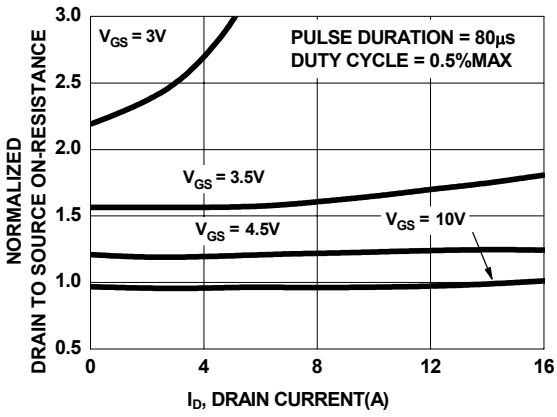


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

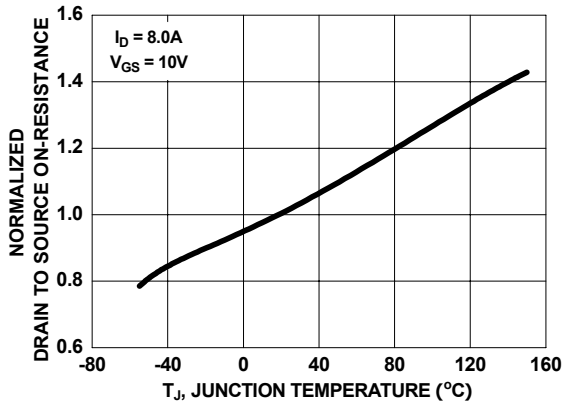


Figure 3. Normalized On Resistance vs Junction Temperature

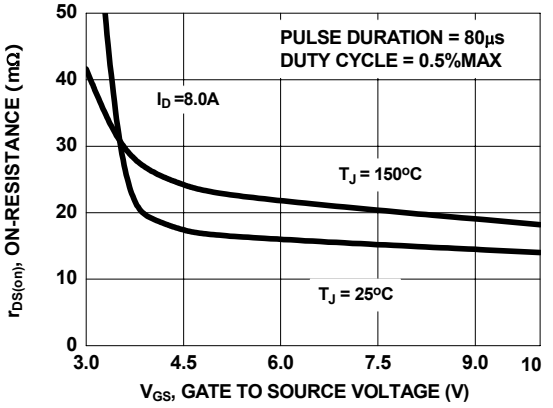


Figure 4. On-Resistance vs Gate to Source Voltage

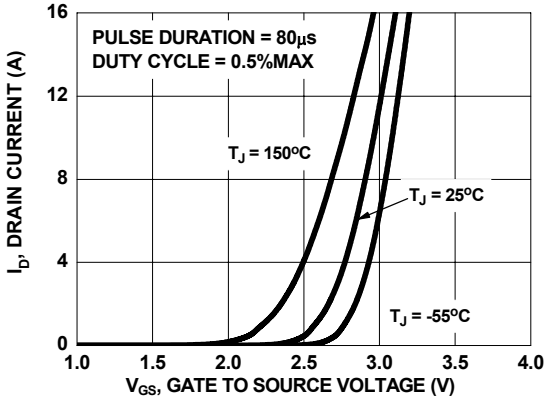


Figure 5. Transfer Characteristics

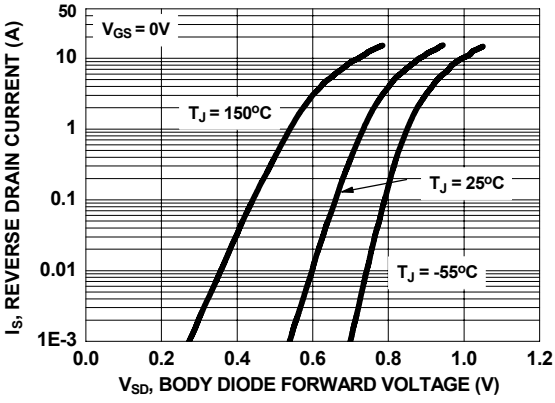


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25°C unless otherwise noted

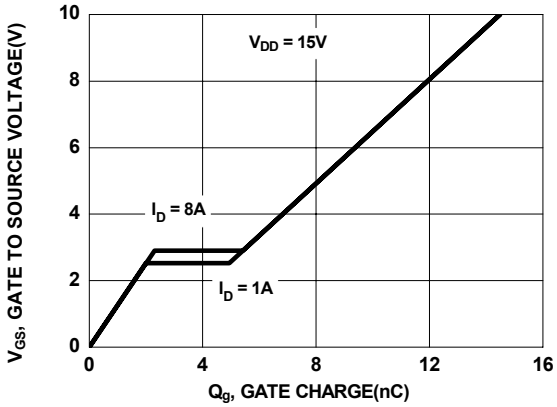


Figure 7. Gate Charge Characteristics

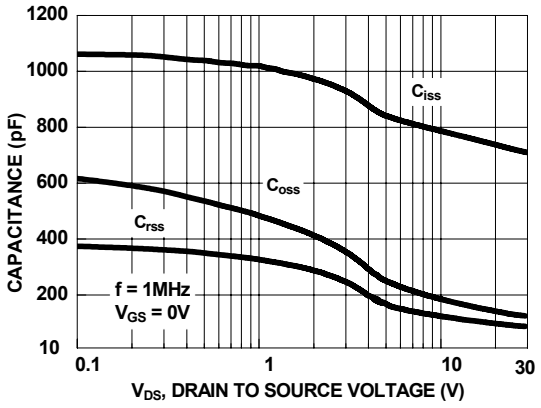


Figure 8. Capacitance vs Drain to Source Voltage

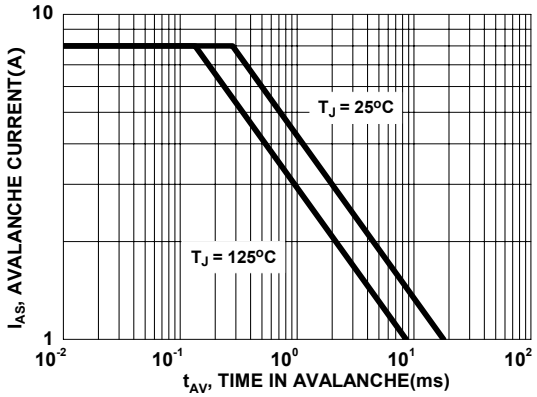


Figure 9. Unclamped Inductive Switching Capability

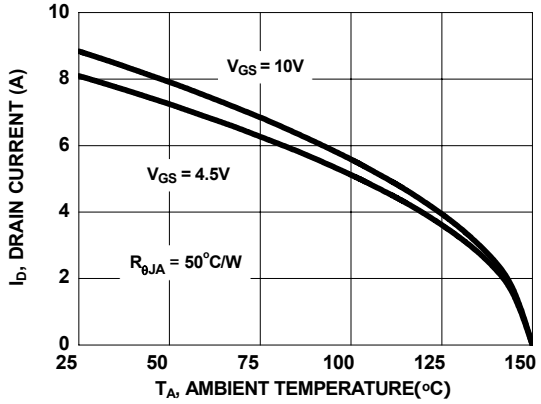


Figure 10. Maximum Continuous Drain Current vs Ambient Temperature

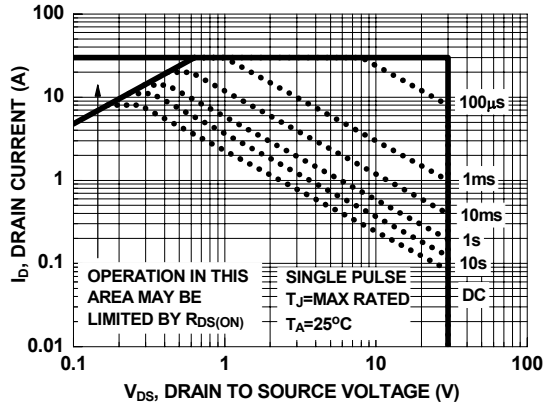


Figure 11. Forward Bias Safe Operating Area

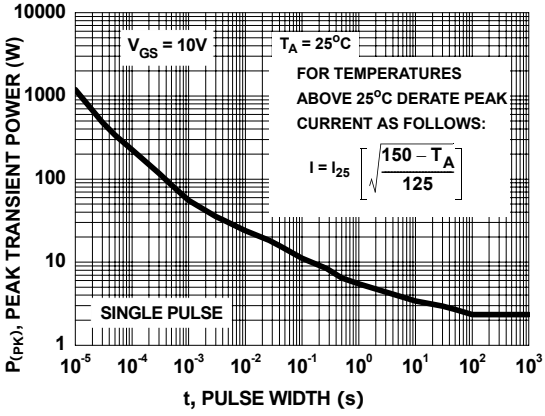


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25°C unless otherwise noted

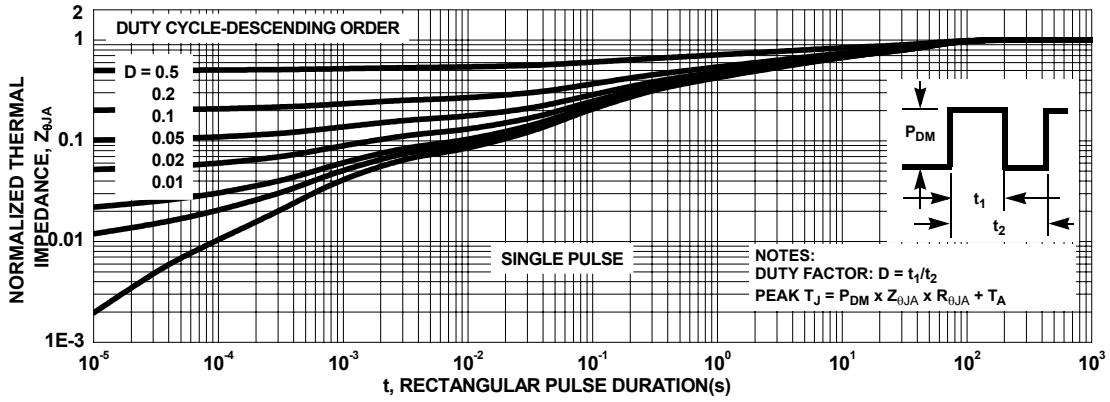


Figure 13. Transient Thermal Response Curve

TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx™
ActiveArray™
Bottomless™
Build it Now™
CoolFET™
CROSSVOLT™
DOME™
EcoSPARK™
E^2CMOS™
EnSigna™
FACT™
FACT Quiet Series™
FAST®
FASTr™
FPS™
FRFET™
GlobalOptoisolator™
GTO™
HiSeC™
I^2C™
i-Lo™
ImpliedDisconnect™
IntelliMAX™
ISOPLANAR™
LittleFET™
MICROCOUPLER™
MicroFET™
MicroPak™
MICROWIRE™
MSX™
MSXPro™
OCX™
OCXPro™
OPTOLOGIC®
OPTOPLANAR™
PACMAN™
POP™
Power247™
PowerEdge™
PowerSaver™
PowerTrench®
QFET®
QS™
QT Optoelectronics™
Quiet Series™
RapidConfigure™
RapidConnect™
µSerDes™
ScalarPump™
SILENT SWITCHER®
SMART START™
SPM™
Stealth™
SuperFET™
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SyncFET™
TCM™
TinyLogic®
TINYOPTO™
TruTranslation™
UHC™
UltraFET®
UniFET™
VCX™
Wire™

Across the board. Around the world.™
The Power Franchise®
Programmable Active Droop™

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.
As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.