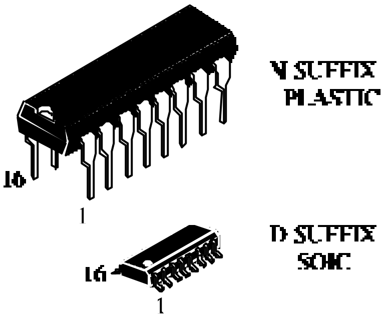
Dual 4-Bit Shift Register

High-Performance Silicon-Gate CMOS

The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LS/ALSTTL outputs.

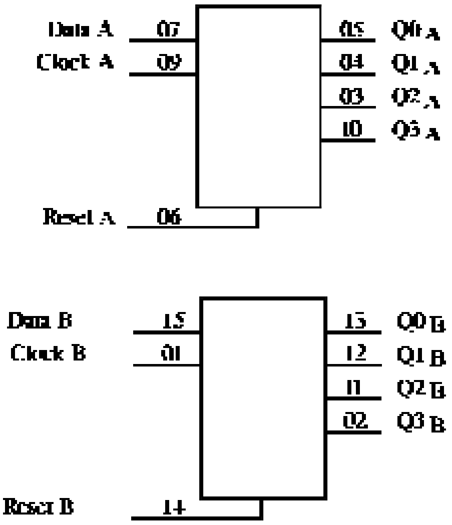
This device consists of two identical independent 4-stage serial-input/parallel-output registers. Each register has independent Clock and Reset inputs as well as a single serial Data input. "Q" outputs are available from each of the four stages on both registers. All register stages are D-type, master-slave flip-flops. The logic level present at the Data input is transferred into the first register stage and shifted over one stage at each positive-going clock transition. Resetting of all stages is accomplished by a high level on the reset line.

- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 µA
- High Noise Immunity Characteristic of CMOS Devices



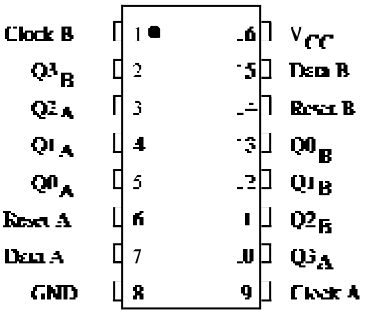
ORDERING INFORMATION
SL74HC4015N Plastic
SL74HC4015D SOIC
T_A = -55° to 125° C for all packages

LOGIC DIAGRAM



PIN 16 = V_{CC}
PIN 8 = GND

PIN ASSIGNMENT



FUNCTION TABLE

Inputs			Outputs	
Clock	Data	Reset	Q_0	Q_n
↑	L	L	L	Q_{n-1}
↑	H	L	H	Q_{n-1}
↓	X	L	Q_0^*	Q_n^*
X	X	H	L	L

* = No Change
X = don' t care

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	-1.5 to V_{CC} +1.5	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	±20	mA
I_{OUT}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: : - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	V_{CC} =2.0 V	0	1000	ns
		V_{CC} =4.5 V	0	500	
		V_{CC} =6.0 V	0	400	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS(Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25 °C to -55°C	≤85 °C	≤125 °C	
V_{IH}	Minimum High-Level Input Voltage	V_{OUT}= 0.1 V or V_{CC}-0.1 V $\lvert I_{OUT}\rvert \leq 20$ µA	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low -Level Input Voltage	V_{OUT}=0.1 V or V_{CC}-0.1 V $\lvert I_{OUT}\rvert \leq 20$ µA	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \leq 20$ µA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{IN}= V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \leq 4.0$ mA $\lvert I_{OUT}\rvert \leq 5.2$ mA	 4.5 6.0	 3.98 5.48	 3.84 5.34	 3.7 5.2	
V_{OL}	Maximum Low-Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \leq 20$ µA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{IN}= V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \leq 4.0$ mA $\lvert I_{OUT}\rvert \leq 5.2$ mA	 4.5 6.0	 0.26 0.26	 0.33 0.33	 0.4 0.4	
I_{IN}	Maximum Input Leakage Current	V_{IN}=V_{CC} or GND	6.0	±0.1	±1.0	±1.0	µA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{IN}=V_{CC} or GND I_{OUT}=0µA	6.0	8.0	80	160	µA

AC ELECTRICAL CHARACTERISTICS (C_L=50pF,Input t_r=t_f=6.0 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit 25 °C to -55°C	≤85°C	≤125°C	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figure 2)	2.0	6	4.8	4	MHz
		4.5	30	24	20	
		6.0	35	28	24	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock to Q (Figures 2 and 5)	2.0	175	220	265	ns
		4.5	35	44	53	
		6.0	30	37	45	
t_{PHL}	Maximum Propagation Delay, Reset to Q (Figures 1 and 5)	2.0	205	255	310	ns
		4.5	41	51	62	
		6.0	35	43	53	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 3 and 5)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C_{IN}	Maximum Input Capacitance	-	10	10	10	pF

C_{PD}	Power Dissipation Capacitance (Per Latch)	Typical @25°C,V_{CC}=5.0 V	pF
	Used to determine the no-load dynamic power consumption: $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$	140	

TIMING REQUIREMENTS (C_L=50pF,Input t_r=t_f=6.0 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit 25 °C to -55°C	≤85°C	≤125°C	Unit
t_{su}	Minimum Setup Time, D to Clock (Figure 4)	2.0	50	65	75	ns
		4.5	10	13	15	
		6.0	9.0	11	13	
t_h	Minimum Hold Time, Clock to D (Figure 4)	2.0	5	5	5	ns
		4.5	5	5	5	
		6.0	5	5	5	
t_{rec}	Minimum Recovery Time, Reset to Clock (Figure 1)	2.0	5	5	5	ns
		4.5	5	5	5	
		6.0	5	5	5	
t_w	Minimum Pulse Width, Reset (Figure 1)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t_w	Minimum Pulse Width, Clock (Figure 4)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

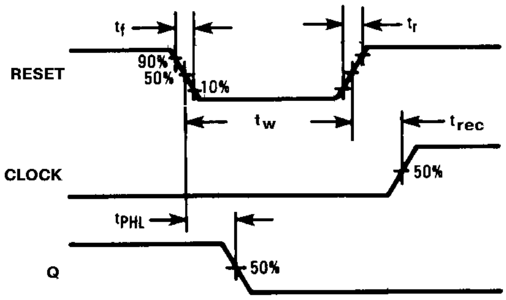


Figure 1. Switching Waveforms

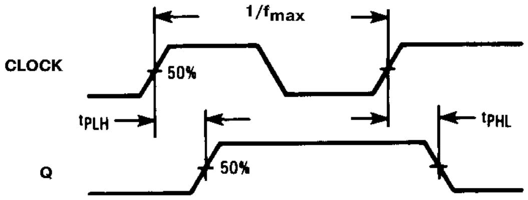


Figure 2. Switching Waveforms

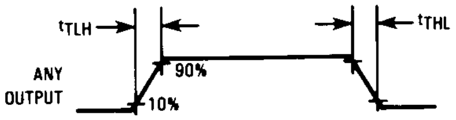


Figure 3. Switching Waveforms

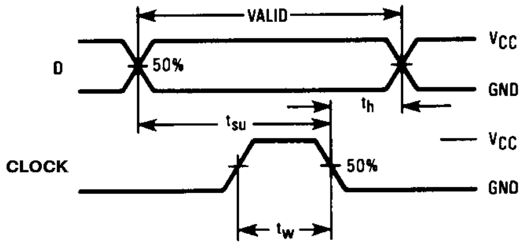
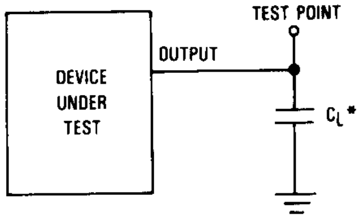


Figure 4. Switching Waveforms



*Includes all probe and jig capacitance.

Figure 5. Test Circuit

EXPANDED LOGIC DIAGRAM