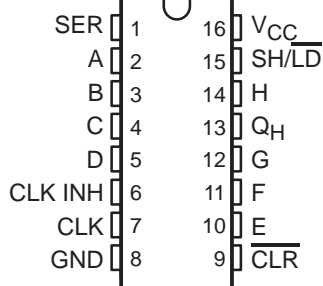


SN54HC166, SN74HC166 8-BIT PARALLEL-LOAD SHIFT REGISTERS

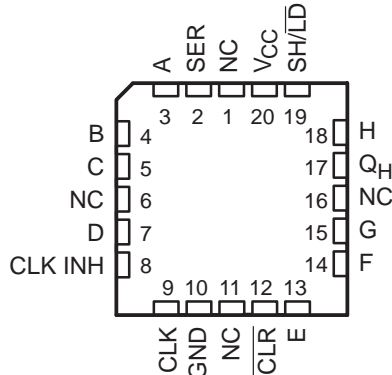
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- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 80- μ A Max I_{CC}
- Typical $t_{pd} = 13$ ns
- ± 4 -mA Output Drive at 5 V
- Low Input Current of 1 μ A Max
- Synchronous Load
- Direct Overriding Clear
- Parallel-to-Serial Conversion

SN54HC166 . . . J OR W PACKAGE
SN74HC166 . . . D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54HC166 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

ORDERING INFORMATION

| TA | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------|--------------|-----------------------|------------------|
| -40°C to 85°C | PDIP – N | Tube of 25 | SN74HC166N | SN74HC166N |
| | SOIC – D | Tube of 40 | SN74HC166D | HC166 |
| | | Reel of 2500 | SN74HC166DR | |
| | | Reel of 250 | SN74HC166DT | |
| | SOP – NS | Reel of 2000 | SN74HC166NSR | HC166 |
| | SSOP – DB | Reel of 2000 | SN74HC166DBR | HC166 |
| -55°C to 125°C | TSSOP – PW | Tube of 90 | SN74HC166PW | HC166 |
| | | Reel of 2000 | SN74HC166PWR | |
| | | Reel of 250 | SN74HC166PWT | |
| -55°C to 125°C | CDIP – J | Tube of 25 | SNJ54HC166J | SNJ54HC166J |
| | CFP – W | Tube of 150 | SNJ54HC166W | SNJ54HC166W |
| | LCCC – FK | Tube of 55 | SNJ54HC166FK | SNJ54HC166FK |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54HC166, SN74HC166

8-BIT PARALLEL-LOAD SHIFT REGISTERS

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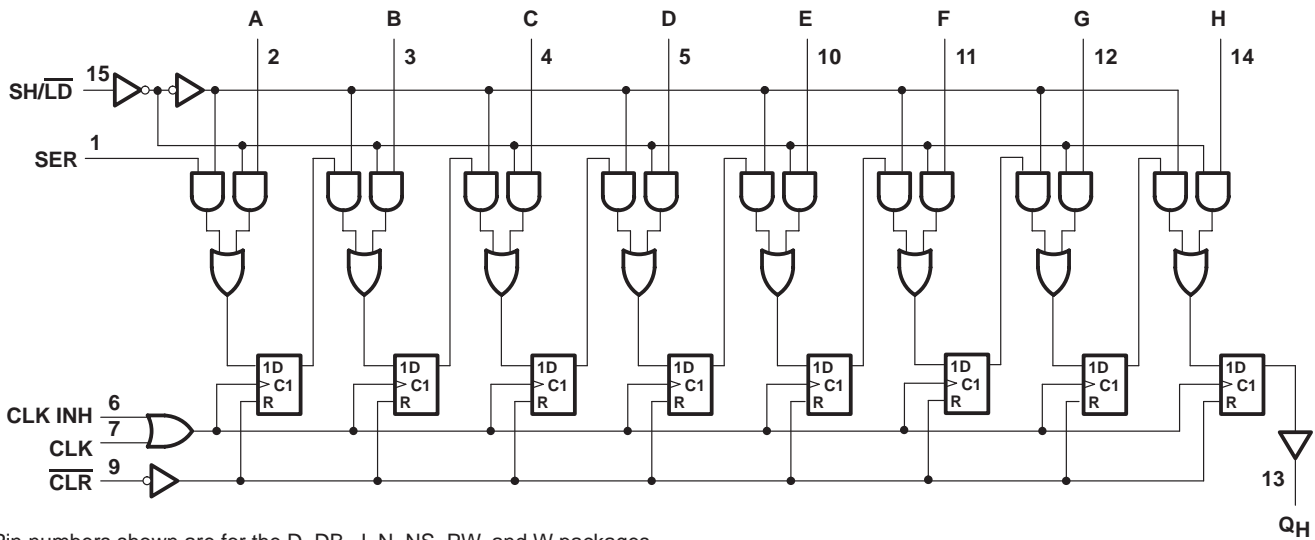
description/ordering information (continued)

These parallel-in or serial-in, serial-out registers feature gated clock (CLK, CLK INH) inputs and an overriding clear ($\overline{\text{CLR}}$) input. The parallel-in or serial-in modes are established by the shift/load ($\text{SH}/\overline{\text{LD}}$) input. When high, $\text{SH}/\overline{\text{LD}}$ enables the serial (SER) data input and couples the eight flip-flops for serial shifting with each clock (CLK) pulse. When low, the parallel (broadside) data inputs are enabled, and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high-level edge of CLK through a 2-input positive-NOR gate, permitting one input to be used as a clock-enable or clock-inhibit function. Holding either CLK or CLK INH high inhibits clocking; holding either low enables the other clock input. This allows the system clock to be free running, and the register can be stopped on command with the other clock input. CLK INH should be changed to the high level only when CLK is high. $\overline{\text{CLR}}$ overrides all other inputs, including CLK, and resets all flip-flops to zero.

FUNCTION TABLE

| INPUTS | | | | | | OUTPUTS | | |
|-------------------------|----------------------------------|---------|------------|-----|-----------------------|----------|----------|----------|
| | | | | | | INTERNAL | | Q_H |
| $\overline{\text{CLR}}$ | $\text{SH}/\overline{\text{LD}}$ | CLK INH | CLK | SER | PARALLEL A . . . H | Q_A | Q_B | |
| L | X | X | X | X | X | L | L | L |
| H | X | L | L | X | X | Q_{A0} | Q_{B0} | Q_{H0} |
| H | L | L | \uparrow | X | a . . . h | a | b | h |
| H | H | L | \uparrow | H | X | H | Q_{An} | Q_{Gn} |
| H | H | L | \uparrow | L | X | L | Q_{An} | Q_{Gn} |
| H | X | H | \uparrow | X | X | Q_{A0} | Q_{B0} | Q_{H0} |

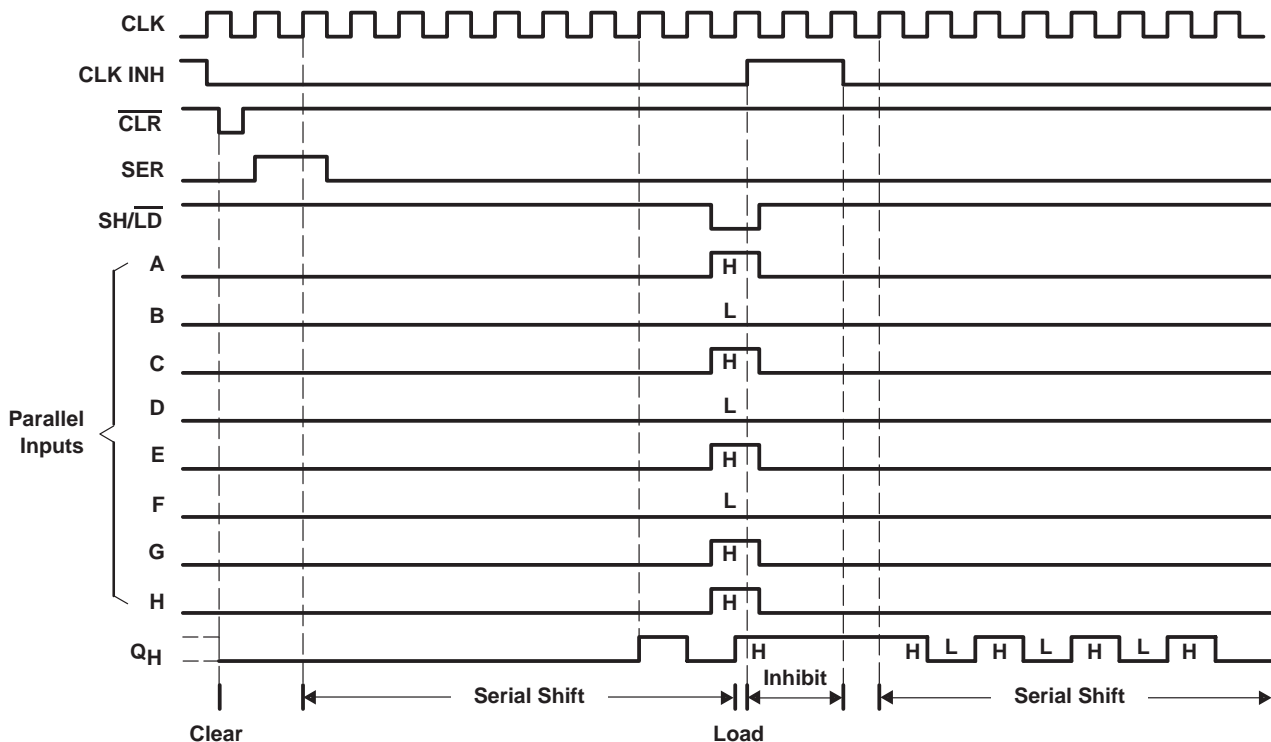
logic diagram (positive logic)



SN54HC166, SN74HC166 8-BIT PARALLEL-LOAD SHIFT REGISTERS

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typical clear, shift, load, inhibit, and shift sequence



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|----------------|
| Supply voltage range, V_{CC} | -0.5 V to 7 V |
| Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) | ± 20 mA |
| Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) | ± 20 mA |
| Continuous output current, I_O ($V_O = 0$ to V_{CC}) | ± 25 mA |
| Continuous current through V_{CC} or GND | ± 50 mA |
| Package thermal impedance, θ_{JA} (see Note 2): D package | 73°C/W |
| DB package | 82°C/W |
| N package | 67°C/W |
| NS package | 64°C/W |
| PW package | 108°C/W |
| Storage temperature range, T_{stg} | -65°C to 150°C |

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

SN54HC166, SN74HC166

8-BIT PARALLEL-LOAD SHIFT REGISTERS

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recommended operating conditions (see Note 3)

| | | SN54HC166 | | | SN74HC166 | | | UNIT |
|-----------------------------|---------------------------------|-------------------------|----------|------|-----------|----------|-----|------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V_{CC} | Supply voltage | 2 | 5 | 6 | 2 | 5 | 6 | V |
| V_{IH} | High-level input voltage | $V_{CC} = 2\text{ V}$ | | 1.5 | 1.5 | | V | |
| | | $V_{CC} = 4.5\text{ V}$ | | 3.15 | 3.15 | | | |
| | | $V_{CC} = 6\text{ V}$ | | 4.2 | 4.2 | | | |
| V_{IL} | Low-level input voltage | $V_{CC} = 2\text{ V}$ | | 0.5 | | 0.5 | V | |
| | | $V_{CC} = 4.5\text{ V}$ | | 1.35 | | 1.35 | | |
| | | $V_{CC} = 6\text{ V}$ | | 1.8 | | 1.8 | | |
| V_I | Input voltage | 0 | V_{CC} | | 0 | V_{CC} | | V |
| V_O | Output voltage | 0 | V_{CC} | | 0 | V_{CC} | | V |
| $\Delta t/\Delta v^\dagger$ | Input transition rise/fall time | $V_{CC} = 2\text{ V}$ | | 1000 | | 1000 | | ns |
| | | $V_{CC} = 4.5\text{ V}$ | | 500 | | 500 | | |
| | | $V_{CC} = 6\text{ V}$ | | 400 | | 400 | | |
| T_A | Operating free-air temperature | -55 | 125 | | -40 | 85 | | °C |

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

† If this device is used in the threshold region (from $V_{IL\text{max}} = 0.5\text{ V}$ to $V_{IH\text{min}} = 1.5\text{ V}$), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at $t_f = 1000\text{ ns}$ and $V_{CC} = 2\text{ V}$ does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | V_{CC} | $T_A = 25^\circ\text{C}$ | | | SN54HC166 | | SN74HC166 | | UNIT | |
|-----------|--------------------------------|-----------------------------|------------|--------------------------|-----------|-----------|-----------|------------|-----------|------------|------|---------------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | | |
| V_{OH} | $V_I = V_{IH}$ or V_{IL} | $I_{OH} = -20\ \mu\text{A}$ | 2 V | 1.9 | 1.998 | | 1.9 | | 1.9 | V | | |
| | | | 4.5 V | 4.4 | 4.499 | | 4.4 | | 4.4 | | | |
| | | | 6 V | 5.9 | 5.999 | | 5.9 | | 5.9 | | | |
| | | $I_{OH} = -4\text{ mA}$ | 4.5 V | 3.98 | 4.3 | | 3.7 | | 3.84 | | | |
| | | | 6 V | 5.48 | 5.8 | | 5.2 | | 5.34 | | | |
| V_{OL} | $V_I = V_{IH}$ or V_{IL} | $I_{OL} = 20\ \mu\text{A}$ | 2 V | | 0.002 | 0.1 | | 0.1 | | V | | |
| | | | 4.5 V | | 0.001 | 0.1 | | 0.1 | | | | |
| | | | 6 V | | 0.001 | 0.1 | | 0.1 | | | | |
| | | $I_{OL} = 4\text{ mA}$ | 4.5 V | | 0.17 | 0.26 | | 0.4 | | | 0.33 | |
| | | | 6 V | | 0.15 | 0.26 | | 0.4 | | | 0.33 | |
| I_I | $V_I = V_{CC}$ or 0 | | 6 V | | ± 0.1 | ± 100 | | ± 1000 | | ± 1000 | nA | |
| I_{CC} | $V_I = V_{CC}$ or 0, $I_O = 0$ | | 6 V | | | | 8 | | 160 | | 80 | μA |
| C_i | | | 2 V to 6 V | | 3 | 10 | | 10 | | | 10 | pF |



SN54HC166, SN74HC166 8-BIT PARALLEL-LOAD SHIFT REGISTERS

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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

| | | V _{CC} | T _A = 25°C | | SN54HC166 | | SN74HC166 | | UNIT | | |
|-------------------------|--|--|-----------------------|-----|-----------|-----|-----------|-----|------|--|----|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | | | |
| f _{clock} | Clock frequency | 2 V | 6 | | 4.2 | | 5 | | MHz | | |
| | | 4.5 V | 31 | | 21 | | 25 | | | | |
| | | 6 V | 36 | | 25 | | 29 | | | | |
| t _w | $\overline{\text{CLR}}$ low | 2 V | 100 | | 150 | | 125 | | ns | | |
| | | 4.5 V | 20 | | 30 | | 25 | | | | |
| | | 6 V | 17 | | 26 | | 21 | | | | |
| | CLK high or low | 2 V | 80 | | 120 | | 100 | | | | |
| | | 4.5 V | 16 | | 24 | | 20 | | | | |
| | | 6 V | 14 | | 20 | | 17 | | | | |
| t _{su} | SH/ $\overline{\text{LD}}$ high before CLK↑ | 2 V | 145 | | 220 | | 180 | | ns | | |
| | | 4.5 V | 29 | | 44 | | 36 | | | | |
| | | 6 V | 25 | | 38 | | 31 | | | | |
| | SER before CLK↑ | 2 V | 80 | | 120 | | 100 | | | | |
| | | 4.5 V | 16 | | 24 | | 20 | | | | |
| | | 6 V | 14 | | 20 | | 17 | | | | |
| | CLK INH low before CLK↑ | 2 V | 100 | | 150 | | 125 | | | | |
| | | 4.5 V | 20 | | 30 | | 25 | | | | |
| | | 6 V | 17 | | 26 | | 21 | | | | |
| | Data before CLK↑ | 2 V | 80 | | 120 | | 100 | | | | |
| | | 4.5 V | 16 | | 24 | | 20 | | | | |
| | | 6 V | 14 | | 20 | | 17 | | | | |
| | $\overline{\text{CLR}}$ inactive before CLK↑ | 2 V | 40 | | 60 | | 50 | | | | |
| | | 4.5 V | 8 | | 12 | | 10 | | | | |
| | | 6 V | 7 | | 10 | | 9 | | | | |
| | t _h | SH/ $\overline{\text{LD}}$ high after CLK↑ | 2 V | 0 | | 0 | | 0 | | | ns |
| | | | 4.5 V | 0 | | 0 | | 0 | | | |
| | | | 6 V | 0 | | 0 | | 0 | | | |
| SER after CLK↑ | | 2 V | 5 | | 5 | | 5 | | | | |
| | | 4.5 V | 5 | | 5 | | 5 | | | | |
| | | 6 V | 5 | | 5 | | 5 | | | | |
| CLK INH high after CLK↑ | | 2 V | 0 | | 0 | | 0 | | | | |
| | | 4.5 V | 0 | | 0 | | 0 | | | | |
| | | 6 V | 0 | | 0 | | 0 | | | | |
| Data after CLK↑ | | 2 V | 5 | | 5 | | 5 | | | | |
| | | 4.5 V | 5 | | 5 | | 5 | | | | |
| | | 6 V | 5 | | 5 | | 5 | | | | |



SN54HC166, SN74HC166

8-BIT PARALLEL-LOAD SHIFT REGISTERS

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switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

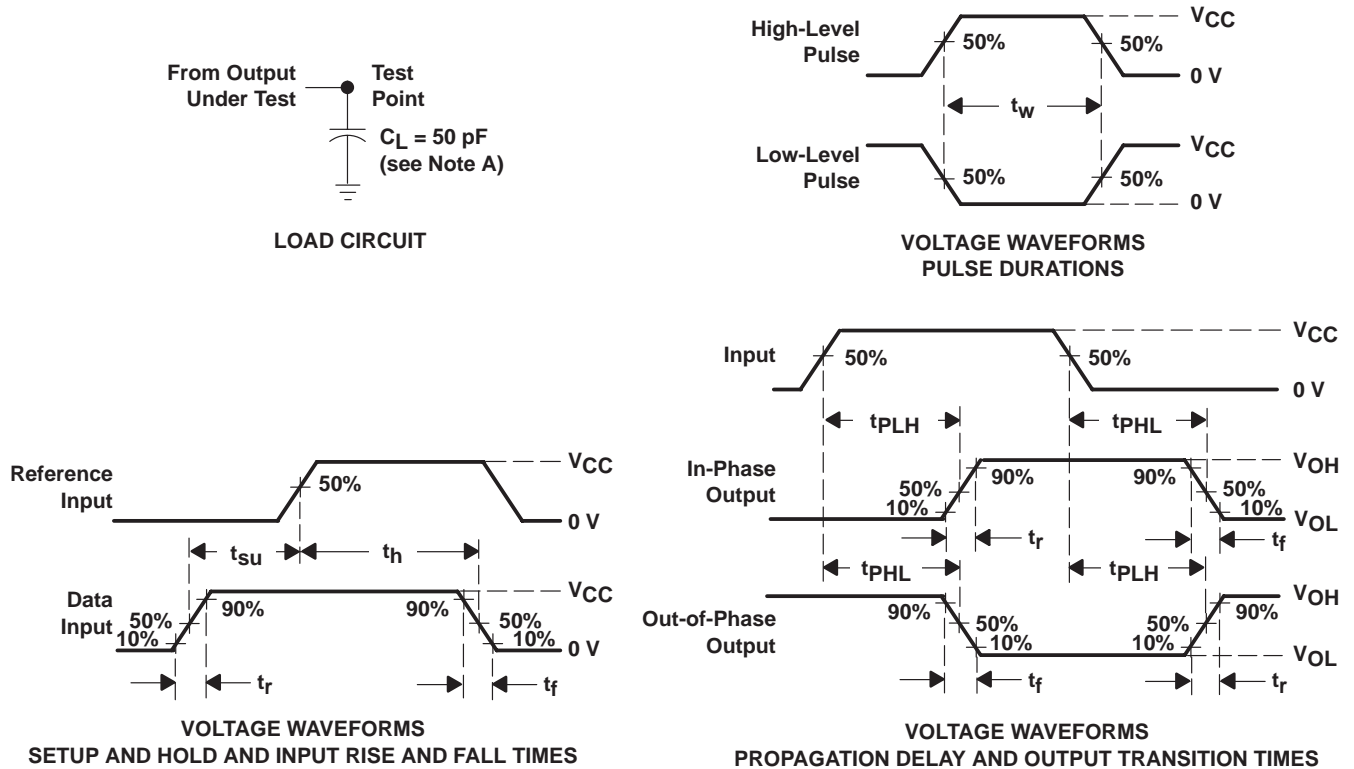
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} | T _A = 25°C | | | SN54HC166 | | SN74HC166 | | UNIT |
|------------------|-------------------------|----------------|-----------------|-----------------------|-----|-----|-----------|-----|-----------|-----|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| f _{max} | | | 2 V | 6 | 11 | | 4.2 | | 5 | MHz | |
| | | | 4.5 V | 31 | 36 | | 21 | | 25 | | |
| | | | 6 V | 36 | 45 | | 25 | | 29 | | |
| t _{PHL} | $\overline{\text{CLR}}$ | Q _H | 2 V | | 62 | 120 | | 180 | | 150 | ns |
| | | | 4.5 V | | 18 | 24 | | 36 | | 30 | |
| | | | 6 V | | 13 | 20 | | 31 | | 26 | |
| t _{pd} | CLK | Q _H | 2 V | | 75 | 150 | | 225 | | 190 | ns |
| | | | 4.5 V | | 15 | 30 | | 45 | | 38 | |
| | | | 6 V | | 13 | 26 | | 38 | | 32 | |
| t _t | | Any | 2 V | | 38 | 75 | | 110 | | 95 | ns |
| | | | 4.5 V | | 8 | 15 | | 22 | | 19 | |
| | | | 6 V | | 6 | 13 | | 19 | | 16 | |

operating characteristics, T_A = 25°C

| PARAMETER | TEST CONDITIONS | TYP | UNIT |
|---|-----------------|-----|------|
| C _{pd} Power dissipation capacitance | No load | 50 | pF |



PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and test-fixture capacitance.
 B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 6 \text{ ns}$, $t_f = 6 \text{ ns}$.
 C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
 D. The outputs are measured one at a time with one input transition per measurement.
 E. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



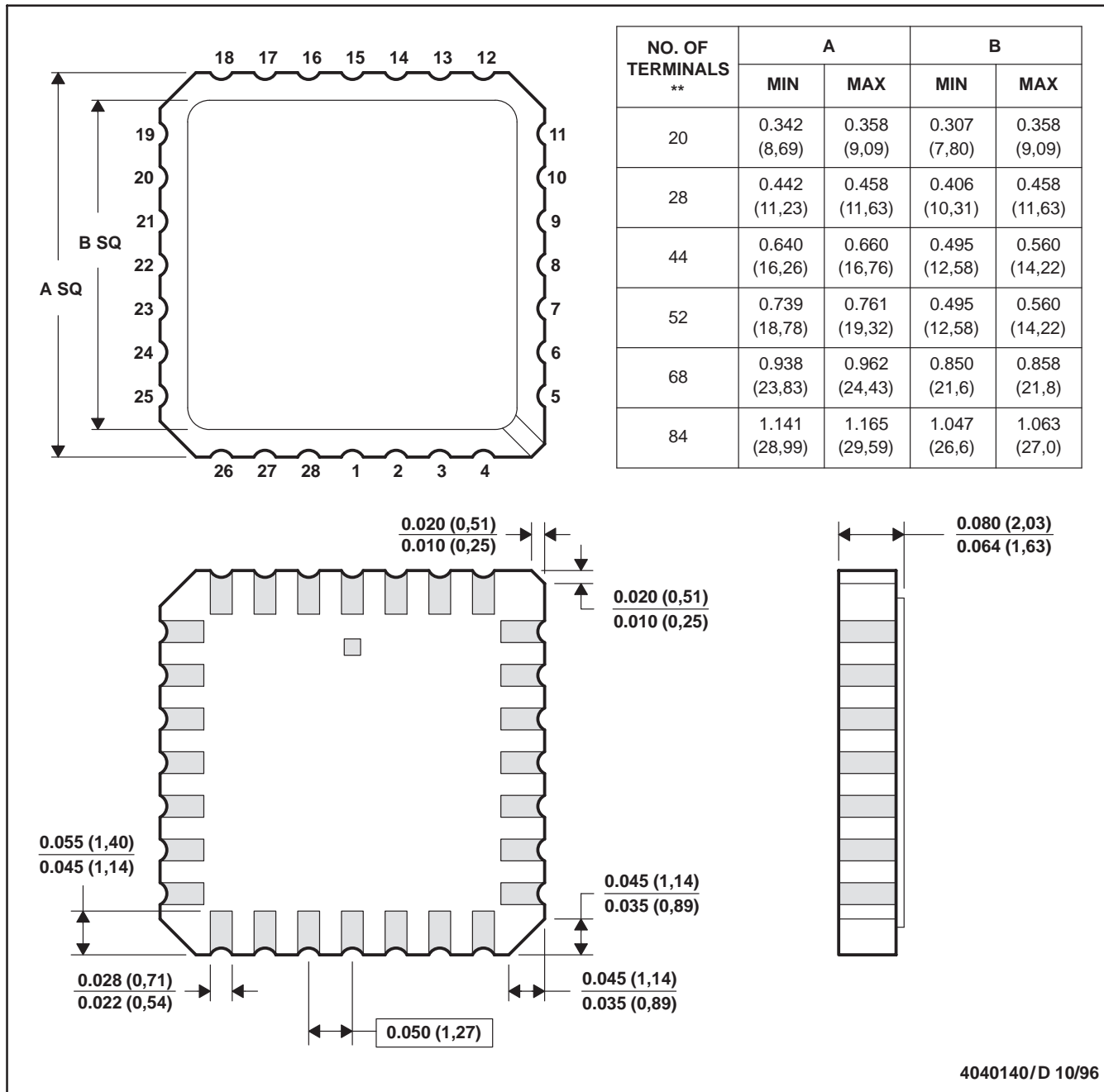
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN

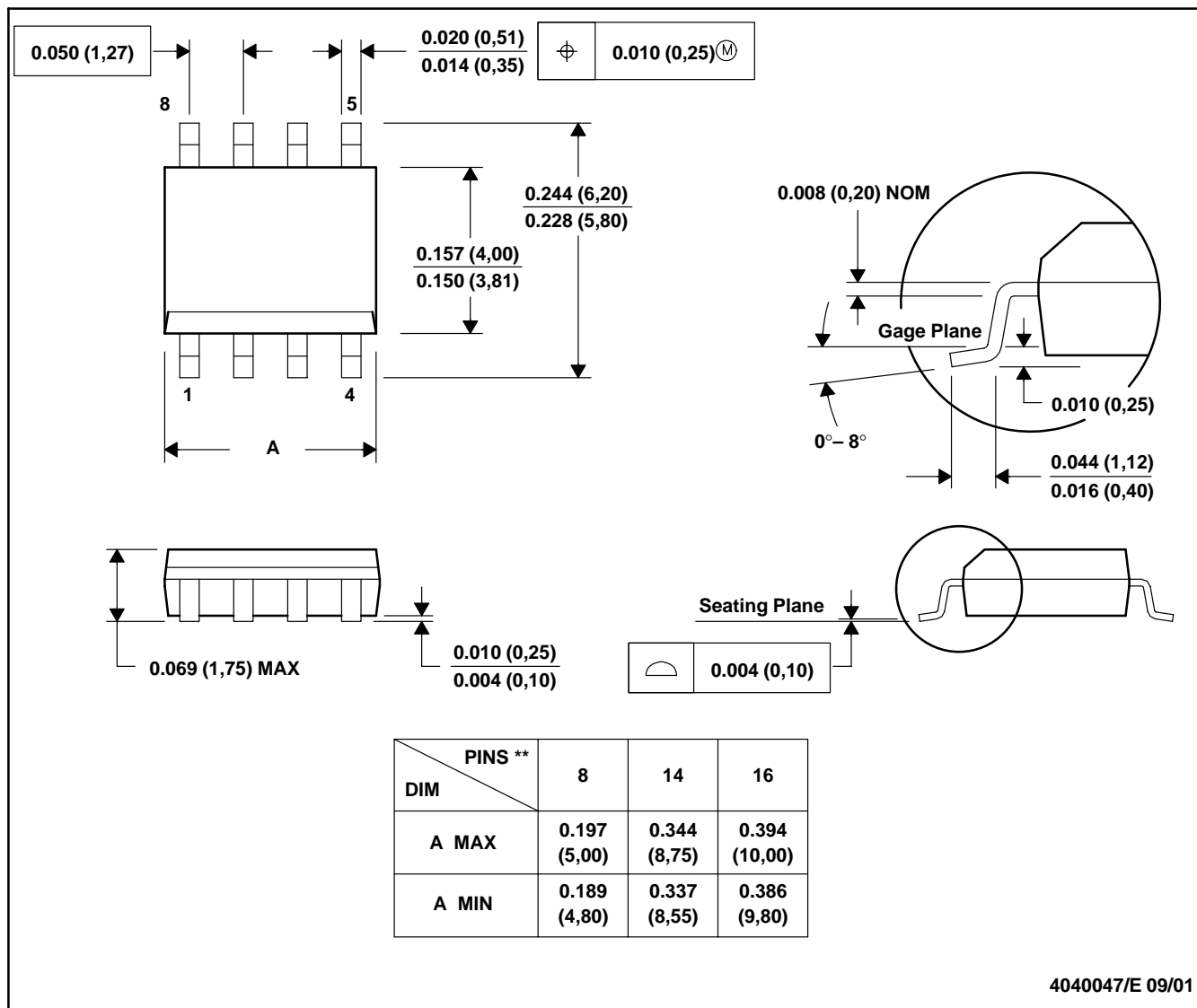


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-012

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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