

MC10H141

Four-Bit Universal Shift Register

The MC10H141 is a four-bit universal shift register. This device is a functional/pinout duplication of the standard MECL 10K part with 100% improvement in propagation delay and operation frequency and no increase in power supply current.

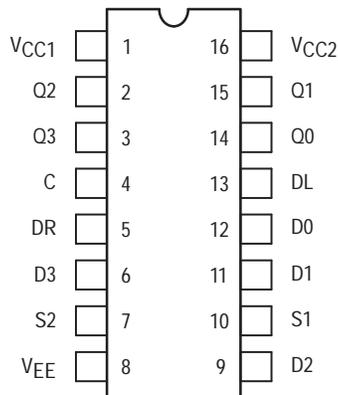
- Shift frequency, 250 MHz Min
- Power Dissipation, 425 mW Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

TRUTH TABLE

SELECT		OPERATING MODE	OUTPUTS			
S1	S2		Q0 _{n+1}	Q1 _{n+1}	Q2 _{n+1}	Q3 _{n+1}
L	L	Parallel Entry	D0	D1	D2	D3
L	H	Shift Right*	Q1 _n	Q2 _n	Q3 _n	DR
H	L	Shift Left*	DL	Q0 _n	Q1 _n	Q2 _n
H	H	Stop Shift	Q0 _n	Q1 _n	Q2 _n	Q3 _n

* Outputs as exist after pulse appears at "C" input with input conditions as shown (Pulse Positive transition of clock input).

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-Line Package.

For PLCC pin assignment, see the Pin Conversion Tables on page 18 of the ON Semiconductor MECL Data Book (DL122/D).



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MARKING DIAGRAMS



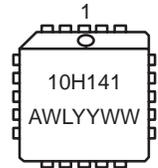
**CDIP-16
L SUFFIX
CASE 620**



**PDIP-16
P SUFFIX
CASE 648**



**PLCC-20
FN SUFFIX
CASE 775**



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H141L	CDIP-16	25 Units/Rail
MC10H141P	PDIP-16	25 Units/Rail
MC10H141FN	PLCC-20	46 Units/Rail

MC10H141

MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{EE}	Power Supply ($V_{CC} = 0$)	-8.0 to 0	Vdc
V_I	Input Voltage ($V_{CC} = 0$)	0 to V_{EE}	Vdc
I_{out}	Output Current – Continuous – Surge	50 100	mA
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range – Plastic – Ceramic	-55 to +150 -55 to +165	°C °C

ELECTRICAL CHARACTERISTICS ($V_{EE} = -5.2\text{ V} \pm 5\%$, See Note 1.)

Symbol	Characteristic	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
I_E	Power Supply Current	–	112	–	102	–	112	mA
I_{inH}	Input Current High Pins 5,6,9,11,12,13 Pins 7,10 Pin 4	–	405	–	255	–	255	μA
		–	416	–	260	–	260	
		–	510	–	320	–	320	
		–	510	–	320	–	320	
I_{inL}	Input Current Low	0.5	–	0.5	–	0.3	–	μA
V_{OH}	High Output Voltage	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
V_{OL}	Low Output Voltage	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
V_{IH}	High Input Voltage	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
V_{IL}	Low Input Voltage	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

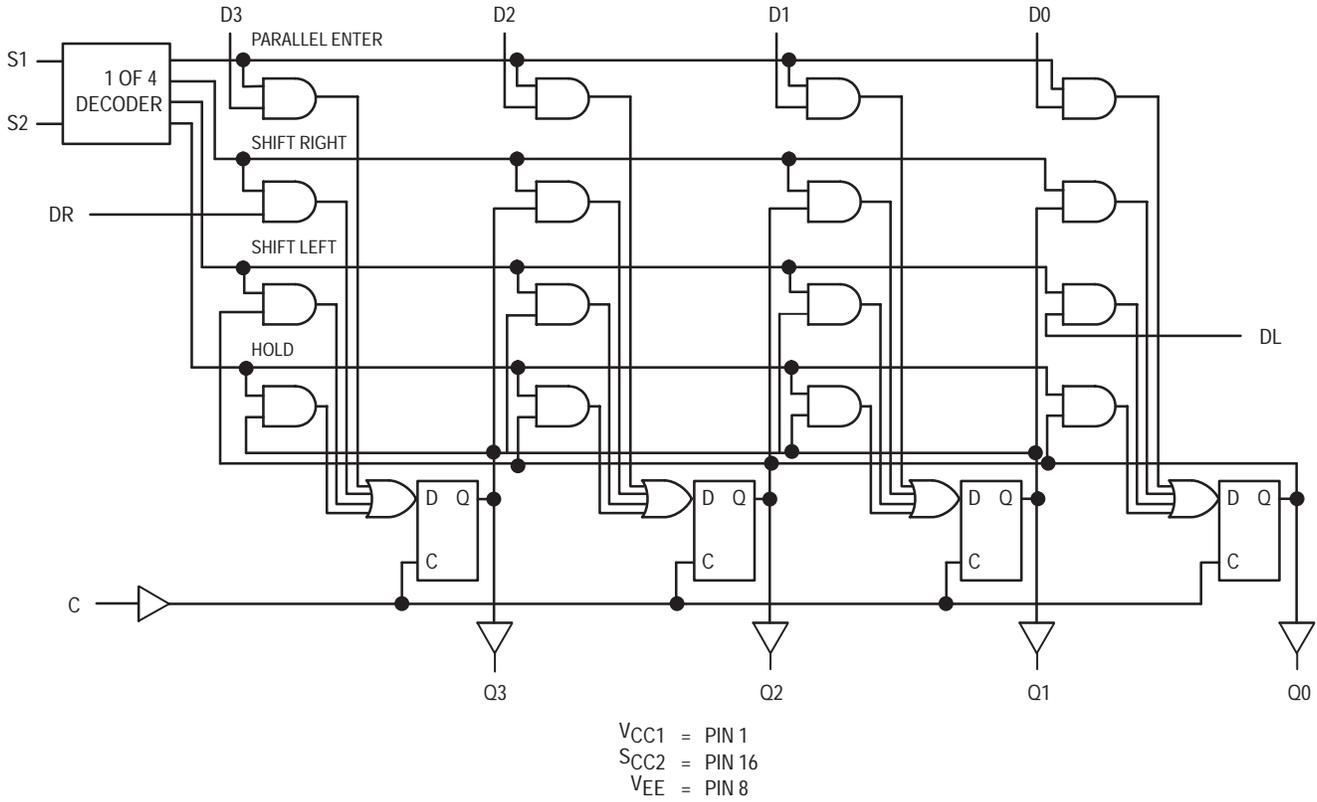
AC PARAMETERS

t_{pd}	Propagation Delay	1.0	2.0	1.0	2.0	1.1	2.1	ns
t_{hold}	Hold Time – Data, Select	1.0	–	1.0	–	1.0	–	ns
t_{set}	Set-up Time Data Select	1.5	–	1.5	–	1.5	–	ns
		3.0	–	3.0	–	3.0	–	
t_r	Rise Time	0.5	2.4	0.5	2.4	0.5	2.4	ns
t_f	Fall Time	0.5	2.4	0.5	2.4	0.5	2.4	ns
f_{shift}	Shift Frequency	250	–	250	–	250	–	MHz

- Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 ohm resistor to -2.0 volts.

MC10H141

LOGIC DIAGRAM



APPLICATION INFORMATION

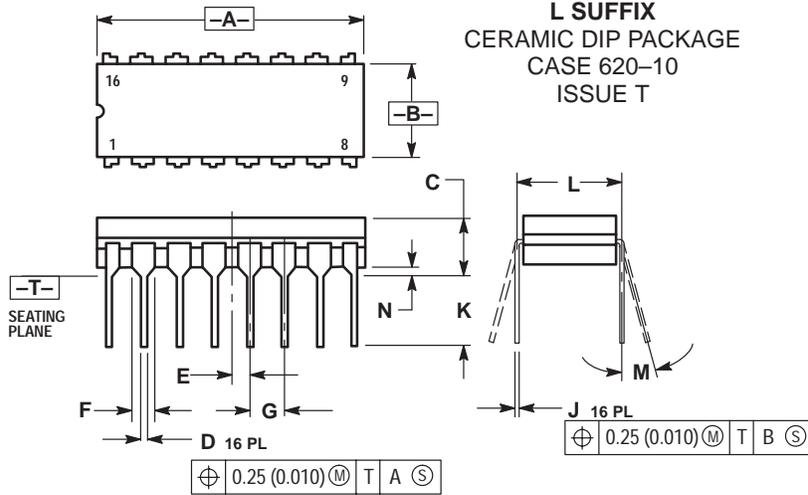
The MC10H141 is a four-bit universal shift register which performs shift left, or shift right, serial/parallel in, and serial/parallel out operations with no external gating. Inputs S1 and S2 control the four possible operations of the register without external gating of the clock. The flip-flops shift

information on the positive edge of the clock. The four operations are stop shift, shift left, shift right, and parallel entry of data. The other six inputs are all data type inputs; four for parallel entry data, and one for shifting in from the left (DL) and one for shifting in from the right (DR).

MC10H141

PACKAGE DIMENSIONS

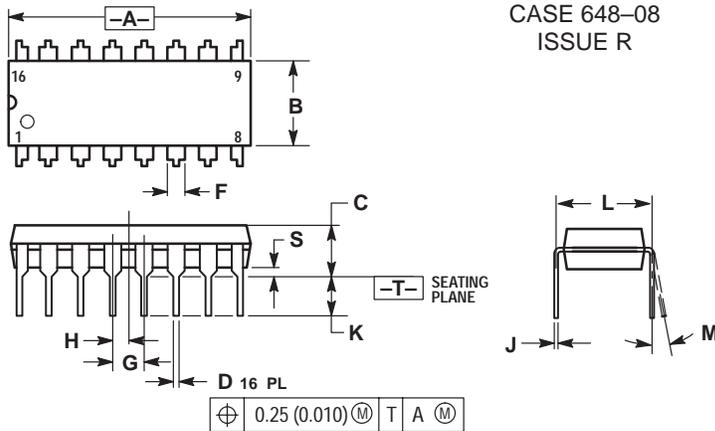
CDIP-16 L SUFFIX CERAMIC DIP PACKAGE CASE 620-10 ISSUE T



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
 4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	---	0.200	---	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

PDIP-16 P SUFFIX PLASTIC DIP PACKAGE CASE 648-08 ISSUE R



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
 5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

Notes

Notes

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