SONY

CXA1352AS

2-channel 5 Elements Graphic Equalizer IC

Description

The CXA1352AS is a bipolar IC for graphic equalizer use. All controls are DC performed while the addition of single-potentiometers easily composes a 2-channel graphic equalizer.

Features

- Microcomputer control possible
- Built-in electronic volume
- Built-in pseudo loudness function
- Built-in balance function
- Each channel corresponds to 5 elements
- 2 channels of FIX OUT and LINE OUT pins

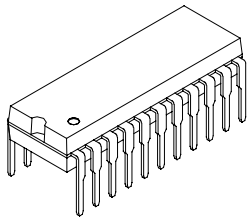
Applications

Graphic equalizer for cassette tape recorder with radio, mobile stereo and portable stereo

Structure

Bipolar silicon monolithic IC

22 pin SDIP (Plastic)



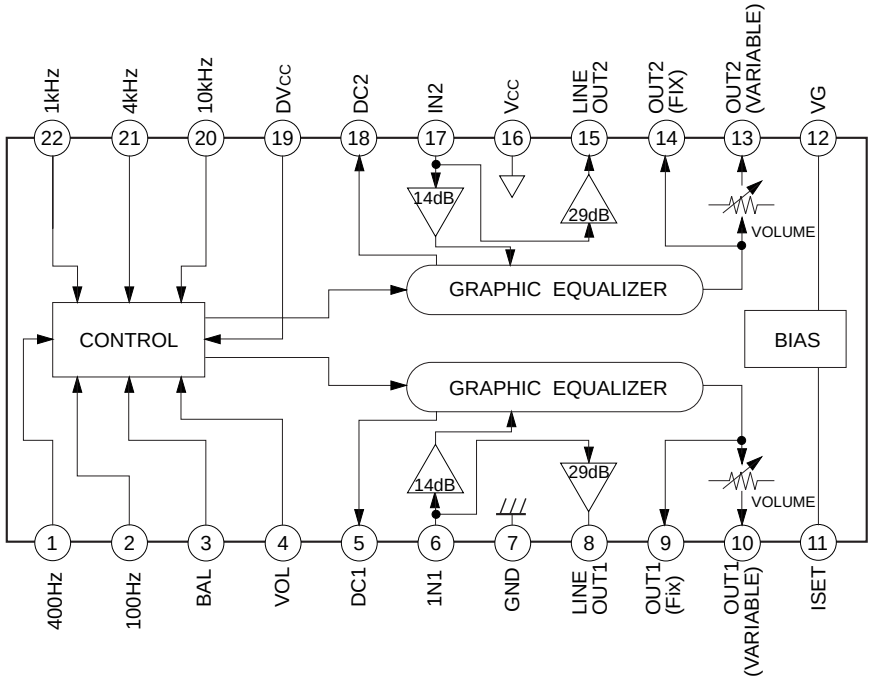
Absolute Maximum Ratings (Ta=25 °C)

• Supply voltage	V_{CC}	12	V
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	1200	mW

Operating Conditions

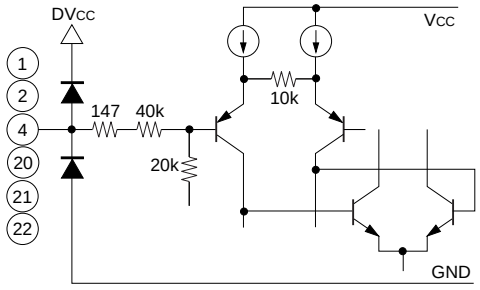
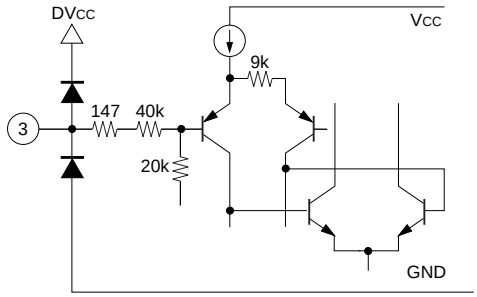
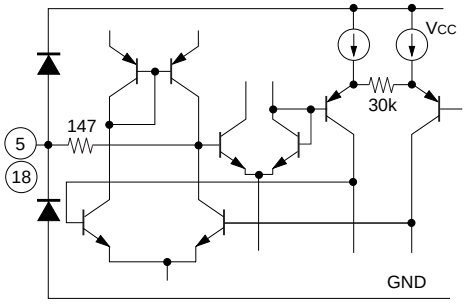
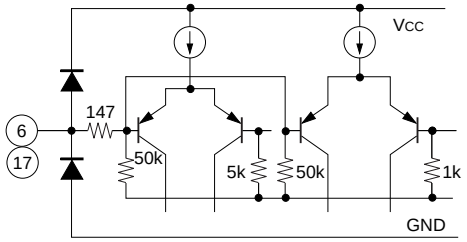
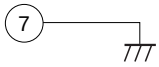
• Supply voltage	V_{CC}	4.0 to 10.0	V
	DV_{CC}	3.5 to V_{CC}	V
• Operating temperature	Topr	–20 to +75	°C

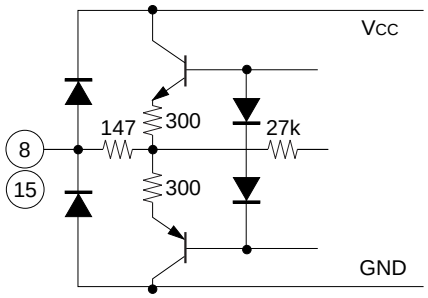
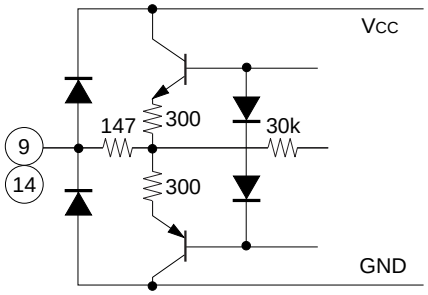
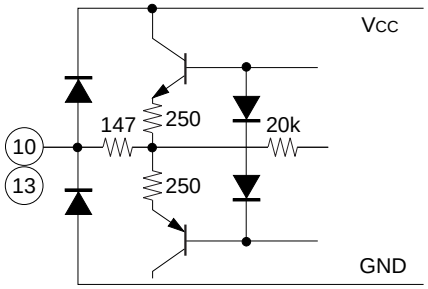
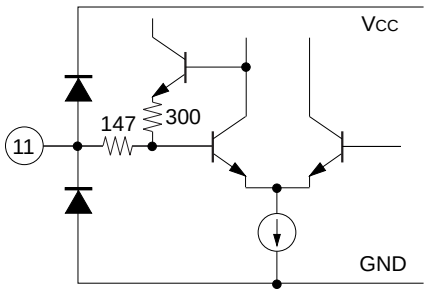
Block Diagram and Pin Configuration

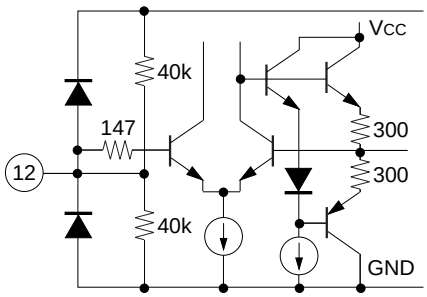
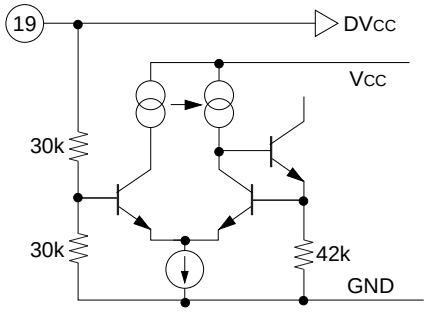


E91912B95-TE

Pin Description

Pin No.	Symbol	Voltage	I/O resistance	Equivalent circuit	Description
1 2 20 21 22	400 Hz 100 Hz 10 kHz 4 kHz 1 kHz	$\frac{DV_{CC}}{2}$	60 kΩ		Graphic equalizer control pin DC input
4	VOL				Volume control pin DC input
3	BAL	$\frac{DV_{CC}}{2}$	60 kΩ		Balance control pin DC input
5 18	DC1 DC2	$\frac{V_{CC}}{2}$	—		Connects the DC feedback capacitor of the LPF used in the 100 Hz graphic equalizer
6 17	IN1 IN2	$\frac{V_{CC}}{2}$	25 kΩ		Signal input pin
7	GND	GND			GND pin

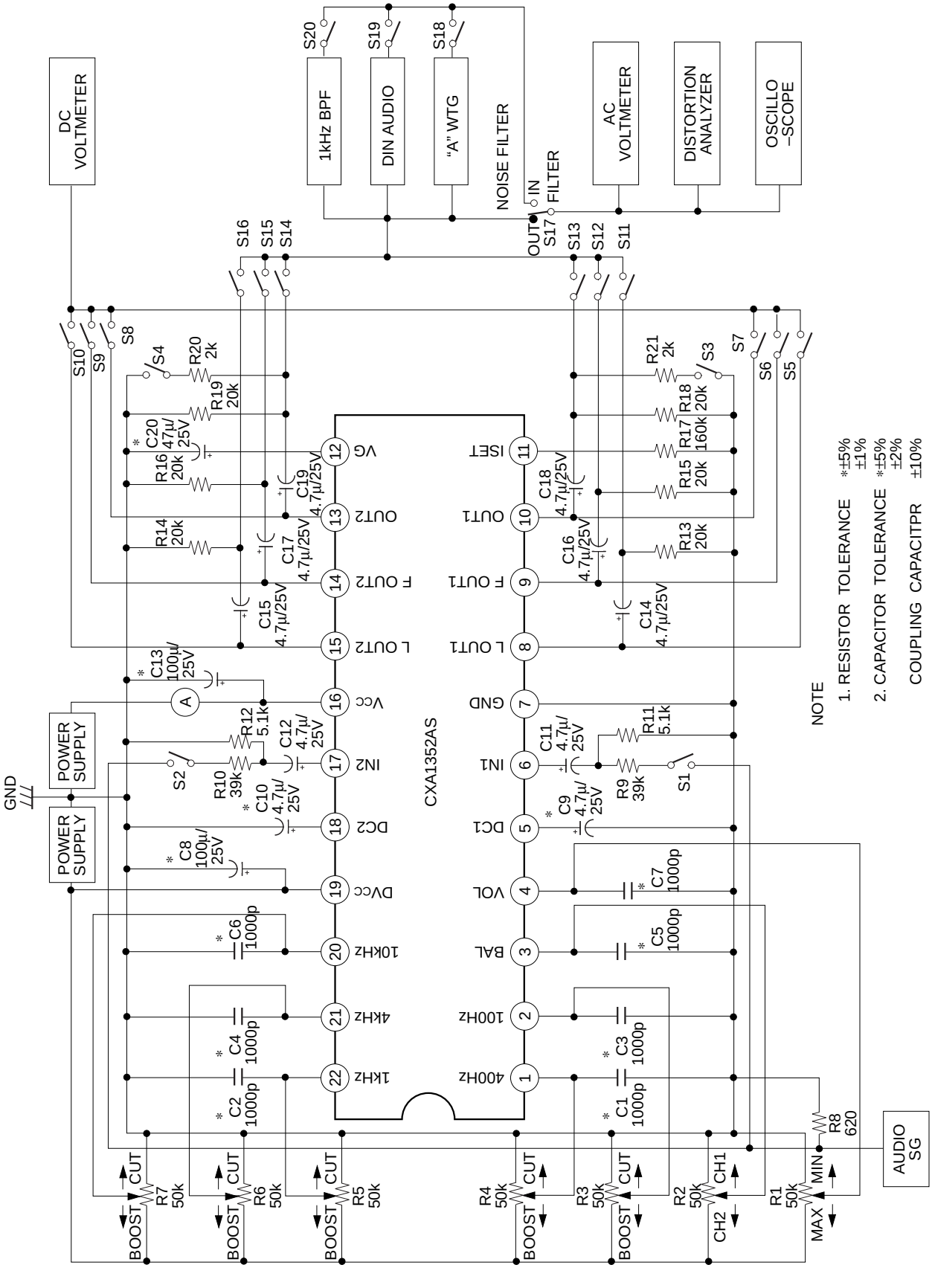
Pin No.	Symbol	Voltage	I/O resistance	Equivalent circuit	Description
8 15	L OUT1 L OUT2	$\frac{V_{CC}}{2}$	0		Line output pin
9 14	F OUT1 F OUT2	$\frac{V_{CC}}{2}$	0		Fix output pin
10 13	OUT1 OUT2	$\frac{V_{CC}}{2}$	0		Electronic volume output pin
11	ISET	1.3 V	0		Reference current setting pin (for graphic equalizer) Normally 160 kΩ resistor is connected

Pin No.	Symbol	Voltage	I/O resistance	Equivalent circuit	Description
12	VG	$\frac{V_{CC}}{2}$	20 kΩ		Signal reference voltage pin A capacitor is connected for ripple rejection
16	Vcc	Vcc			Power supply pin (operation)
19	DVcc	DVcc	60 kΩ		Power supply pin (control)

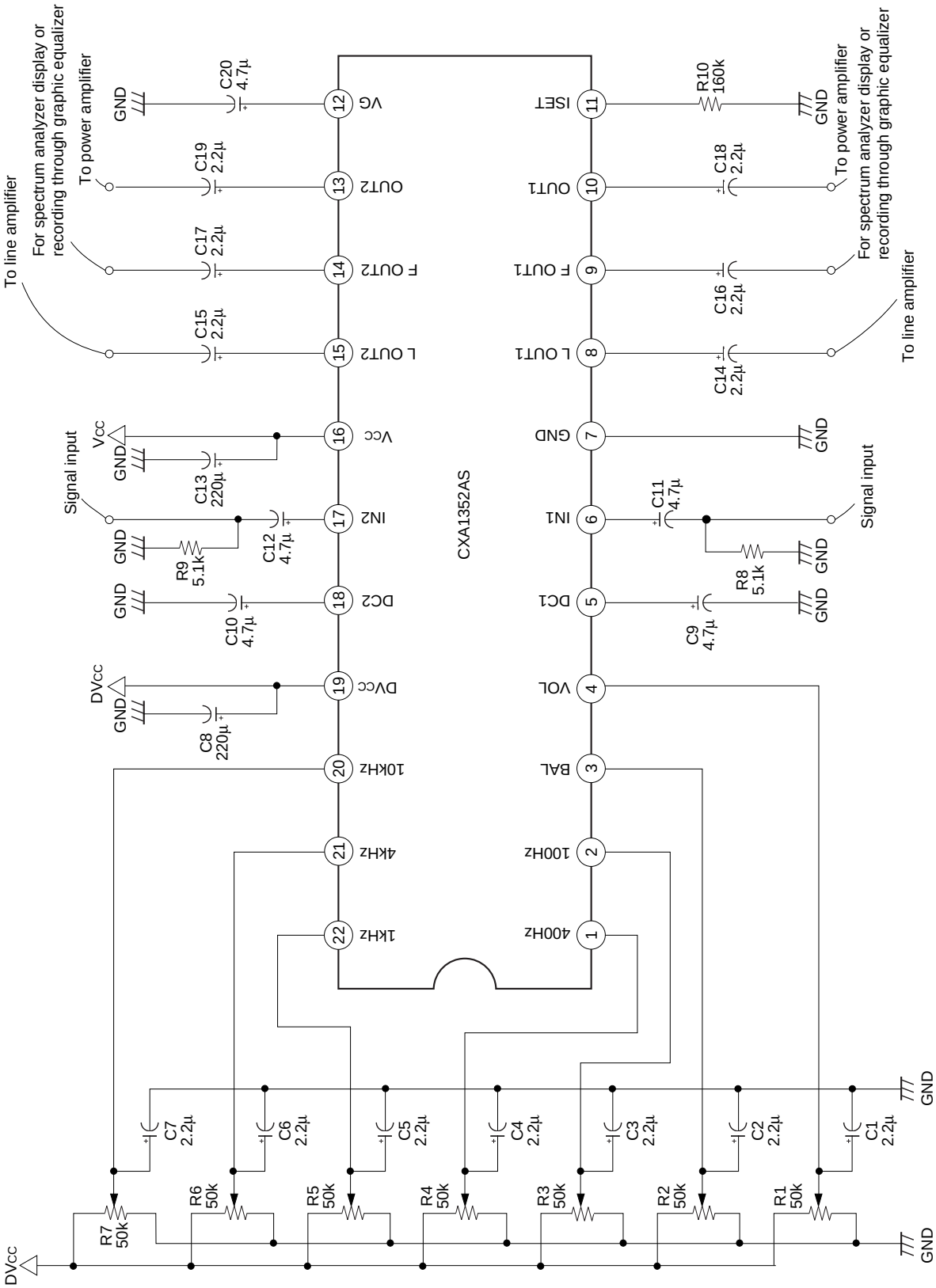
Electrical Characteristics (Ta=25 °C, V_{CC}=8 V, DV_{CC}=5 V)

No.	Item	Symbol	Test conditions	Min.	Typ.	Max.	Unit
1	Supply voltage (operation)	V_{CC}		4.0	—	10.0	V
2	Supply voltage (control)	DV_{CC}		3.5	—	V_{CC}	V
3	Current consumption	I_{CC}	Graphic equalizer ALL FLAT, Volume MID	8.0	12.0	16.0	mA
4	Reference input level	V_{IN}		—	–34.0	—	dBm
5	Reference output level	V_{OUT}	Graphic equalizer ALL FLAT, Volume MAX, f=1 kHz	–23.0	–20.0	–17.0	dBm
6	Reference LINE output level	V_{LINE}	f=1 kHz	–6.5	–4.5	–2.5	dBm
7	Reference FIX output level	V_{FIX}	Graphic equalizer ALL FLAT, f=1 kHz	–23.0	–20.0	–17.0	dBm
8	Graphic equalizer setting frequency (1)	GEQ1	LPF cut off frequency (–3 dB)	—	200	—	Hz
9	Graphic equalizer setting frequency (2)	GEQ2	BPF (1) central frequency	—	400	—	Hz
10	Graphic equalizer setting frequency (3)	GEQ3	BPF (2) central frequency	—	1.0	—	kHz
11	Graphic equalizer setting frequency (4)	GEQ4	BPF (3) central frequency	—	4.0	—	kHz
12	Graphic equalizer setting frequency (5)	GEQ5	HPF cut off frequency (–3 dB)	—	8.0	—	kHz
13	Graphic equalizer frequency deviation	Δ EQ	Cut off frequency and central frequency deviation	–20	0	20	%
14	Maximum boost (1)	GEQB1	f=400 Hz, 1 kHz, 4 kHz maximum boost	9.0	11.2	14.0	dB
15	Maximum boost (2)	GEQB2	f=100 Hz, 10 kHz maximum boost	8.0	10.7	14.0	dB
16	Maximum cut (1)	GEQC1	f=400 Hz, 1 kHz, 4kHz maximum cut	–13.0	–10.7	–8.5	dB
17	Maximum cut (2)	GEQC2	f=100 Hz, 10 kHz maximum cut R_L=2 kΩ, Graphic equalizer	–12.0	–9.5	–7.0	dB
18	Total harmonic distortion	THD	ALL FLAT, Volume MAX, f=1 kHz, Reference +10 dB is input	—	0.25	1.0	%
19	Volume attenuation (1)	VOL1	Graphic equalizer ALL FLAT, Volume MAX, f=1 kHz	–1.5	0	1.5	dB
20	Volume attenuation (2)	VOL2	Graphic equalizer ALL FLAT, Volume MIN, f=1 kHz	—	–94.4	–80.0	dB
21	Balance adjustment (1)	BAL1	Graphic equalizer ALL FLAT, BAL=MAX,Volume MAX, f=1kHz	—	0	—	dB
22	Balance adjustment (2)	BAL2	Graphic equalizer ALL FLAT, BAL=MIN, Volume MAX, f=1kHz	—	–66	—	dB
23	Noise level	V_{NOIS}	Rg=5 kΩ, Graphic equalizer ALL FLAT, Volume MAX, “A” WTG filter	—	–93.1	–88.0	dB
24	Output offset voltage	V_{OFF}	Graphic equalizer ALL FLAT, Volume MAX	3.5	4.0	4.5	V

Electrical Characteristics Test Circuit



Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Description of Operation

1. Graphic equalizer

• Conventional system

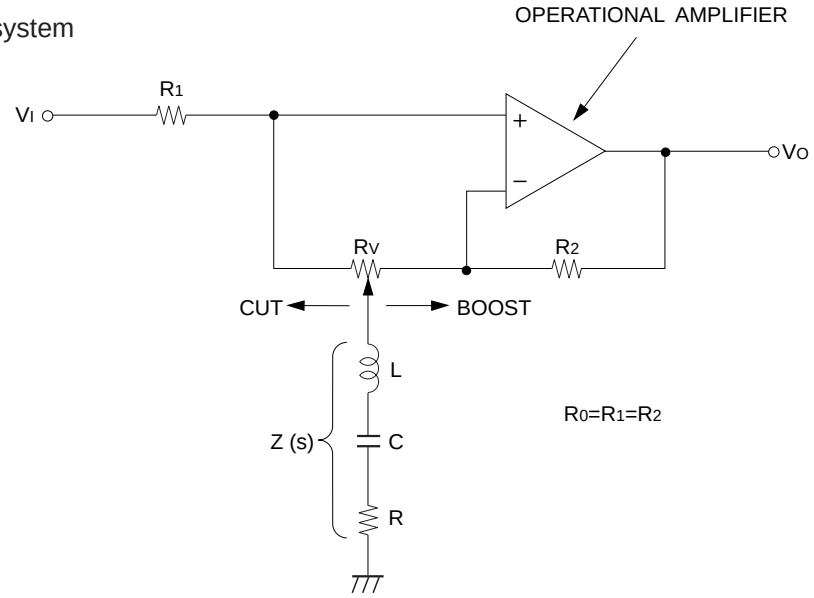


Fig. 1.

Fig. 1. indicates the conventional graphic equalizer system. This circuit performs boost and cut near "fo" controlled by the variable volume RV. ("fo" is resonance frequency determined by Z (s) (formed LCR).) The operation can be seen as follows : When the LCR circuit goes to the far left of RV, a state of graphic equalizer becomes maximum cut. At that time, assuming transmittance as T (s), we have

$$T(s) = \frac{Z(s)}{Z(s) + R_O}$$

Here as $Z(s) = sL + R + \frac{1}{sC}$

Then $T(s) = \frac{LCs^2 + RCs + 1}{LCs^2 + (R + Ro)\,Cs + 1}$

Defining fo as $f_O = \frac{\omega o}{2\pi}$, ωo as $\omega o = \frac{1}{LC}$, and Q as $Q = \frac{\omega oL}{R}$, we can obtain the frequency characteristics at cut.

Also, when LCR circuit goes to the far right of RV, a state of graphic equalizer becomes maximum boost. At that time transmittance is :

$$T(s) = \frac{Z(s) + R_O}{Z(s)} = \frac{LCs^2 + (R + Ro)\,Cs + 1}{LCs^2 + RCs + 1}$$

Defining fo, ωo and Q as for cut, we can obtain the frequency characteristics at boost.

Fig. 2. Indicates frequency characteristics at boost and cut.

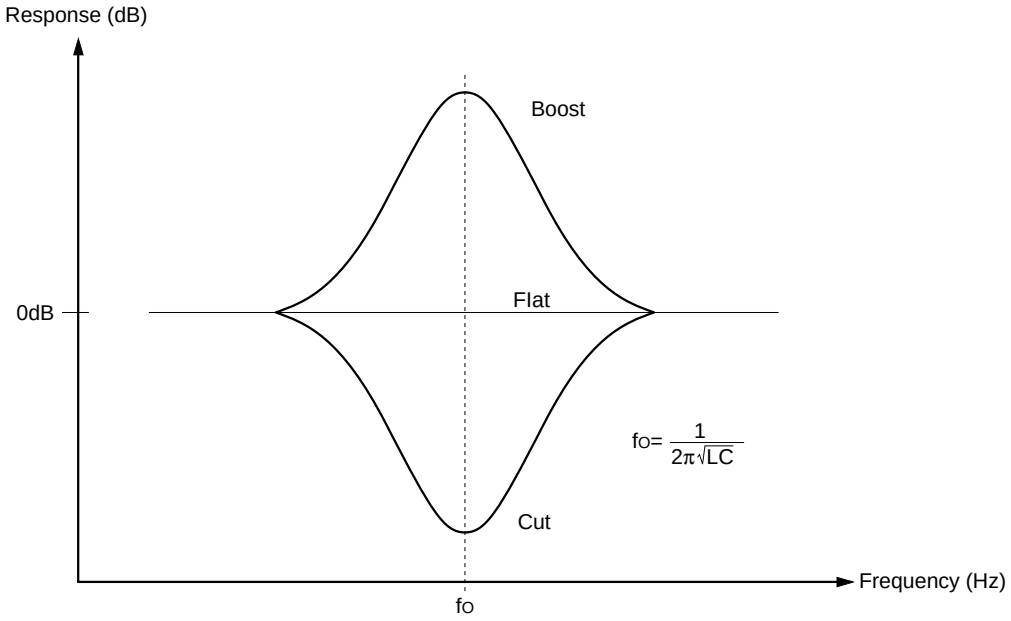


Fig. 2.

• CXA1352AS system

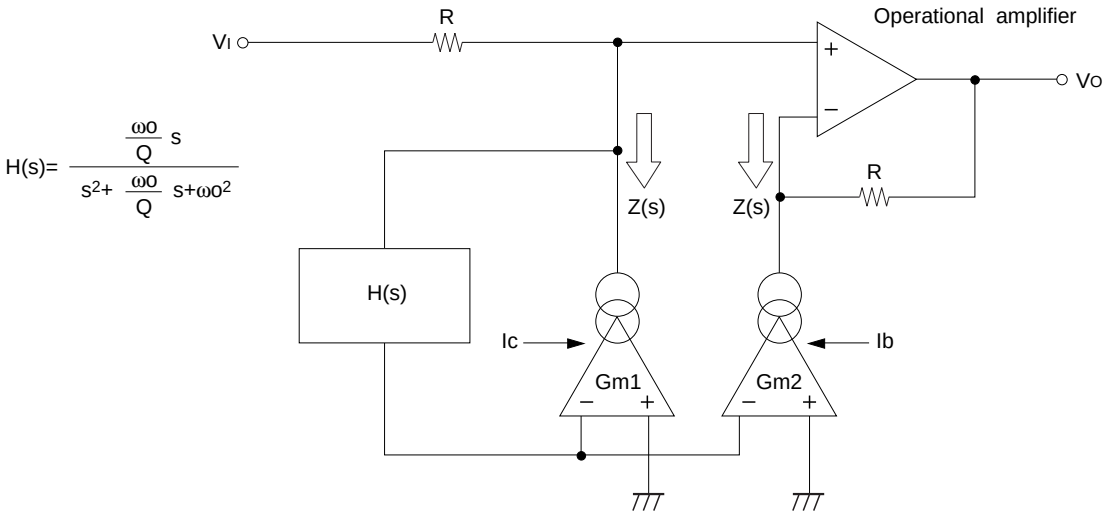


Fig. 3.

The structure of the graphic equalizer used in this IC is shown on Fig. 3. This circuit performs boost and cut controlled by 2 transconductance amplifiers that can vary the conversion coefficient through control currents Ib, and Ic around ωo. ("ωo" is central frequency determined by Band Pass Filter.) Considering output impedance Z (s) of Gm1, Gm2 we have

$$Z(s) = \frac{1}{H(s) \bullet Gm1}$$

Here, using ωo and Q we can express BPF transmittance H (s) as

$$H(s) = \frac{\frac{\omega o}{Q} \cdot s}{s^2 + \frac{\omega o}{Q} s + \omega o^2}$$

$$Z(s) = \frac{Q}{\omega o \cdot Gm1} s + \frac{1}{Gm1} + \frac{\omega o \cdot Q}{Gm1 \cdot s}$$

This formula shows that this system and the aforementioned LCR circuit have equivalent impedance characteristics on Z (s).
Then, regarding Gm as the maximum value of Gm1 and Gm2, the operation can be observed as follows.
Maximum cut occurs when Gm1=Gm and Gm2=0. At that time we have transmittance T (s) as

$$T(s) = \frac{Z(s)}{Z(s)+R} = \frac{s^2 + \frac{\omega o}{Q} \cdot s + \omega o^2}{s^2 + \frac{(1+R \cdot Gm) \cdot \omega o^2}{Q} \cdot s + \omega o^2}$$

This is equal to the frequency characteristics of the conventional graphic equalizer at cut.
Also, maximum boost occurs when Gm1=0 and Gm2=Gm. At that time we have transmittance T (s) as

$$T(s) = \frac{Z(s)+R}{Z(s)} = \frac{s^2 + \frac{(1+R \cdot Gm) \cdot \omega o^2}{Q} \cdot s + \omega o^2}{s^2 + \frac{\omega o}{Q} \cdot s + \omega o^2}$$

This is equal to the frequency characteristics of the conventional graphic equalizer at boost.
We can then deduce that, as far as the operation is concerned the graphic equalizer on this IC and the conventional graphic equalizer are equal, even when the system differs. The merit in using this IC's system rests with the fact that monolithic filter technology realizes a graphic equalizer without external parts.
The structure of the actual graphic equalizer, including BPF, is shown on Fig. 4.

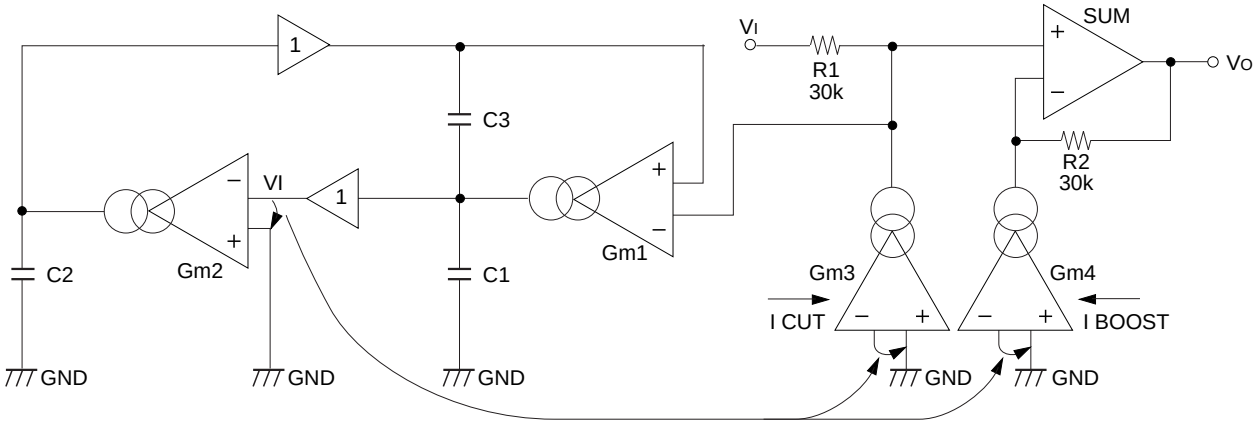


Fig. 4

2. Control through microcomputer possible

Volume, balance and the 100 Hz, 400 Hz, 1 kHz, 4 kHz, 10 kHz boost, cut control respectively are all executed through DC voltage.

Also, the control voltage range is determined through DV_{CC} (control power supply, independent from V_{CC}) and is from 0 V to DV_{CC}. Accordingly, the control range can be varied at will, by changing DV_{CC} voltage. By setting DV_{CC} 5 V, control through the microcomputer becomes possible.

Setting to $DV_{CC}=V_{CC}$ enables usage with single power supply.

3. Pseudo loudness

A loudness function interlocking with volume (VOL) is featured.

With this IC, to provide a loudness effect, the 100 Hz and 10 kHz graphic equalizer part does not use a BPF but is composed of a low pass filter (LPF) and a high pass filter (HPF) respectively.

The operation is explained as follows. As VOL drops below the center, the 100 Hz and 10 kHz graphic equalizer part Ib (See Fig. 3.) gradually increases even if the graphic equalizer control pin (100 Hz and 10 kHz) is flat, boost applies and as a result loudness effect is obtained.

Notes on Operation

1. Power supply

DVCC can be used independently from VCC but supply voltage should be

VCC≥DVCC, without fall.

2. Pseudo loudness

As mentioned in the paragraph on Description of Operation, as it is interlocked with VOL, loudness can not be put OFF.

3. Output pin

This IC features 2 channels for each of OUT pin, LINE OUT pin and FIX OUT pin.

Usage of the respective output pins is indicated as follows.

- OUT pin

  Normally used as the graphic equalizer output.
- LINE OUT pin

  A sound from a source that has not passed through the graphic equalizer is only amplified and output from this pin.
- FIX OUT pin

  This pin is useful for REC or spectrum analyzer display after the sound formation at the graphic equalizer.

  The relation between the input and the respective outputs is shown on Fig. 5.

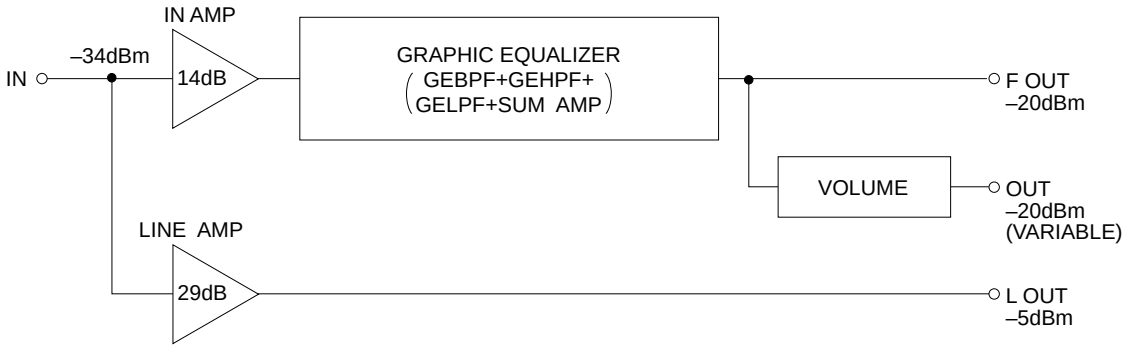


Fig. 5.

4. Reference resistor

To check the central frequency deviation of the graphic equalizer, the control current that determines the filter time constant is determined by means of an external, not an internal, resistor.

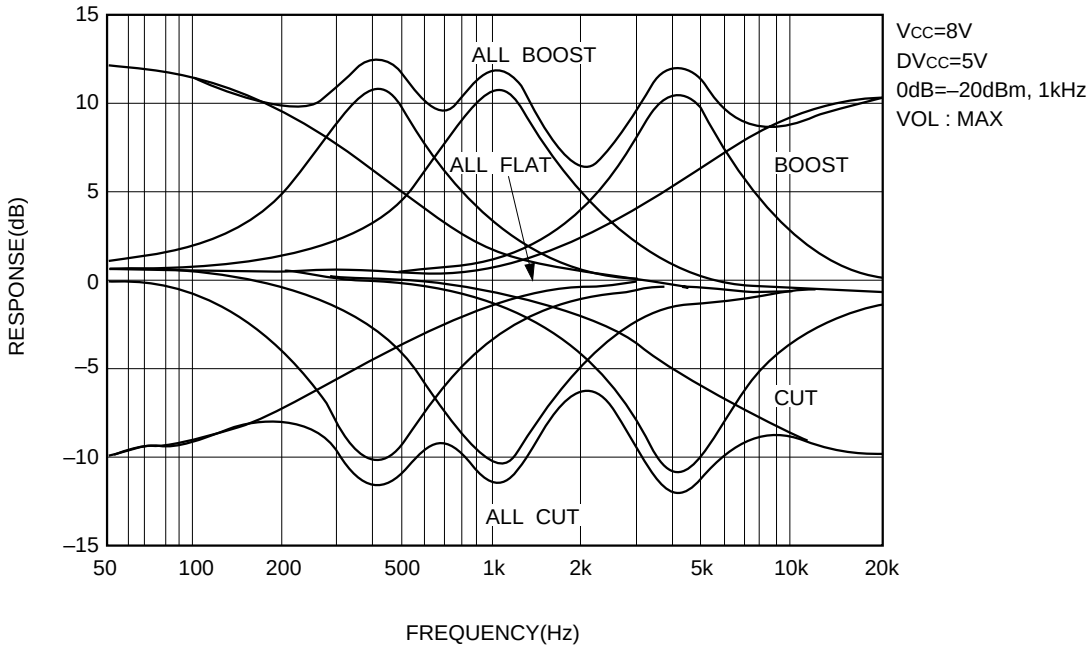
This is the 160 kΩ external resistor connected to ISET pin (Pin 11). Accordingly, for the resistor to be connected to ISET pin, it is recommended to use a resistor with excellent dispersion and temperature characteristics.

Also, by varying the value of the resistor connected to ISET pin, the frequency characteristics of the graphic equalizer can be shifted. By reducing the resistor value the shift moves to the high band and by increasing the value the shift moves to the low band.

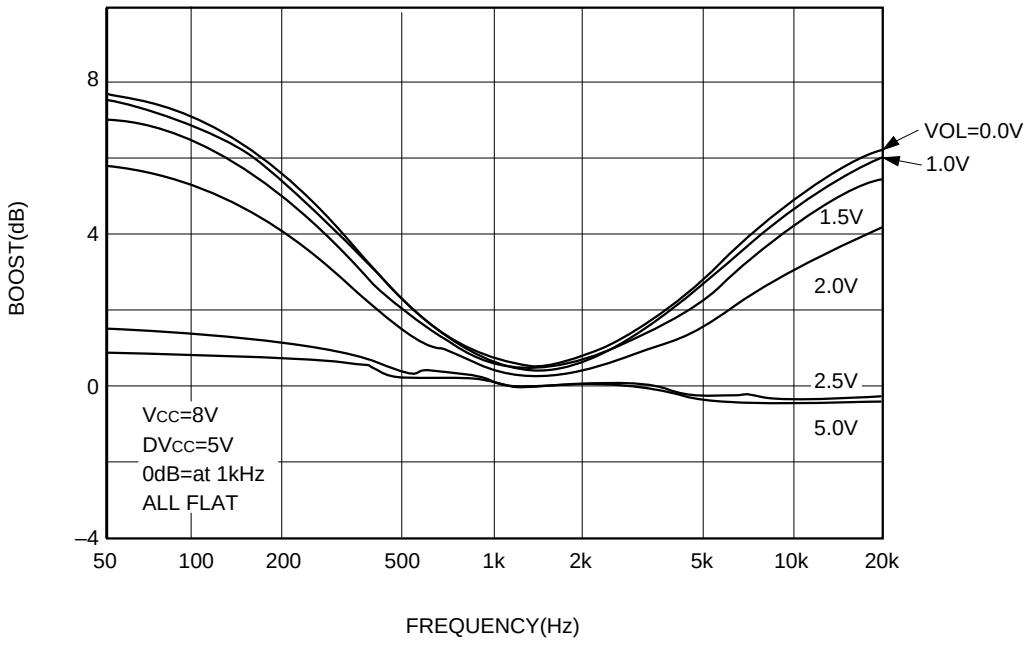
However, 5 elements cannot be shifted independently.

Example of Representative Characteristics

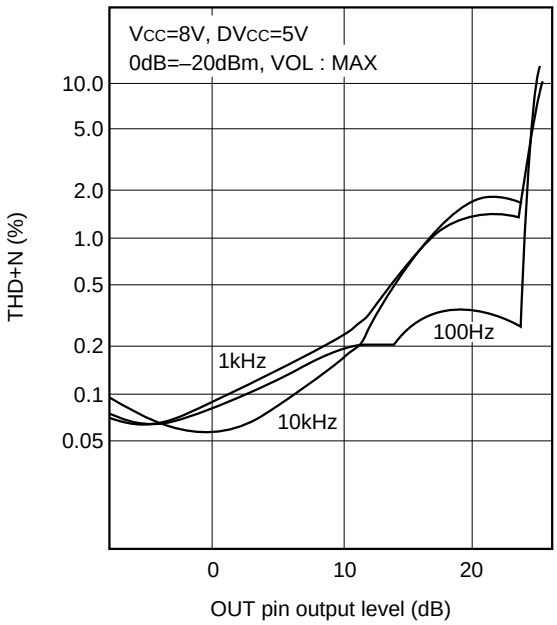
Frequency characterlstlcs



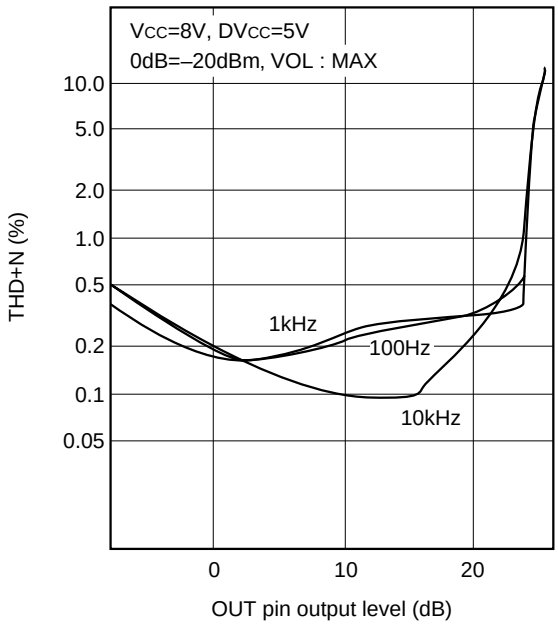
Loudness characteristics



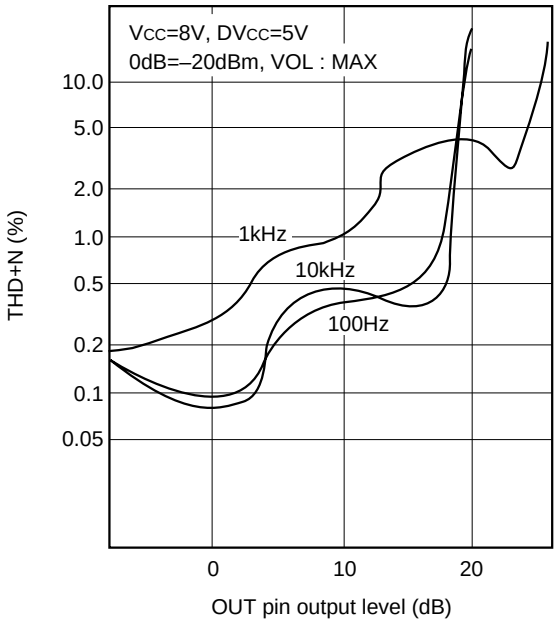
THD-OUT characteristics (ALL FLAT)



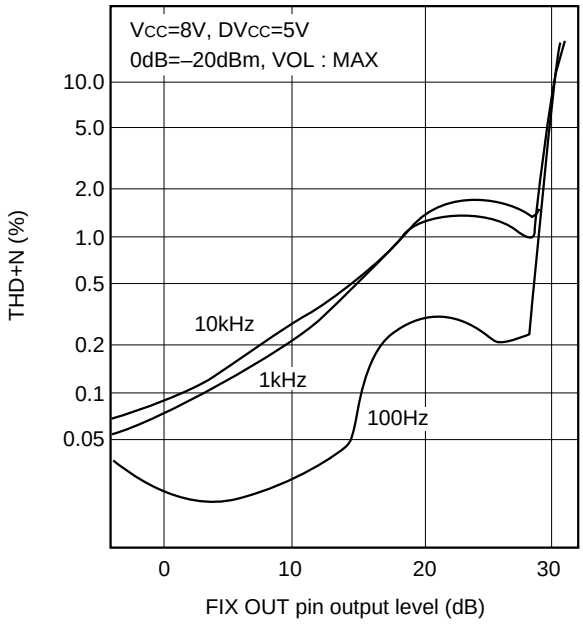
THD-OUT characteristics (ALL BOOST)



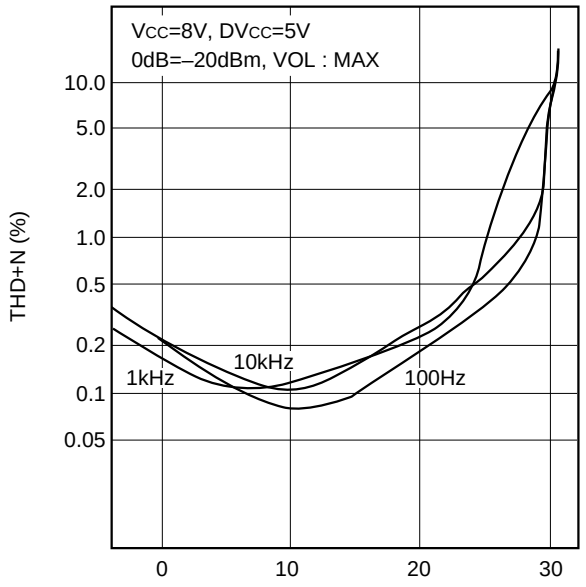
THD-OUT characteristics (ALL CUT)



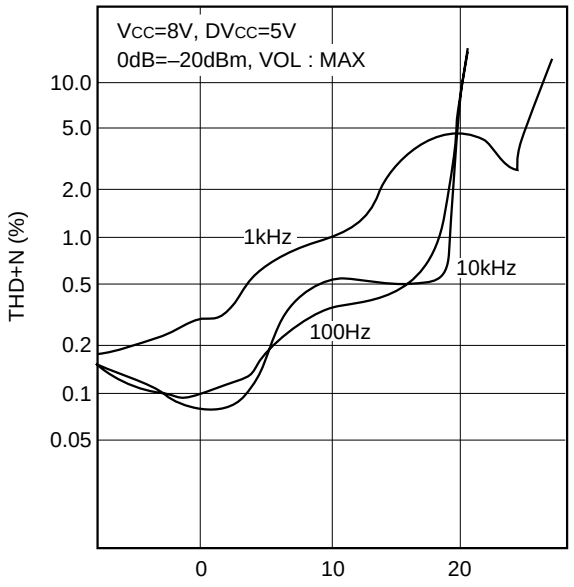
THD-F OUT characteristics (ALL FLAT)



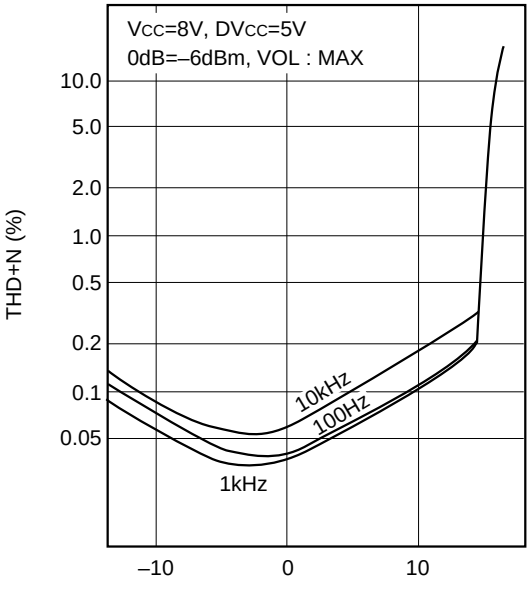
THD-F OUT characteristics (ALL BOOST)



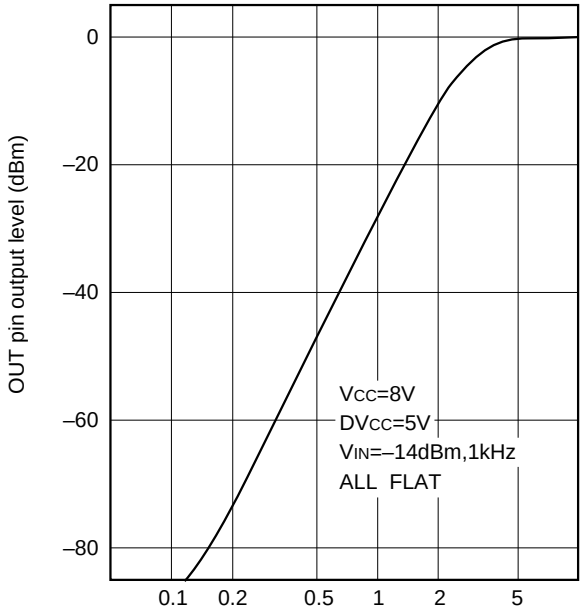
THD-F OUT characteristics (ALL CUT)



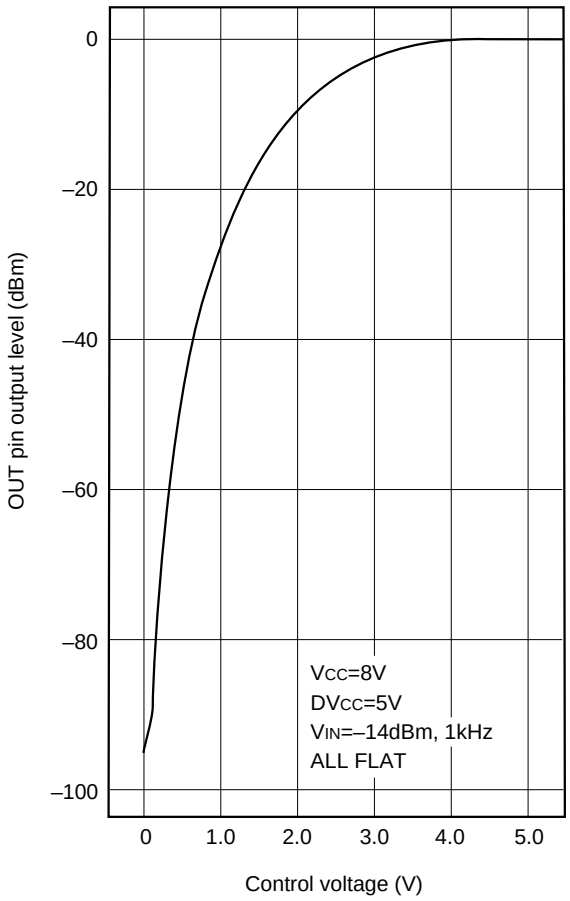
THD-L OUT characteristics



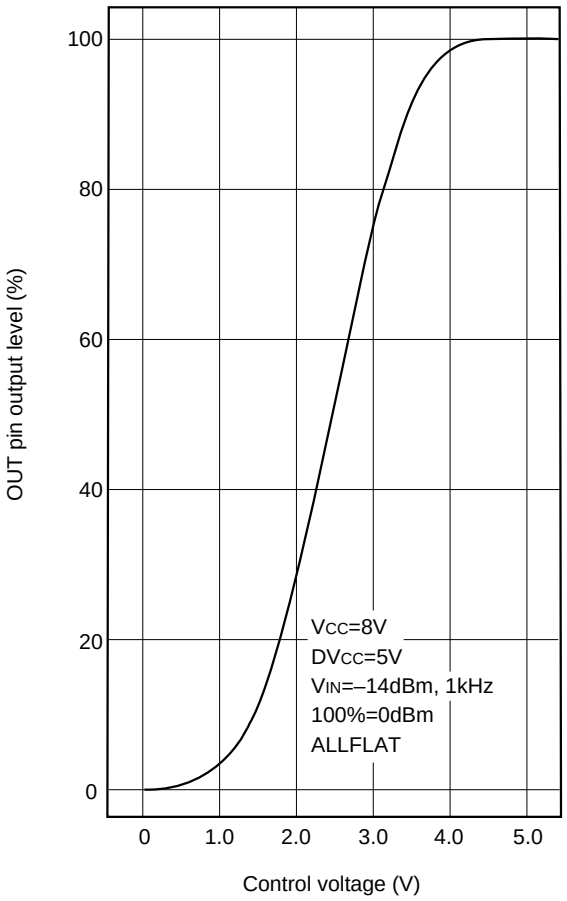
Output voltage vs. Control voltage (VOL)



Output voltage vs. Control voltage (VOL)

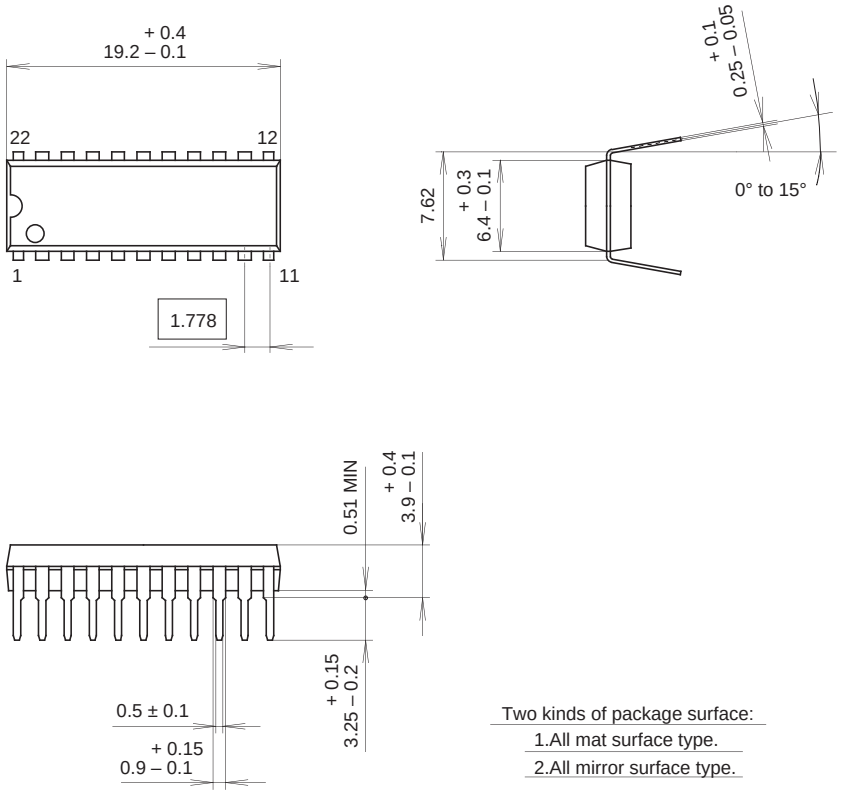


Output voltage vs. Control voltage (VOL)



Package Outline Unit : mm

22PIN SDIP (PLASTIC)



Two kinds of package surface:
1.All mat surface type.
2.All mirror surface type.

PACKAGE STRUCTURE

MOLDING COMPOUND	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.95g

SONY CODE	SDIP-22P-01
EIAJ CODE	SDIP022-P-0300
JEDEC CODE	————