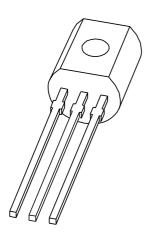
# **DISCRETE SEMICONDUCTORS**

# DATA SHEET



# **BSR52**NPN Darlington transistor

Product specification Supersedes data of 1999 Apr 26 2004 Nov 11





# **NPN Darlington transistor**

**BSR52** 

# **FEATURES**

- High current (max. 1 A)
- Low voltage (max. 80 V)
- Integrated diode and resistor.

# **APPLICATIONS**

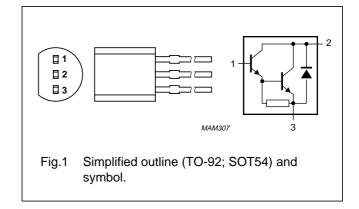
• Industrial high gain amplification.

# **DESCRIPTION**

NPN Darlington transistor in a TO-92; SOT54 plastic package. PNP complement: BSR62.

# **PINNING**

PIN	DESCRIPTION
1	base
2	collector
3	emitter



# **ORDERING INFORMATION**

TYPE NUMBER		PACKAGE				
I TPE NOWIBER	NAME DESCRIPTION VERSION					
BSR52	SC-43A	plastic single-ended leaded (through hole) package; 3 leads				

# **LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>CBO</sub>	collector-base voltage	open emitter	_	90	V
V <sub>CES</sub>	collector-emitter voltage	V <sub>BE</sub> = 0 V	_	80	V
V <sub>EBO</sub>	emitter-base voltage	open collector	_	5	V
I <sub>C</sub>	collector current (DC)		_	1	Α
I <sub>CM</sub>	peak collector current		_	2	А
I <sub>B</sub>	base current (DC)		_	100	mA
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C; note 1	_	830	mW
T <sub>stg</sub>	storage temperature		-65	+150	°C
Tj	junction temperature		_	150	°C
T <sub>amb</sub>	ambient temperature		-65	+150	°C

# Note

1. Transistor mounted on an FR4 printed-circuit board.

# NPN Darlington transistor

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# THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	note 1	150	K/W

# Note

1. Transistor mounted on an FR4 printed-circuit board.

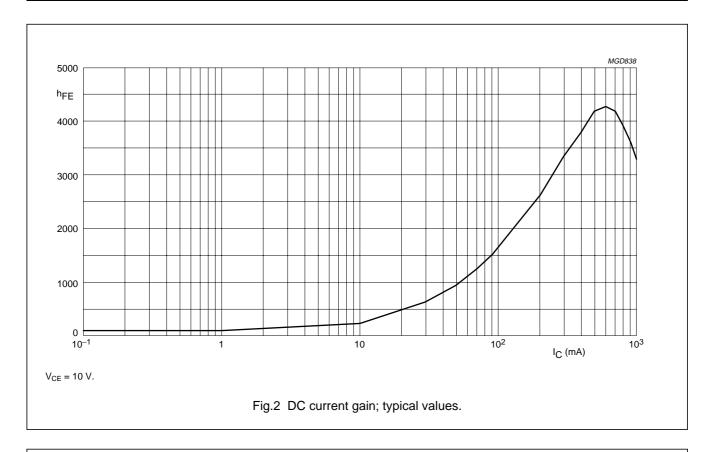
# **CHARACTERISTICS**

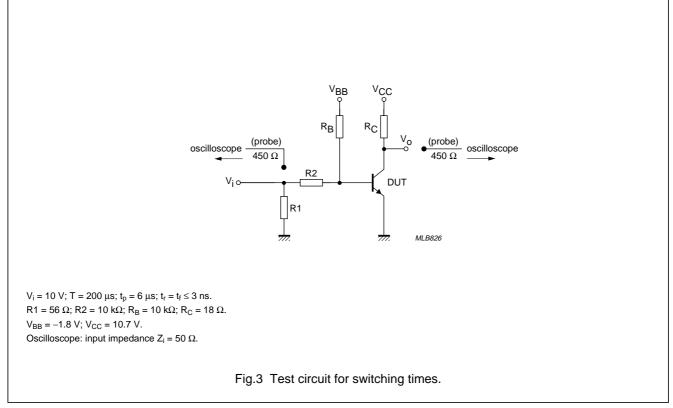
 $T_{amb}$  = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I <sub>CES</sub>	collector-base cut-off current	V <sub>BE</sub> = 0 V; V <sub>CE</sub> = 80 V	_	_	50	nA
I <sub>EBO</sub>	emitter-base cut-off current	V <sub>EB</sub> = 4 V; I <sub>C</sub> = 0 A	_	_	50	nA
h <sub>FE</sub>	DC current gain	V <sub>CE</sub> = 10 V; see Fig.2				
		I <sub>C</sub> = 150 mA	1000	-	-	
		I <sub>C</sub> = 500 mA	2000	-	_	
V <sub>CEsat</sub>	collector-emitter saturation voltage	I <sub>C</sub> = 0.5 A; I <sub>B</sub> = 0.5 mA	_	_	1.3	٧
		I <sub>C</sub> = 1 A; I <sub>B</sub> = 4 mA	_	_	1.6	V
V <sub>BEsat</sub>	base-emitter saturation voltage	I <sub>C</sub> = 0.5 A; I <sub>B</sub> = 0.5 mA	_	_	1.9	V
		I <sub>C</sub> = 1 A; I <sub>B</sub> = 4 mA	_	_	2.2	٧
f <sub>T</sub>	transition frequency	$V_{CE} = 5 \text{ V; } I_{C} = 500 \text{ mA;}$ f = 100 MHz	_	200	_	MHz
Switching t	imes (between 10% and 90% levels	s); see Fig.3				
t <sub>on</sub>	turn-on time	I <sub>Con</sub> = 500 mA; I <sub>Bon</sub> = 0.5 mA;	_	_	500	ns
t <sub>off</sub>	turn-off time	$I_{Boff} = -0.5 \text{ mA}$	_	_	1300	ns

# NPN Darlington transistor

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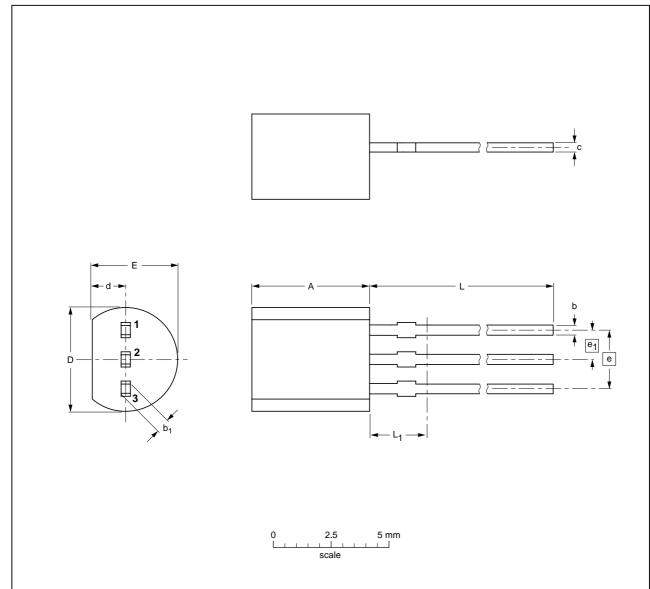
# NPN Darlington transistor

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# **PACKAGE OUTLINE**

# Plastic single-ended leaded (through hole) package; 3 leads

SOT54



# DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b <sub>1</sub>	С	D	d	E	е	e <sub>1</sub>	L	L <sub>1</sub> <sup>(1)</sup> max.	
mm	5.2 5.0	0.48 0.40	0.66 0.55	0.45 0.38	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5	

### Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE		REFER	ENCES	EUROPEAN	ISSUE DATE	
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT54		TO-92	SC-43A			<del>97-02-28</del> 04-06-28

# NPN Darlington transistor

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LEVEL	DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS(2)(3)	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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