CURRENT MODE PWM CONTROLLER

FEATURES

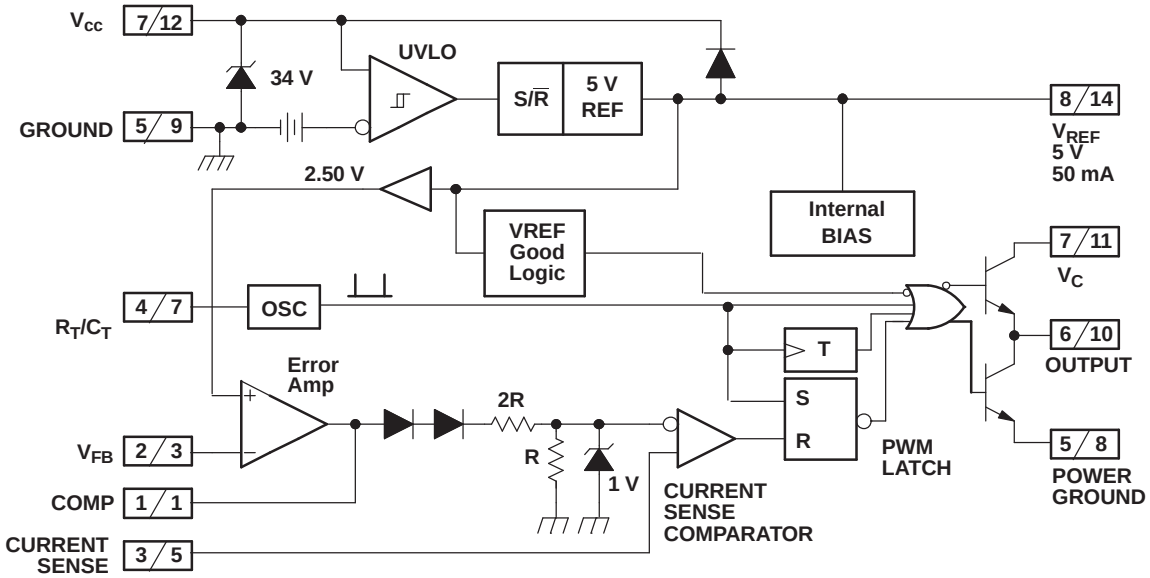
- **Optimized For Off-line and DC-to-DC Converters**
- **Low Start-Up Current (<1 mA)**
- **Automatic Feed Forward Compensation**
- **Pulse-by-Pulse Current Limiting**
- **Enhanced Load Response Characteristics**
- **Under-Voltage Lockout With Hysteresis**
- **Double Pulse Suppression**
- **High Current Totem Pole Output**
- **Internally Trimmed Bandgap Reference**
- **500-kHz Operation**
- **Low R_O Error Amp**

DESCRIPTION

The UC1842/3/4/5 family of control devices provides the necessary features to implement off-line or dc-to-dc fixed frequency current mode control schemes with a minimal external parts count. Internally implemented circuits include under-voltage lockout featuring start up current less than 1 mA, a precision reference trimmed for accuracy at the error amp input, logic to insure latched operation, a PWM comparator which also provides current limit control, and a totem pole output stage designed to source or sink high peak current. The output stage, suitable for driving N-Channel MOSFETs, is low in the off state.

Differences between members of this family are the under-voltage lockout thresholds and maximum duty cycle ranges. The UC1842 and UC1844 have UVLO thresholds of 16 V_{ON} and 10 V_{OFF}, ideally suited to off-line applications. The corresponding thresholds for the UC1843 and UC1845 are 8.4 V and 7.6 V. The UC1842 and UC1843 can operate to duty cycles approaching 100%. A range of zero to 50% is obtained by the UC1844 and UC1845 by the addition of an internal toggle flip flop which blanks the output off every other clock cycle.

BLOCK DIAGRAM



Note 1: A/B A = DIL−8 Pin Number. B = SO−14 and CFP−14 Pin Number.
Note 2: Toggle flip flop used only in 1844 and 1845.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

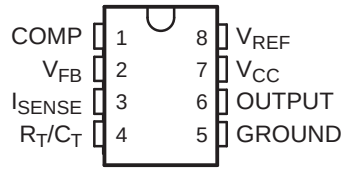
ABSOLUTE MAXIMUM RATINGS(1)

		UNIT
Supply voltage	Low impedance source	30 V
	I_{CC} < 30 mA	Self Limiting
Output current		±1 A
Output energy (capacitive load)		5 µJ
Analog inputs (Pins 2, 3)		–0.3 V to 6.3 V
Error amp output sink current		10 mA
Power dissipation	T_A≤ 25°C (DIL-8)	1 W
	T_A≤ 25°C (SOIC-14)	725 mW
	T_A≤ 25°C (SOIC-8)	650 mW
Storage temperature range		–65°C to 150°C
Junction temperature range		–55°C to 150°C
Lead temperature (soldering, 10 seconds)		300°C

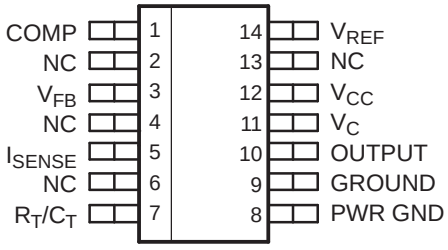
(1) All voltages are with respect to Pin 5. All currents are positive into the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAMS

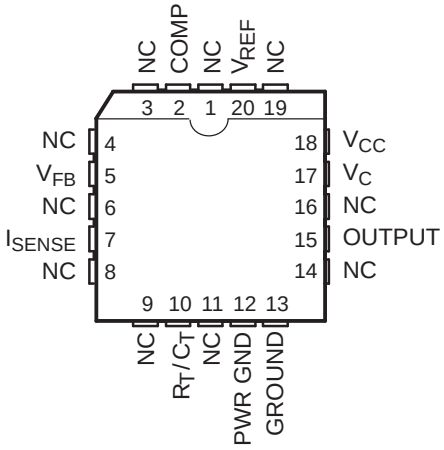
DIL-8, SOIC-8
N or J PACKAGE, D8 PACKAGE
(TOP VIEW)



SOIC-14, CFP-14
D or W PACKAGE
(TOP VIEW)



PLCC-20
Q PACKAGE
(TOP VIEW)



NC − No internal connection

THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PACKAGE		θ_{JC}	θ_{JA}
DIL-8	J	28(1)	125-160
	N	25	110(2)
SOIC-8	D8	42	84-160(2)
SOIC-14	D14	35	50-120(2)
CFP-14	W	5.49°C/W	175.4C/W
PLCC-20	Q	34	43-75(2)

(1) θ_{JC} data values stated were derived from MIL-STD-1835B.
(2) Specified θ_{JA} (junction to ambient) is for devices mounted to 5 in^2 FR4 PC board with one ounce copper where noted. When resistance range is given, lower values are for 5 in^2. Test PWB was 0.062 in thick and typically used 0.635-mm trace widths for power packages and 1.3-mm trace widths for non-power packages with 100 x 100-mil probe land area at the end of each trace.

DISSIPATION RATINGS

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A \leq 25°C$	$T_A \leq 70°C$ POWER RATING	$T_A \leq 85°C$PO WER RATING	$T_A \leq 125°C$ POWER RATING
W	700 mW	5.5 mW/°C	452 mW	370 mW	150 mW

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for $–55°C \leq T_A \leq 125°C$ for the UC184X; $–40°C \leq T_A \leq 85°C$ for the UC284X; $0°C \leq T_A \leq 70°C$ for the 384X; V_{CC} = 15 V(1); R_T = 10 kΩ; C_T = 3.3 nF, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	UC1842/3/4/5 UC2842/3/4/5			UC3842/3/4/5			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
REFERENCE SECTION								
Output Voltage	T_J = 25°C, I_O = 1 mA	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation	$12 \leq V_{IN} \leq 25$ V		6	20		6	20	mV
Load Regulation	$1 \leq I_0 \leq 20$ mA		6	25		6	25	
Temp. Stability	See (2)(3)		0.2	0.4		0.2	0.4	mV/°C
Total Output Variation	Line, load, tempature (2)	4.9		5.1	4.82		5.18	V
Output Noise Voltage	10 Hz≤ f ≤ 10 kHz, T_J = 25°C(2)		50			50		μV
Long Term Stability	T_A = 125°C, 1000 Hrs(2)		5	25		5	25	mV
Output Short Circuit		–30	–100	–180	–30	–100	–180	mA
OSCILLATOR SECTION								
Initial Accuracy	T_J = 25°C(4)	47	52	57	47	52	57	kHz
Voltage Stability	$12 \leq V_{CC} \leq 25$ V		0.2%	1%		0.2%	1%	
Temp. Stability	$T_{MIN} \leq T_A \leq T_{MAX}$(2)		5%			5%		
Amplitude	V_{PIN} 4 peak-to-peak (2)		1.7			1.7		V

(1) Adjust V_{CC} above the start threshold before setting at 15 V.
(2) These parameters, although specified, are not 100% tested in production.
(3) Temperature stability, sometimes referred to as average temperature coefficient, is described by the equation:

$$\text{Temp Stability} = \frac{V_{REF}(\text{max}) - \text{VREF (min)}}{\text{TJ(max)} - \text{TJ (min)}}$$

$V_{REF(max)}$ and $V_{REF(min)}$ are the maximum and minimum reference voltages measured over the appropriate temperature range. Note that the extremes in voltage do not necessarily occur at the extremes in temperature.
(4) Output frequency equals oscillator frequency for the UC1842 and UC1843.
Output frequency is one half oscillator frequency for the UC1844 and UC1845.

ELECTRICAL CHARACTERISTICS (continued)

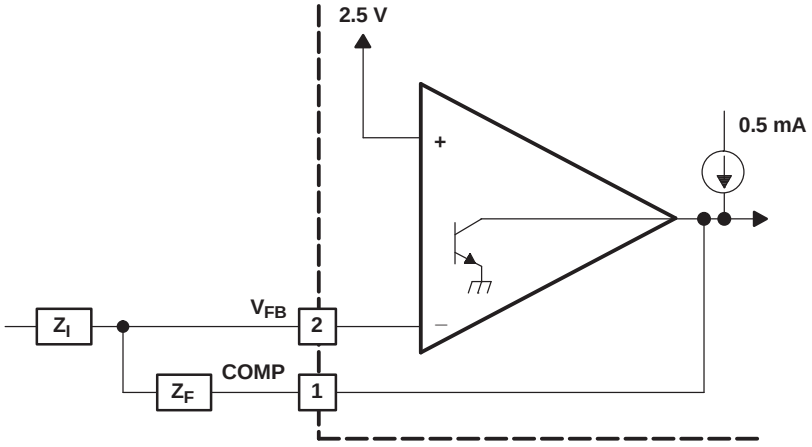
Unless otherwise stated, these specifications apply for –55°C ≤ T_A ≤ 125°C for the UC184X; –40°C ≤ T_A ≤ 85°C for the UC284X; 0°C ≤ T_A ≤ 70°C for the 384X; V_{CC} = 15 V; R_T = 10 kΩ; C_T = 3.3 nF, T_A = T_J.

PARAMETER	TEST CONDITIONS	UC1842/3/4/5 UC2842/3/4/5			UC3842/3/4/5			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
ERROR AMP SECTION								
Input Voltage	$V_{PIN\ 1}$ = 2.5 V	2.45	2.50	2.55	2.42	2.50	2.58	V
Input Bias Current			–0.3	–1		–0.3	–2	µA
A_{VOL}	2 ≤ V_O ≤ 4 V	65	90		65	90		dB
Unity Gain Bandwidth	T_J = 25°C (5)	0.7	1		0.7	1		MHz
PSRR	12 ≤ V_{CC} ≤ 25 V	60	70		60	70		dB
Output Sink Current	$V_{PIN\ 2}$ = 2.7 V, $V_{PIN\ 1}$ = 1.1 V	2	6		2	6		mA
Output Source Current	$V_{PIN\ 2}$ = 2.3 V, $V_{PIN\ 1}$ = 5 V	–0.5	–0.8		–0.5	–0.8		
V_{OUT} High	$V_{PIN\ 2}$ = 2.3 V, R_L = 15 kΩ to ground	5	6		5	6		V
V_{OUT} Low	$V_{PIN\ 2}$ = 2.7 V, R_L = 15 kΩ to Pin 8		0.7	1.1		0.7	1.1	
CURRENT SENSE SECTION								
Gain	See (6)(7)	2.85	3	3.15	2.85	3	3.15	V/V
Maximum Input Signal	$V_{PIN\ 1}$ = 5 V (6)	0.9	1	1.1	0.9	1	1.1	V
PSRR	12 ≤ V_{CC} ≤ 25 V (5)(6)		70			70		dB
Input Bias Current			–2	–10		–2	–10	µA
Delay to Output	$V_{PIN\ 3}$ = 0 V to 2 V (5)		150	300		150	300	ns
OUTPUT SECTION								
Output Low Level	I_{SINK} = 20 mA		0.1	0.4		0.1	0.4	V
	I_{SINK} = 200 mA		1.5	2.2		1.5	2.2	
Output High Level	I_{SOURCE} = 20 mA	13	13.5		13	13.5		
	I_{SOURCE} = 200 mA	12	13.5		12	13.5		
Rise Time	T_J = 25°C, C_L = 1 nF (5)		50	150		50	150	ns
Fall Time	T_J = 25°C, C_L = 1nF (5)		50	150		50	150	
UNDER-VOLTAGE LOCKOUT SECTION								
Start Threshold	X842/4	15	16	17	14.5	16	17.5	V
	X843/5	7.8	8.4	9.0	7.8	8.4	9.0	
Min. Operating Voltage After Turn On	X842/4	9	10	11	8.5	10	11.5	
	X843/5	7.0	7.6	8.2	7.0	7.6	8.2	
PWM SECTION								
Maximum Duty Cycle	X842/3	95%	97%	100%	95%	97%	100%	
	X844/5	46%	48%	50%	47%	48%	50%	
Minimum Duty Cycle				0%			0%	
TOTAL STANDBY CURRENT								
Start-Up Current			0.5	1		0.5	1	mA
Operating Supply Current	$V_{PIN\ 2}$ = $V_{PIN\ 3}$ = 0 V		11	17		11	17	
V_{CC} Zener Voltager	I_{CC} = 25 mA	30	34		30	34		V

(5) These parameters, although specified, are not 100% tested in production.
(6) Parameter measured at trip point of latch with $V_{PIN\ 2}$ = 0.
(7) Gain defined as: $A = \frac{\Delta VPIN\ 1}{\Delta VPIN\ 3},\ 0 \le VPIN\ 3 \le 0.8\ V$

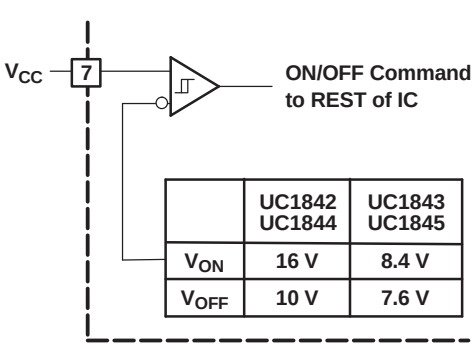
ERROR AMP CONFIGURATION

Error amp can source or sink up to 0.5 mA.

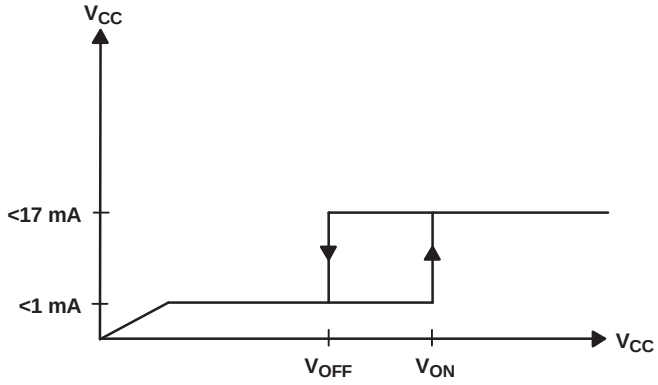


UNDER-VOLTAGE LOCKOUT

During under-voltage lock-out, the output drive is biased to sink minor amounts of current. Pin 6 should be shunted to ground with a bleeder resistor to prevent activating the power switch with extraneous leakage currents.

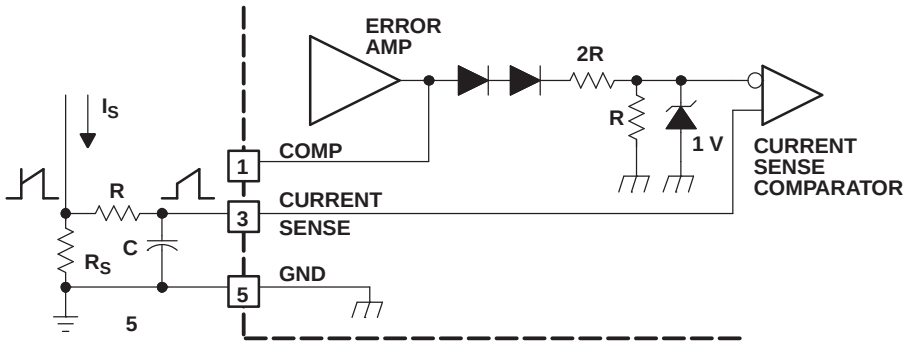


	UC1842 UC1844	UC1843 UC1845
V_{ON}	16 V	8.4 V
V_{OFF}	10 V	7.6 V



CURRENT SENSE CIRCUIT

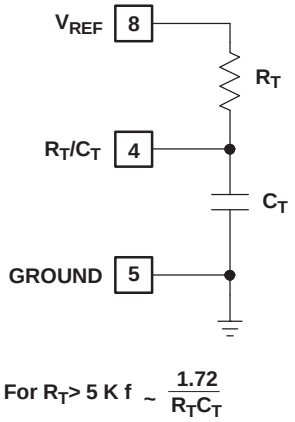
A small RC filter may be required to suppress switch transients.



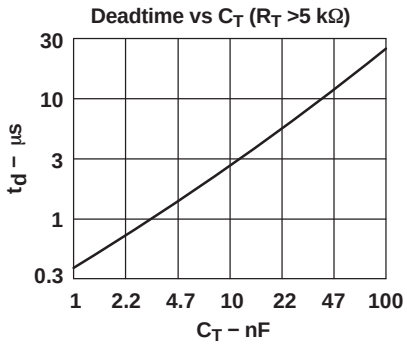
Peak Current (I_S) is Determined By The Formula

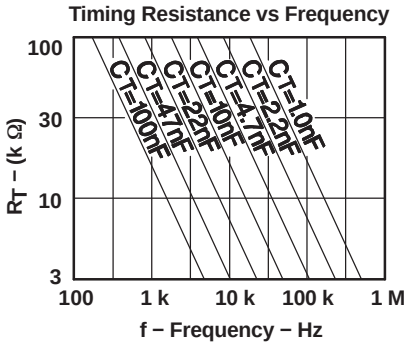
$$I_{SMAX} \approx \frac{1.0\ V}{RS}$$

OSCILLATOR SECTION

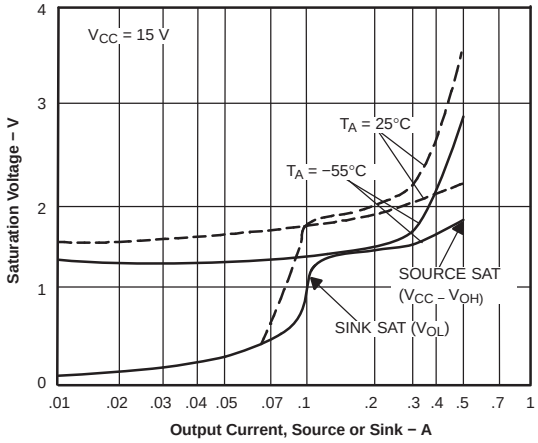


For $R_T > 5\ K\ f \sim \frac{1.72}{R_T C_T}$

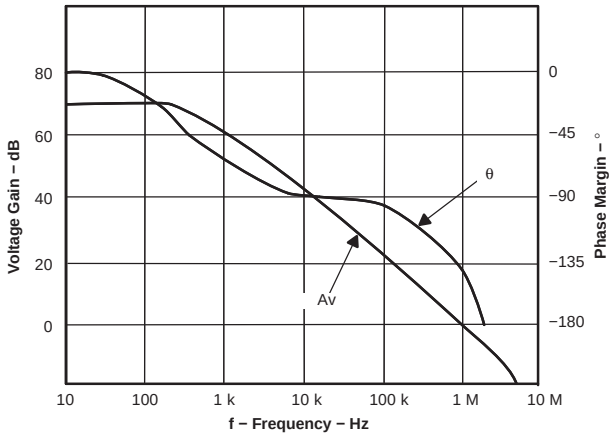




OUTPUT SATURATION CHARACTERISTICS

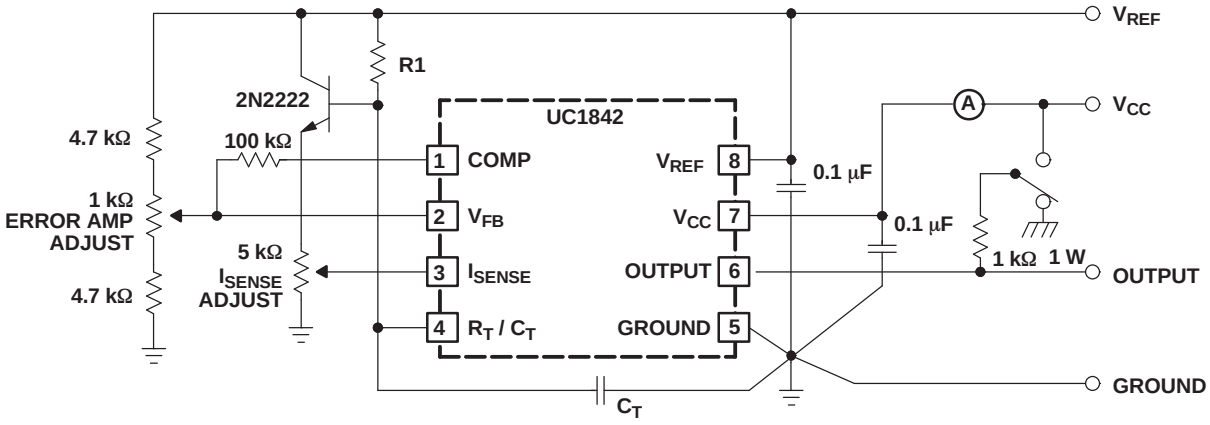


ERROR AMPLIFIER OPEN-LOOP FREQUENCY RESPONSE



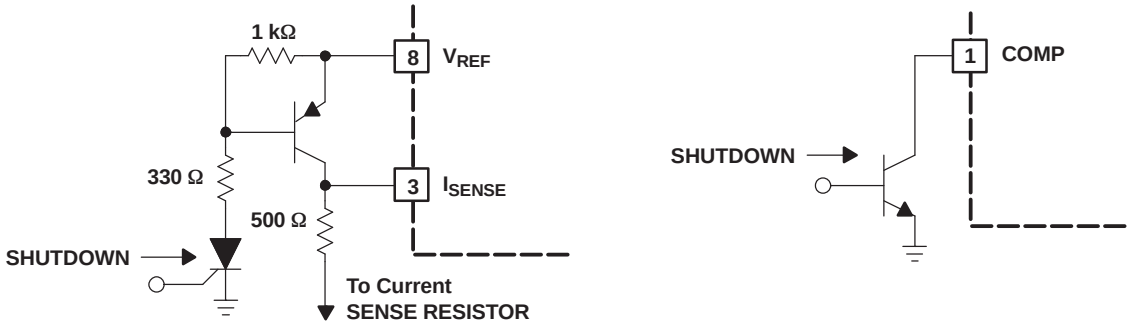
OPEN-LOOP LABORATORY FIXTURE

High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypas capacitors should be conected close to pin 5 in a single point ground. The transistor and 5k potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

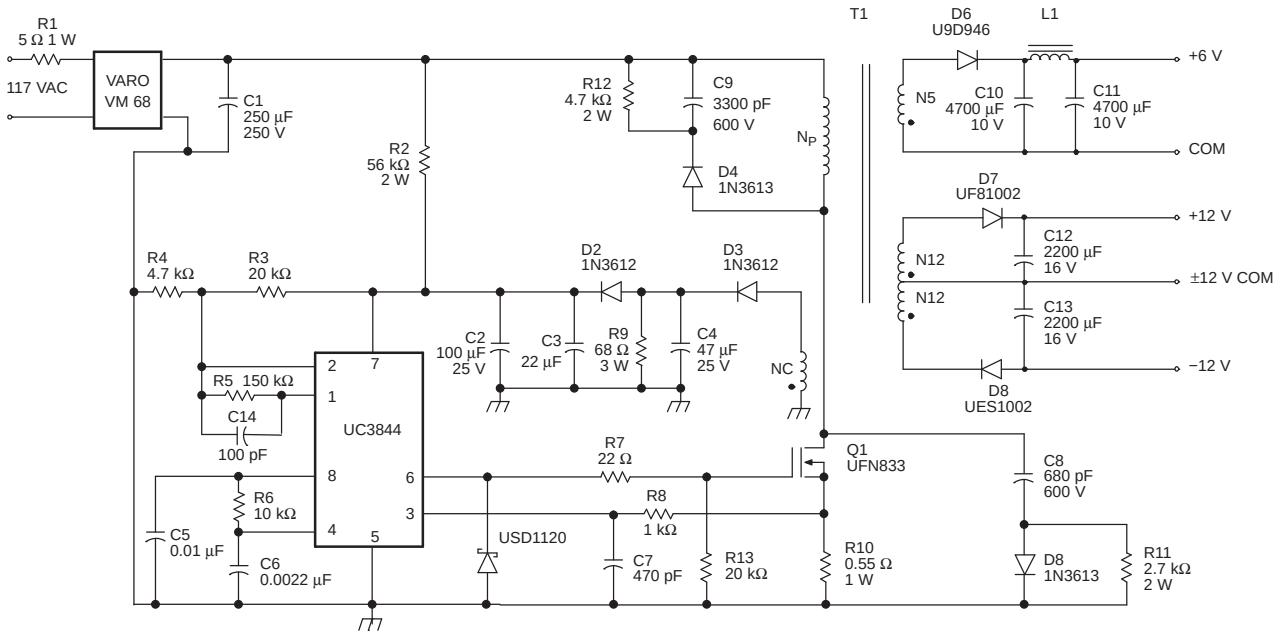


SHUTDOWN TECHNIQUES

Shutdown of the UC1842 can be accomplished by two methods; either raise pin 3 above 1 V or pull pin 1 below a voltage two diode drops above ground. Either method causses the output of the PWM comparator to be high (refer to block diagram). The PWM latch is reset dominant so that the output will remain low until the next clock cycle after the shutdown condition at pin 1 and/or 3 is removed. In one example, an externally latched shutdown may be accomplished by adding an SCR which will be reset by cycling V_{CC} below the lower UVLO threshold. At this pint the reference turns off, allowing the SCR to reset.



OFFLINE FLYBACK REGULATOR



Power Supply Specifications

1. Input Voltages

a. 5VAC to 130VA (50 Hz/60 Hz)

2. Line Isolation: 3750 V
3. Switchng Frequency: 40 kHz
4. Efficiency at Full Load 70%
5. Output Voltage:

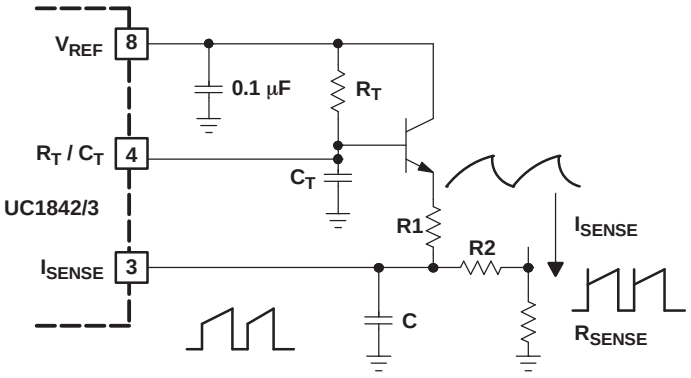
a. +5 V, ±5%; 1A to 4A load
Ripple voltage: 50 mV P-P Max

b. +12 V, ±3%; 0.1A to 0.3A load
Ripple voltage: 100 mV P-P Max

c. –12 V, ±3%; 0.1A to 0.3A load
Ripple voltage: 100 mV P-P Max

SLOPE COMPENSATION

A fraction of the oscillator ramp can be resistively summed with the current sense signal to provide slope compensation for converters requiring duty cycles over 50%.



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
5962-8670401PA	ACTIVE	CDIP	JG	8	1	TBD	Call TI	Call TI	
5962-8670401XA	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
5962-8670402PA	ACTIVE	CDIP	JG	8	1	TBD	Call TI	Call TI	
5962-8670402XA	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
5962-8670403PA	ACTIVE	CDIP	JG	8	1	TBD	Call TI	Call TI	
5962-8670403XA	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
5962-8670404DA	ACTIVE	CFP	W	14	1	TBD	Call TI	Call TI	
5962-8670404PA	ACTIVE	CDIP	JG	8	1	TBD	Call TI	Call TI	
5962-8670404XA	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
UC1842J	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	
UC1842J883B	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	
UC1842L883B	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
UC1842W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	
UC1843J	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	
UC1843J883B	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	
UC1843L	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
UC1843L883B	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
UC1843W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	
UC1844J	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	
UC1844J883B	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	
UC1844L883B	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
UC1845J	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	
UC1845J883B	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	
UC1845L	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
UC1845L883B	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
UC1845W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	
UC1845W883B	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	
UC2842D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
UC2842D8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2842D8G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2842D8TR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2842D8TRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2842DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2842DTR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2842DTRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2842J	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI	
UC2842N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UC2842NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UC2843D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2843D8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2843D8G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2843D8TR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2843D8TRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2843DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2843DTR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2843DTRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2843J	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
UC2843N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UC2843NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UC2844D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2844D8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2844D8G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2844D8TR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2844D8TRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2844DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2844DTR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2844DTRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2844N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UC2844NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UC2845D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2845D8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2845D8G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2845D8TR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2845D8TRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2845DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
UC2845DTR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2845DTRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2845J	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI	
UC2845N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UC2845NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UC3842D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC3842D8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC3842D8G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC3842D8TR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC3842D8TRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC3842DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC3842DTR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC3842DTRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC3842N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UC3842NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UC3843D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC3843D8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC3843D8G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
UC3843D8TR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC3843D8TRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC3843DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC3843DTR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC3843DTRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC3843N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UC3843NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UC3843QTR	OBSOLETE	PLCC	FN	20		TBD	Call TI	Call TI	
UC3844D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC3844D8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC3844D8G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC3844D8TR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC3844D8TRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC3844DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC3844DTR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC3844DTRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC3844N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UC3844NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UC3845AJ	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
UC3845D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC3845D8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC3845D8G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC3845D8TR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC3845D8TRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC3845DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC3845DTR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC3845DTRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC3845N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UC3845NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

OTHER QUALIFIED VERSIONS OF UC1842, UC1843, UC1844, UC1845, UC3842, UC3843, UC3844, UC3845, UC3845AM :

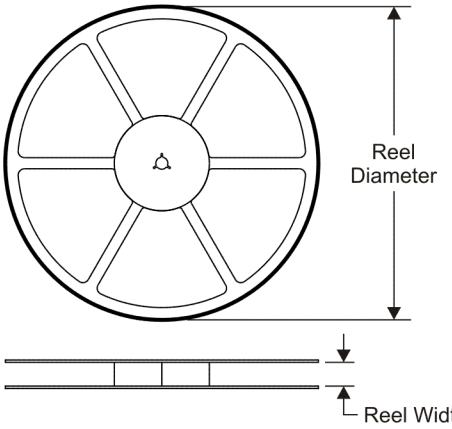
- Catalog: UC3842, UC3843, UC3844, UC3845, UC3842M, UC3845A
- Military: UC1842, UC1843, UC1844, UC1845
- Space: UC1842-SP, UC1843-SP, UC1844-SP, UC1845-SP

NOTE: Qualified Version Definitions:

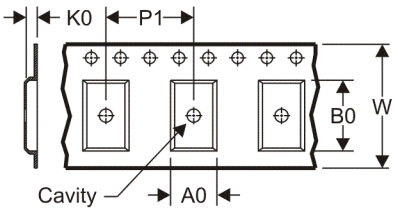
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

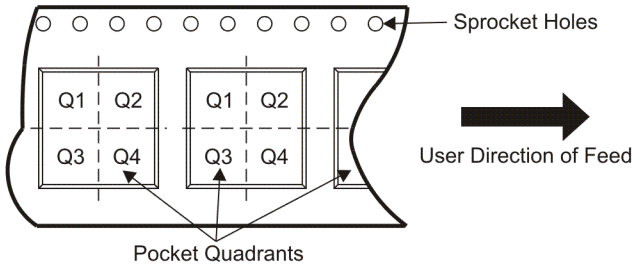


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

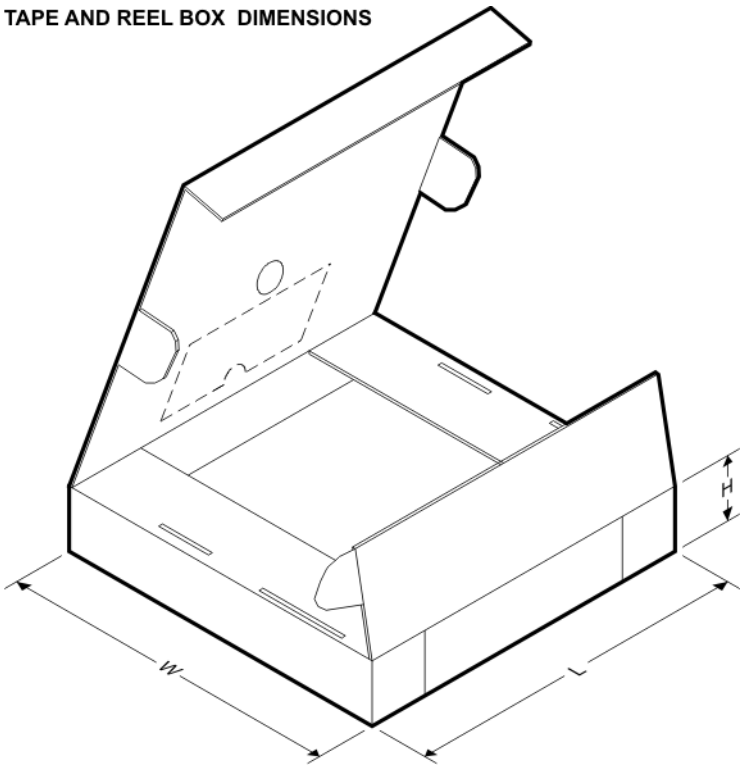
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC2842D8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC2842DTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UC2843D8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC2843DTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UC2844D8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC2844DTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UC2845D8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC2845DTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UC3842D8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC3842DTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UC3843D8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC3843DTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UC3844D8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC3844DTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UC3845D8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC3845DTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

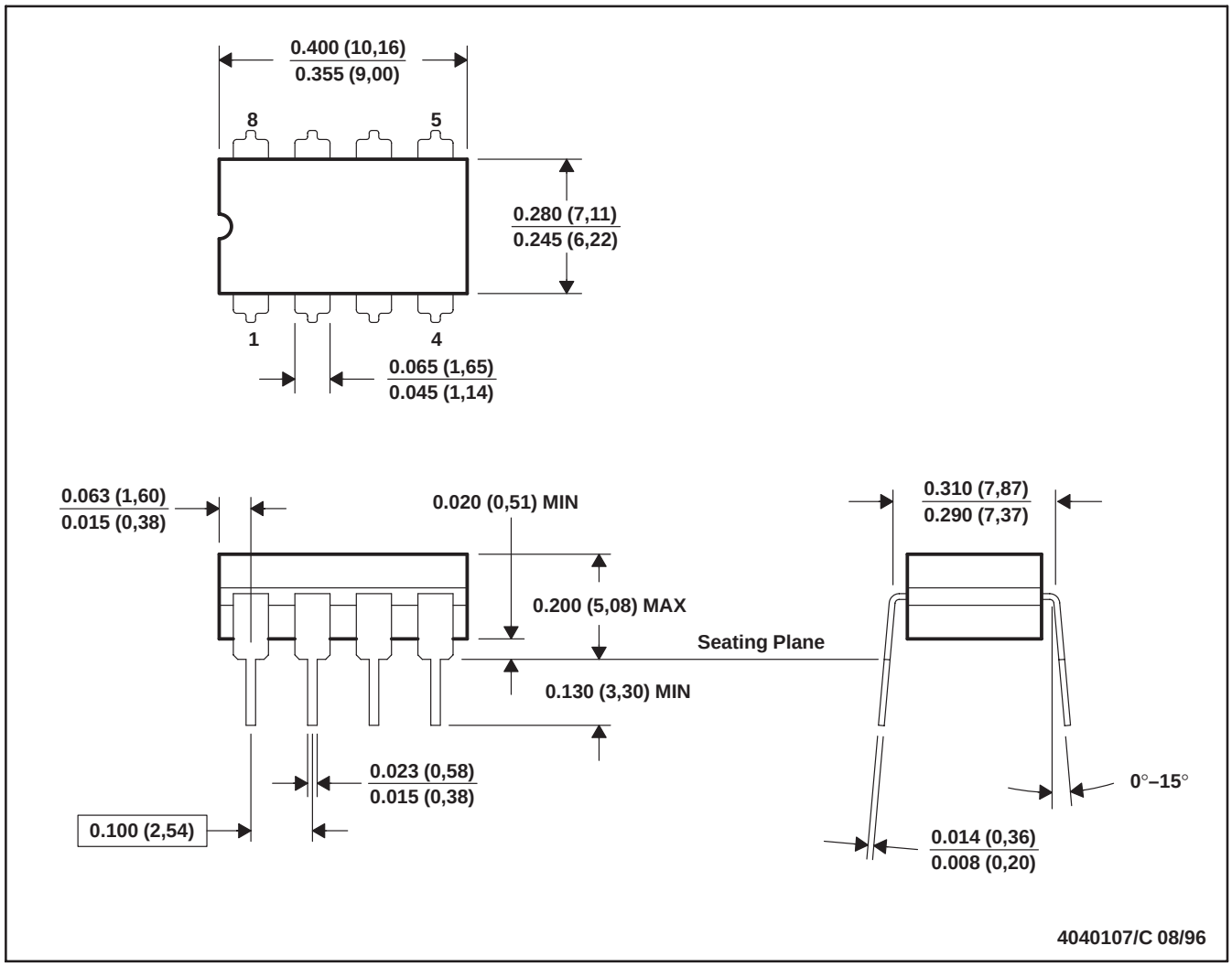


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC2842D8TR	SOIC	D	8	2500	340.5	338.1	20.6
UC2842DTR	SOIC	D	14	2500	333.2	345.9	28.6
UC2843D8TR	SOIC	D	8	2500	340.5	338.1	20.6
UC2843DTR	SOIC	D	14	2500	333.2	345.9	28.6
UC2844D8TR	SOIC	D	8	2500	340.5	338.1	20.6
UC2844DTR	SOIC	D	14	2500	333.2	345.9	28.6
UC2845D8TR	SOIC	D	8	2500	340.5	338.1	20.6
UC2845DTR	SOIC	D	14	2500	333.2	345.9	28.6
UC3842D8TR	SOIC	D	8	2500	340.5	338.1	20.6
UC3842DTR	SOIC	D	14	2500	333.2	345.9	28.6
UC3843D8TR	SOIC	D	8	2500	340.5	338.1	20.6
UC3843DTR	SOIC	D	14	2500	333.2	345.9	28.6
UC3844D8TR	SOIC	D	8	2500	340.5	338.1	20.6
UC3844DTR	SOIC	D	14	2500	333.2	345.9	28.6
UC3845D8TR	SOIC	D	8	2500	340.5	338.1	20.6
UC3845DTR	SOIC	D	14	2500	333.2	345.9	28.6

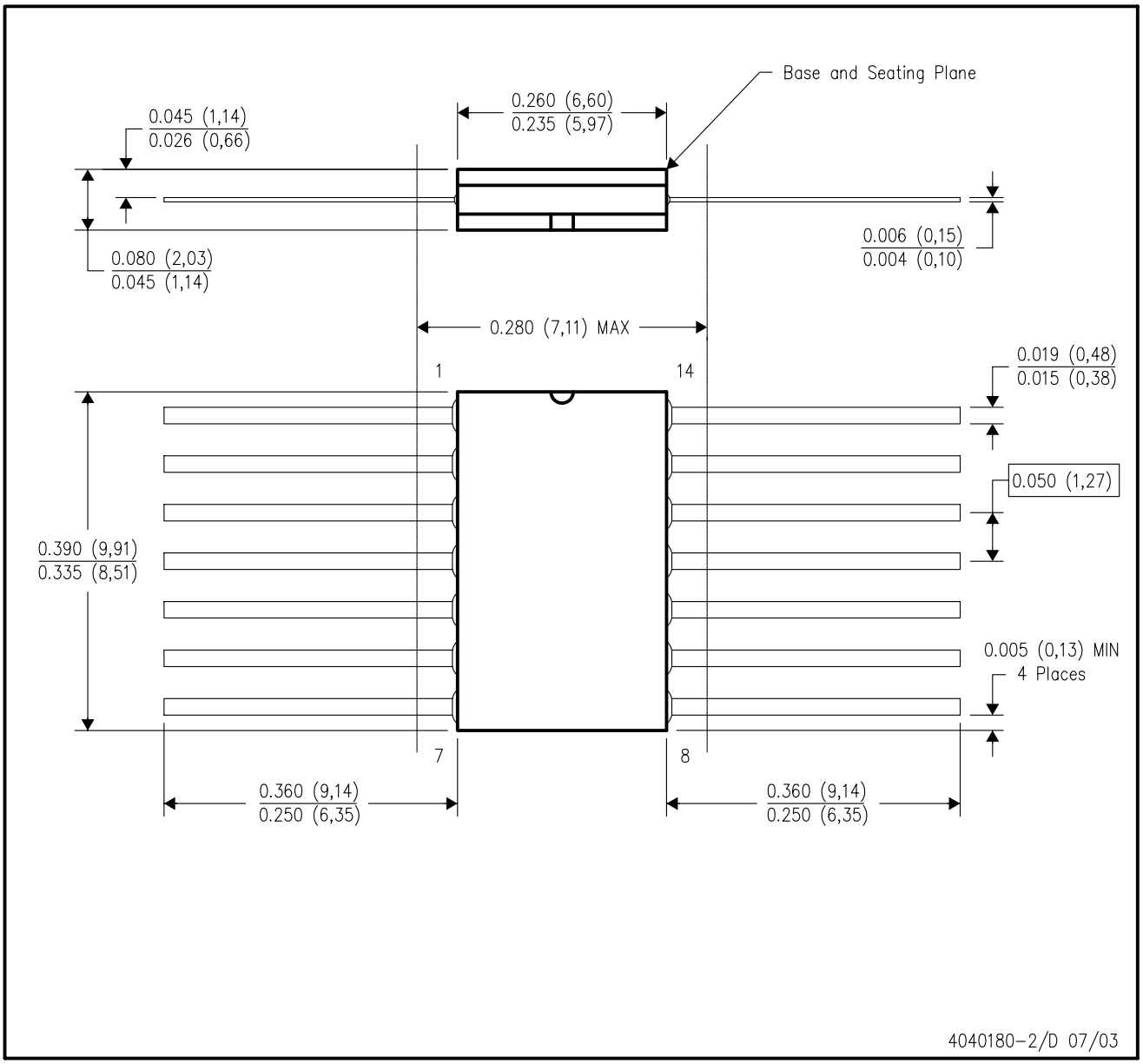
MCER001A – JANUARY 1995 – REVISED JANUARY 1997

JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T8

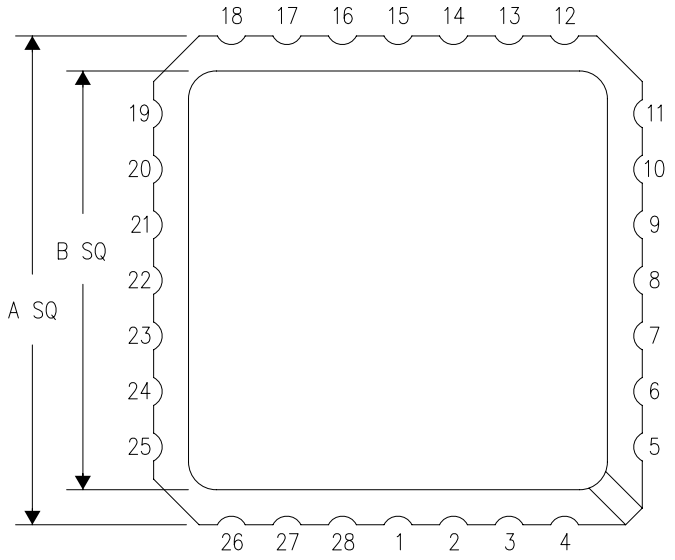
W (R–GDFP–F14) CERAMIC DUAL FLATPACK



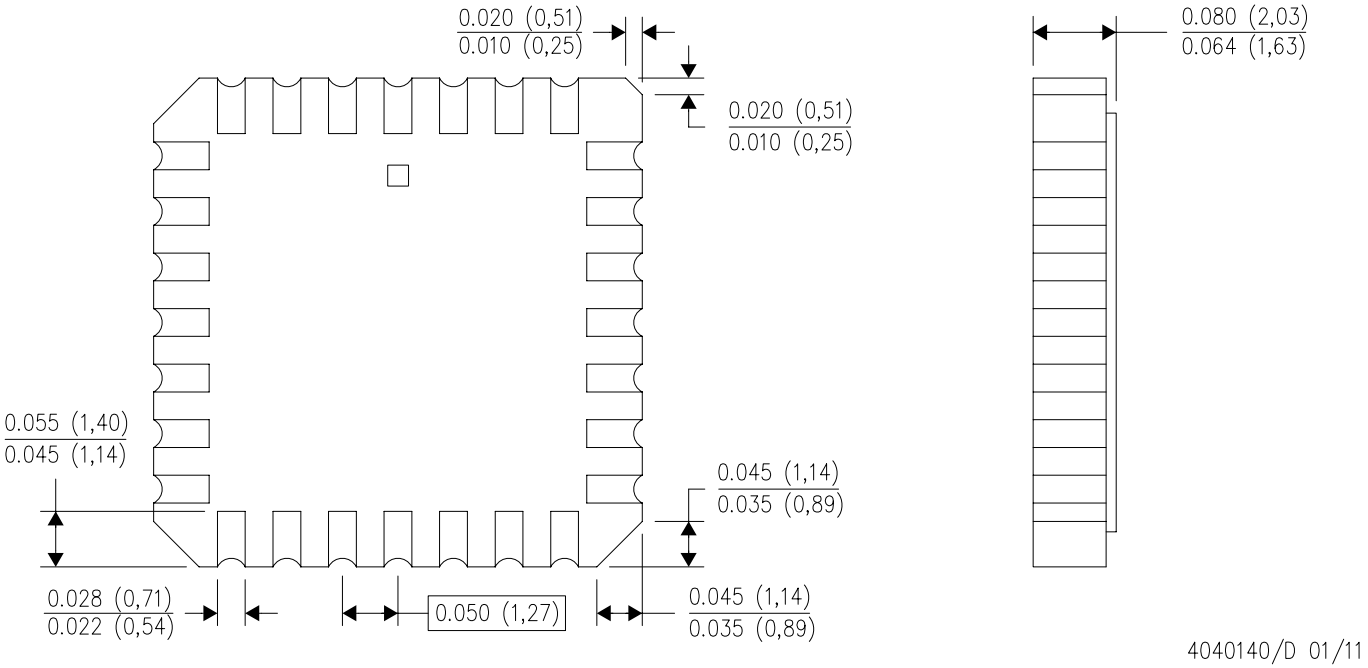
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14 and JEDEC MO–092AB

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



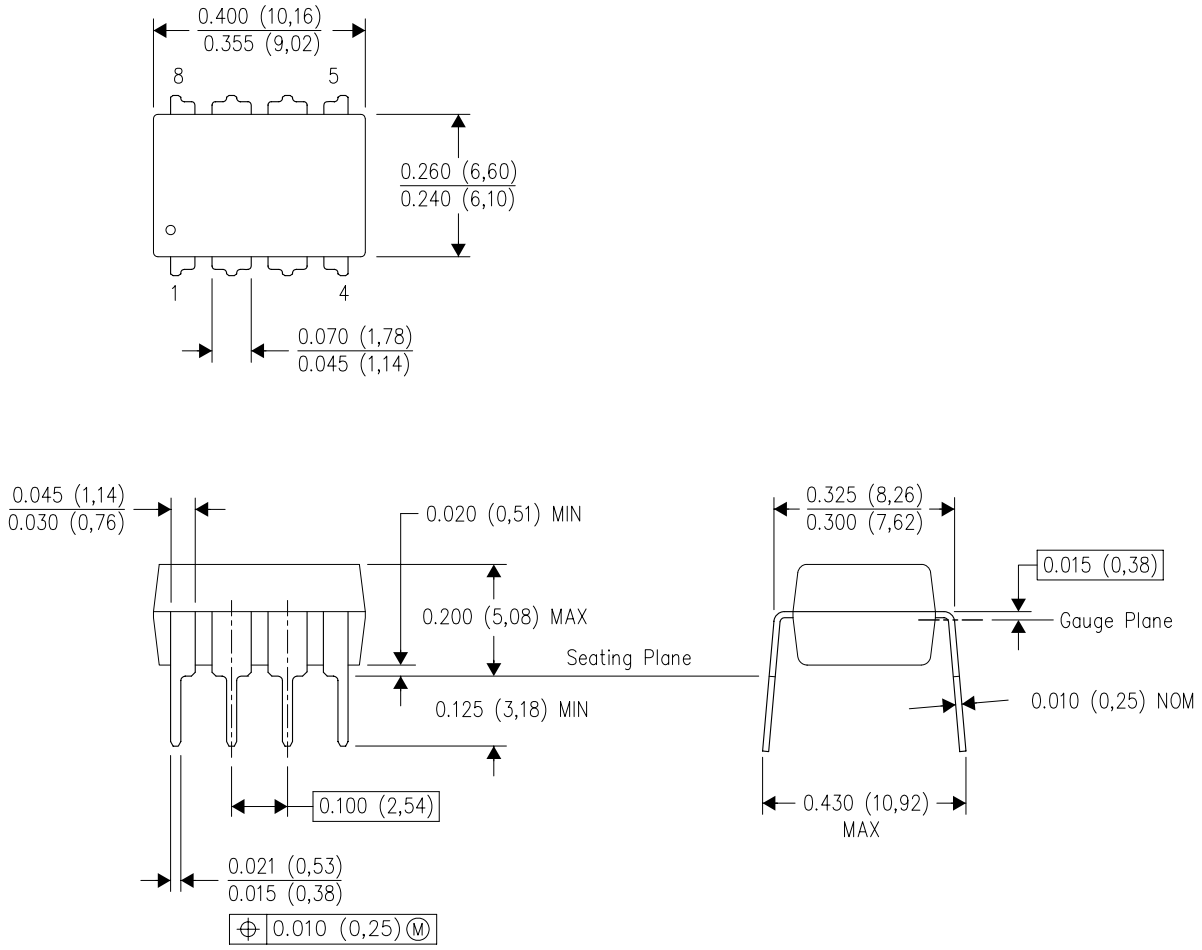
NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

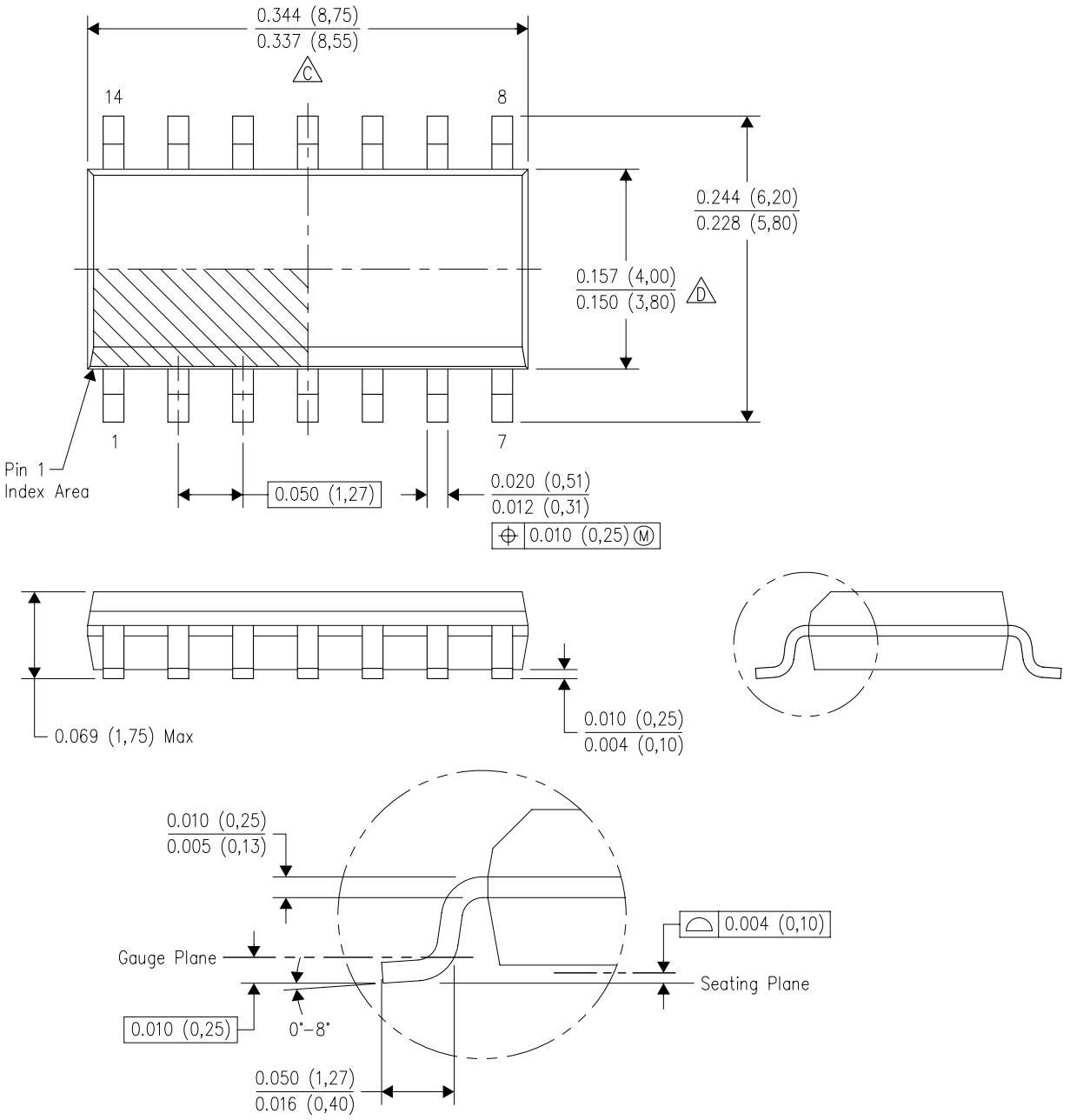
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

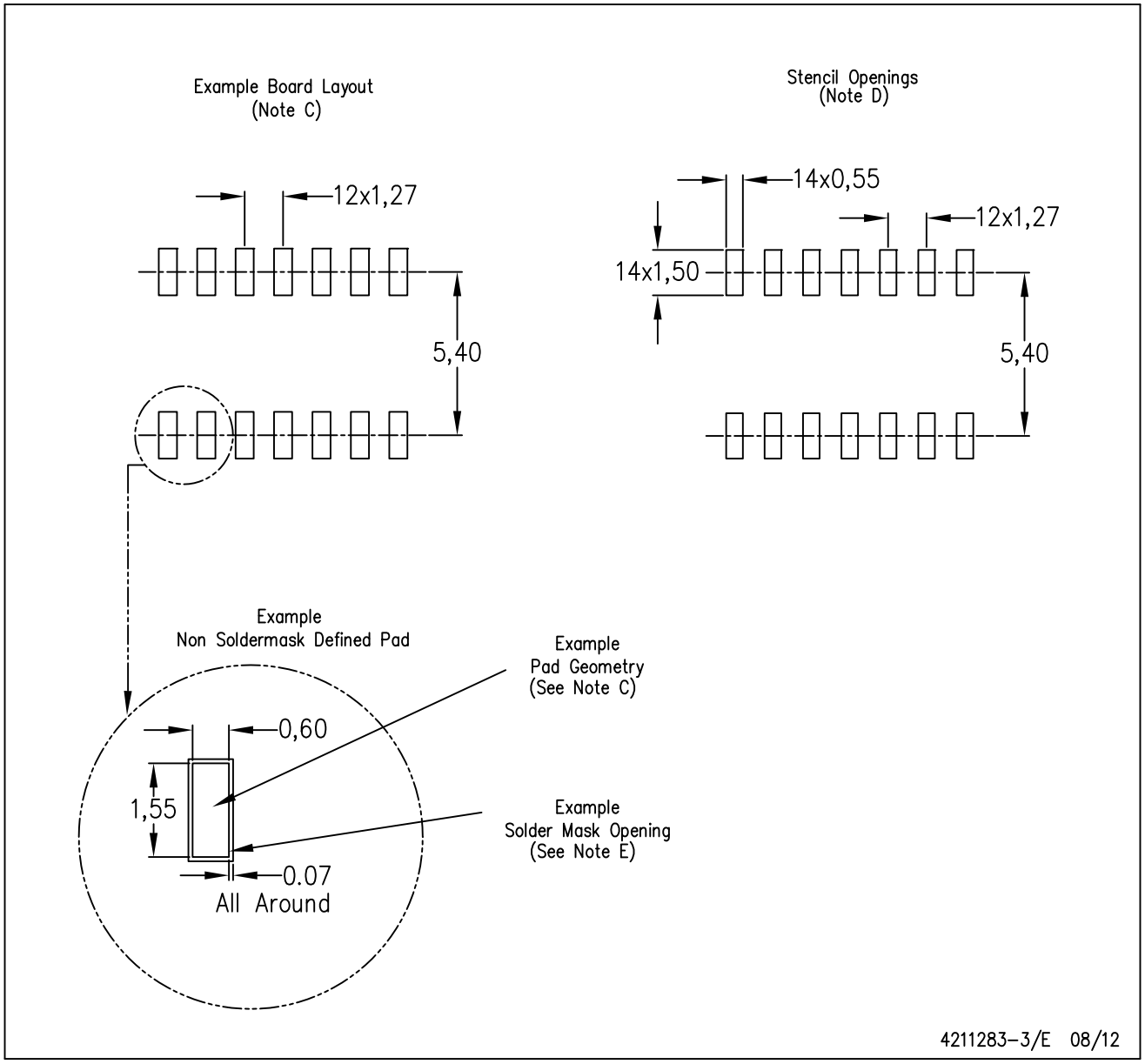
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



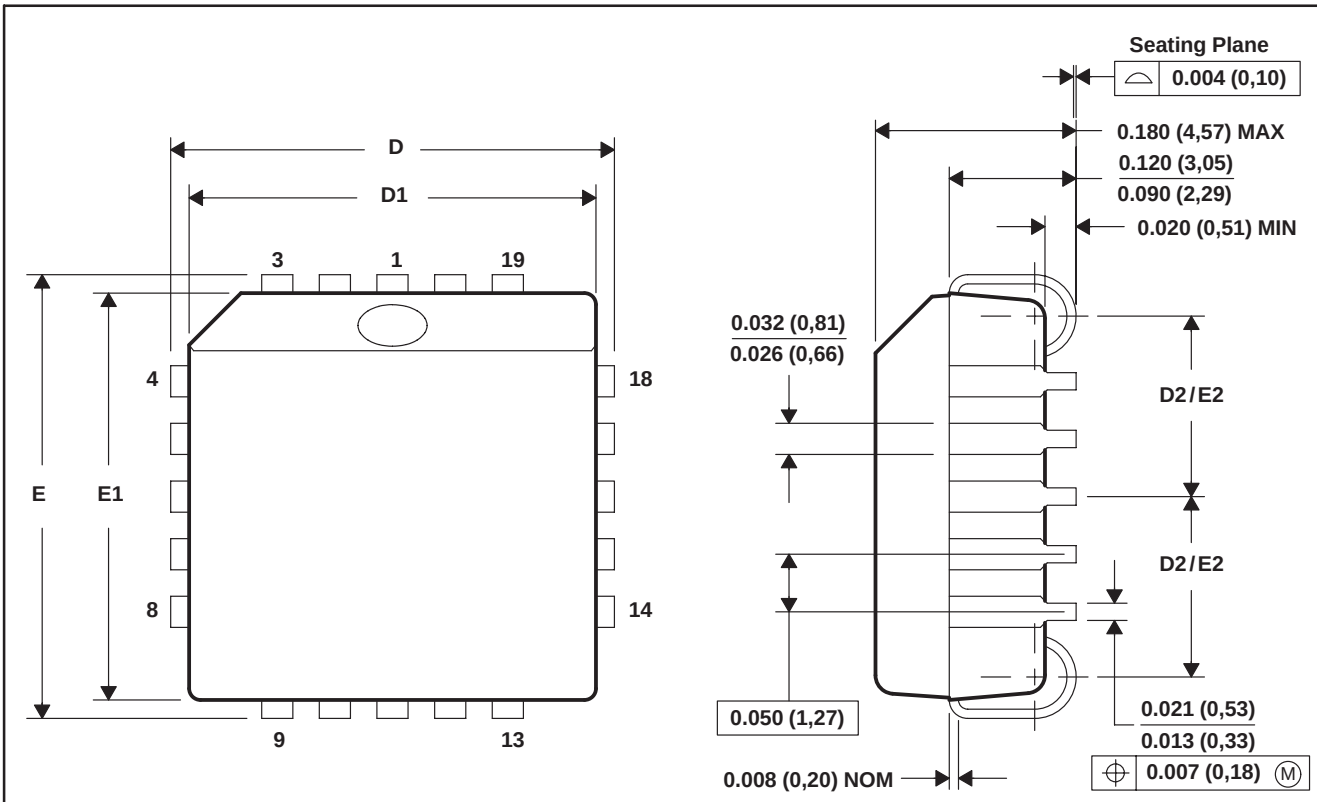
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MPLC004A – OCTOBER 1994

FN (S-PQCC-J**)

PLASTIC J-LEADED CHIP CARRIER

20 PIN SHOWN

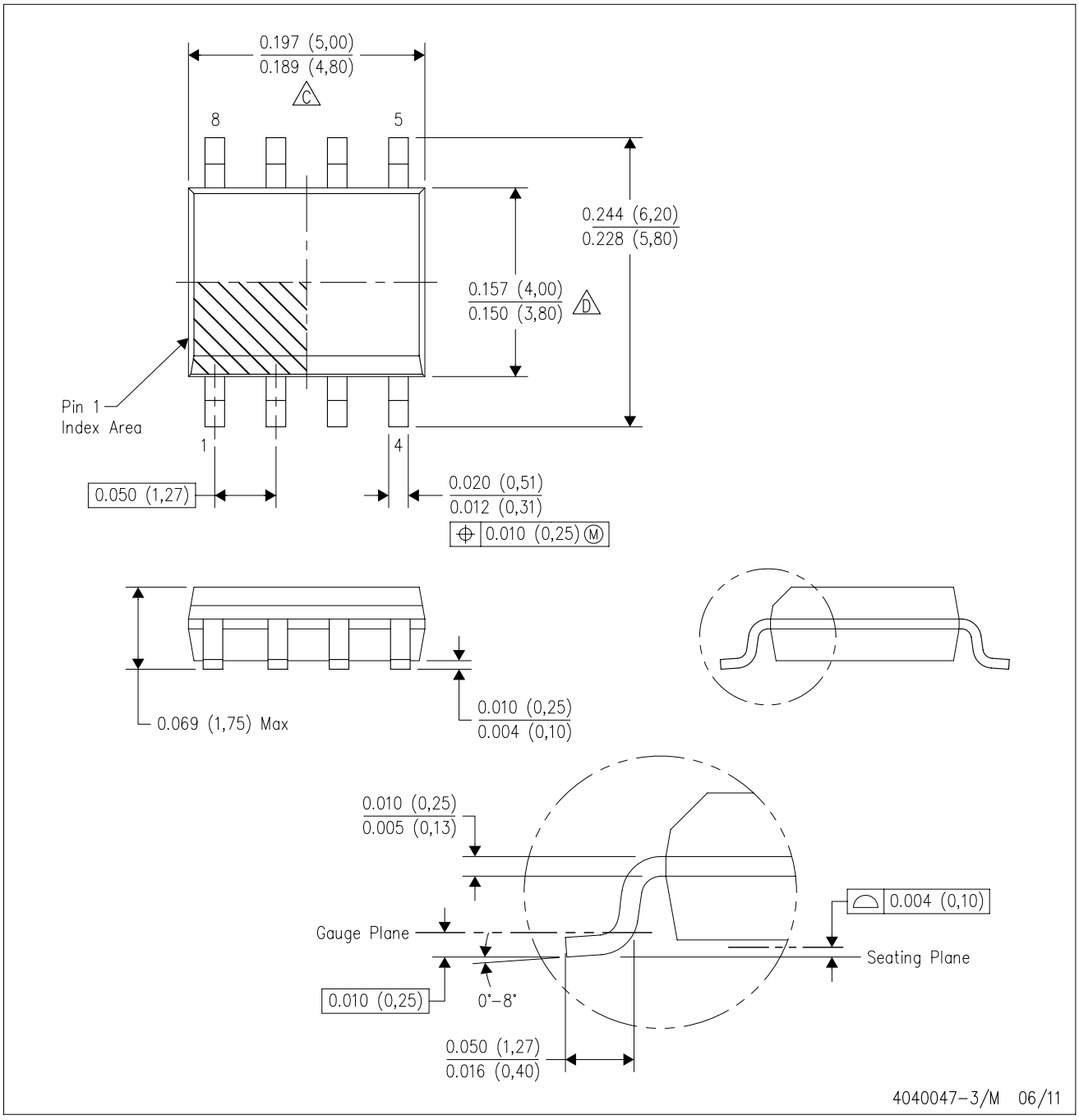


NO. OF PINS **	D/E		D1/E1		D2/E2	
	MIN	MAX	MIN	MAX	MIN	MAX
20	0.385 (9,78)	0.395 (10,03)	0.350 (8,89)	0.356 (9,04)	0.141 (3,58)	0.169 (4,29)
28	0.485 (12,32)	0.495 (12,57)	0.450 (11,43)	0.456 (11,58)	0.191 (4,85)	0.219 (5,56)
44	0.685 (17,40)	0.695 (17,65)	0.650 (16,51)	0.656 (16,66)	0.291 (7,39)	0.319 (8,10)
52	0.785 (19,94)	0.795 (20,19)	0.750 (19,05)	0.756 (19,20)	0.341 (8,66)	0.369 (9,37)
68	0.985 (25,02)	0.995 (25,27)	0.950 (24,13)	0.958 (24,33)	0.441 (11,20)	0.469 (11,91)
84	1.185 (30,10)	1.195 (30,35)	1.150 (29,21)	1.158 (29,41)	0.541 (13,74)	0.569 (14,45)

4040005/B 03/95

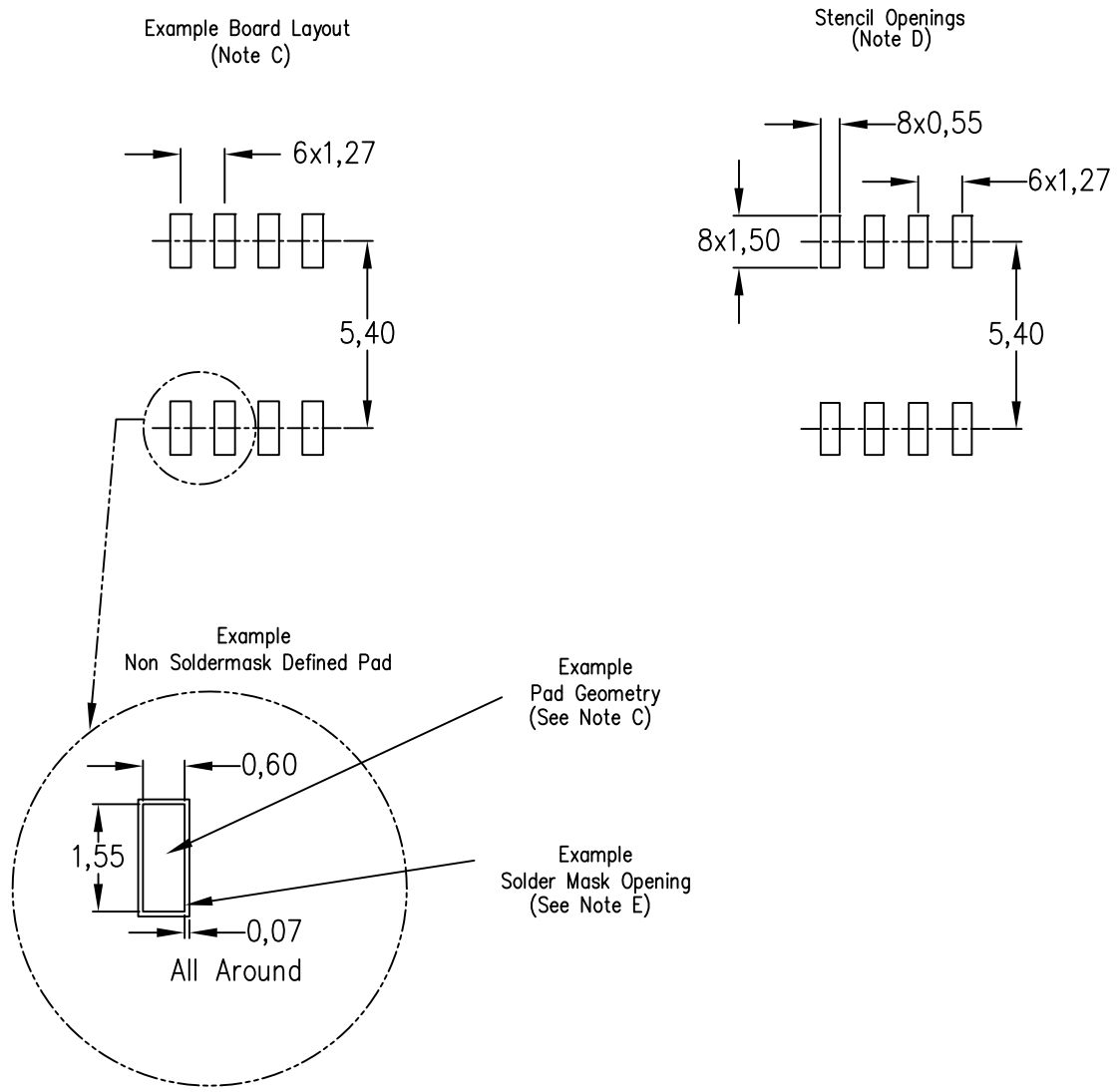
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-018

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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