TSA1001

10-BIT, 25MSPS, 35mW A/D CONVERTER

- 10-bit A/D converter in deep submicron CMOS technology
- Ultra low power consumption: 35mW @ 25Msps (10mW @ 5Msps)
- Single supply voltage: 2.5V
- Input range: 2Vpp differential
- 25Msps sampling frequency
- ENOB=9.7 @ Nyquist
- SFDR typically up to 72dB @ Nyquist
- Built-in reference voltage with external bias capability
- STMicroelectronics 8, 10, 12 and 14-bits ADC pinout compatibility

DESCRIPTION

The TSA1001 is a 10-bit, 25Msps sampling frequency Analog to Digital converter using a CMOS technology combining high performances and very low power consumption.

The TSA1001 is based on a pipeline structure and digital error correction to provide excellent static linearity and go beyond 9.8 effective bits at Fs=25Msps, and Fin=10MHz.

Especially designed for portable applications, the TSA1001 only dissipates 35mW at 25Msps. When running at lower sampling frequencies, even lower consumption can be achieved.

A voltage reference is integrated in the circuit to simplify the design and minimize external components. It is nevertheless possible to use the circuit with an external reference.

The output data can be coded into two different formats. A Data Ready signal is raised as the data is valid on the output and can be used for synchronization purposes.

The TSA1001 is available in commercial (0 to +70°C) and extended (-40 to +85°C) temperature range, in a small 48 pins TQFP package.

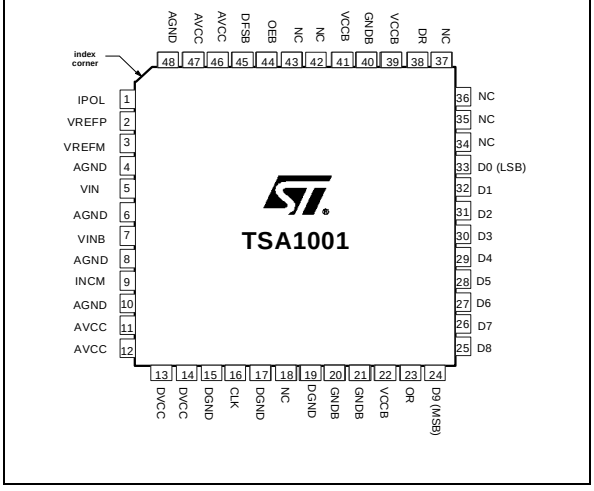
APPLICATIONS

- Portable instrumentation
- Video processing
- Medical imaging and ultrasound
- High resolution fax and scanners
- Digital communications

ORDER CODE

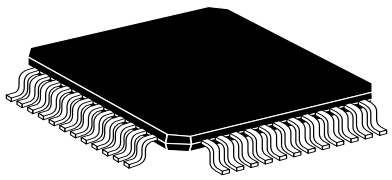
Part Number	Temperature Range	Package	Conditioning	Marking
TSA1001CF	0°C to +70°C	TQFP48	Tray	SA1001C
TSA1001CFT	0°C to +70°C	TQFP48	Tape & Reel	SA1001C
TSA1001IF	-40°C to +85°C	TQFP48	Tray	SA1001I
TSA1001IFT	-40°C to +85°C	TQFP48	Tape & Reel	SA1001I
EVAL1001/AA	Evaluation board			

PIN CONNECTIONS (top view)



PACKAGE

7 × 7 mm TQFP48



ABSOLUTE MAXIMUM RATINGS

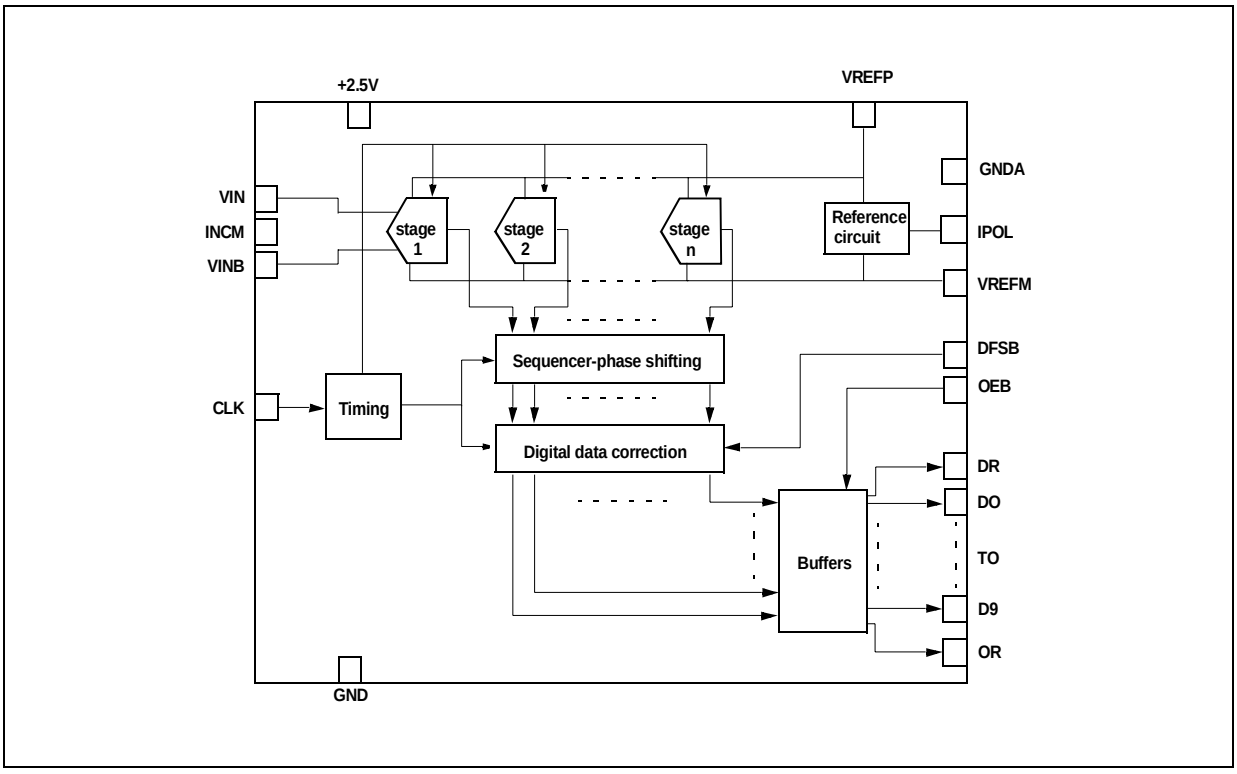
Symbol	Parameter	Values	Unit
AVCC	Analog Supply voltage 1)	0 to 3.3	V
DVCC	Digital Supply voltage 1)	0 to 3.3	V
VCCB	Digital buffer Supply voltage 1)	0 to 3.3	V
IDout	Digital output current	-100 to 100	mA
Tstg	Storage temperature	+150	°C
ESD	Electrical Static Discharge: - HBM - CDM-JEDEC Standard	 2 1.5	KV

1). All voltages values, except differential voltage, are with respect to network ground terminal. The magnitude of input and output voltages must never exceed -0.3V or VCC+0V

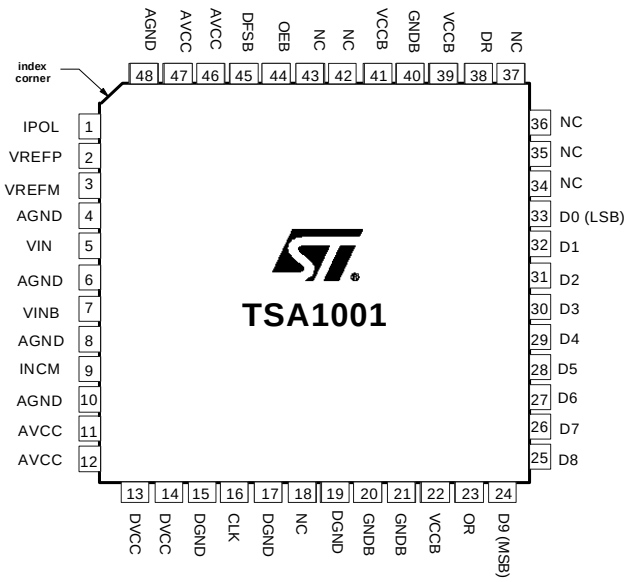
OPERATING CONDITIONS

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
AVCC	Analog Supply voltage		2.25	2.5	2.7	V
DVCC	Digital Supply voltage		2.25	2.5	2.7	V
VCCB	Digital buffer Supply voltage		2.25	2.5	2.7	V
VREFP	Forced top voltage reference		1.16	-	AVCC	V
VREFM	Forced bottom reference voltage		0	0	0.5	V

BLOCK DIAGRAM



PIN CONNECTIONS (top view)



PIN DESCRIPTION

Pin No	Name	Description	Observation	Pin No	Name	Description	Observation
1	IPOL	Analog bias current input		25	D8	Digital output	CMOS output (2.5V)
2	VREFP	Top voltage reference	1V	26	D7	Digital output	CMOS output (2.5V)
3	VREFM	Bottom voltage reference	0V	27	D6	Digital output	CMOS output (2.5V)
4	AGND	Analog ground	0V	28	D5	Digital output	CMOS output (2.5V)
5	VIN	Analog input	1Vpp	29	D4	Digital output	CMOS output (2.5V)
6	AGND	Analog ground	0V	30	D3	Digital output	CMOS output (2.5V)
7	VINB	Inverted analog input	1Vpp	31	D2	Digital output	CMOS output (2.5V)
8	AGND	Analog ground	0V	32	D1	Digital output	CMOS output (2.5V)
9	INCM	Input common mode	0.5V	33	D0(LSB)	Least Significant Bit output	CMOS output (2.5V)
10	AGND	Analog ground	0V	34	NC	Non connected	
11	AVCC	Analog power supply	2.5V	35	NC	Non connected	
12	AVCC	Analog power supply	2.5V	36	NC	Non connected	
13	DVCC	Digital power supply	2.5V	37	NC	Non connected	
14	DVCC	Digital power supply	2.5V	38	DR	Data Ready output	CMOS output (2.5V)
15	DGND	Digital ground	0V	39	VCCB	Digital Buffer power supply	2.5V
16	CLK	Clock input	2.5V compatible CMOS input	40	GNDB	Digital Buffer ground	0V
17	DGND	Digital ground	0V	41	VCCB	Digital Buffer power supply	2.5V
18	NC	Non connected		42	NC	Non connected	
19	DGND	Digital ground	0V	43	NC	Non connected	
20	GNDB	Digital buffer ground	0V	44	OEB	Output Enable input	2.5V compatible CMOS input
21	GNDB	Digital buffer ground	0V	45	DFSB	Data Format Select input	2.5V compatible CMOS input
22	VCCB	Digital buffer power supply	2.5V	46	AVCC	Analog power supply	2.5V
23	OR	Out Of Range output	CMOS output (2.5V)	47	AVCC	Analog power supply	2.5V
24	D9(MSB)	Most Significant Bit output	CMOS output (2.5V)	48	AGND	Analog ground	0V

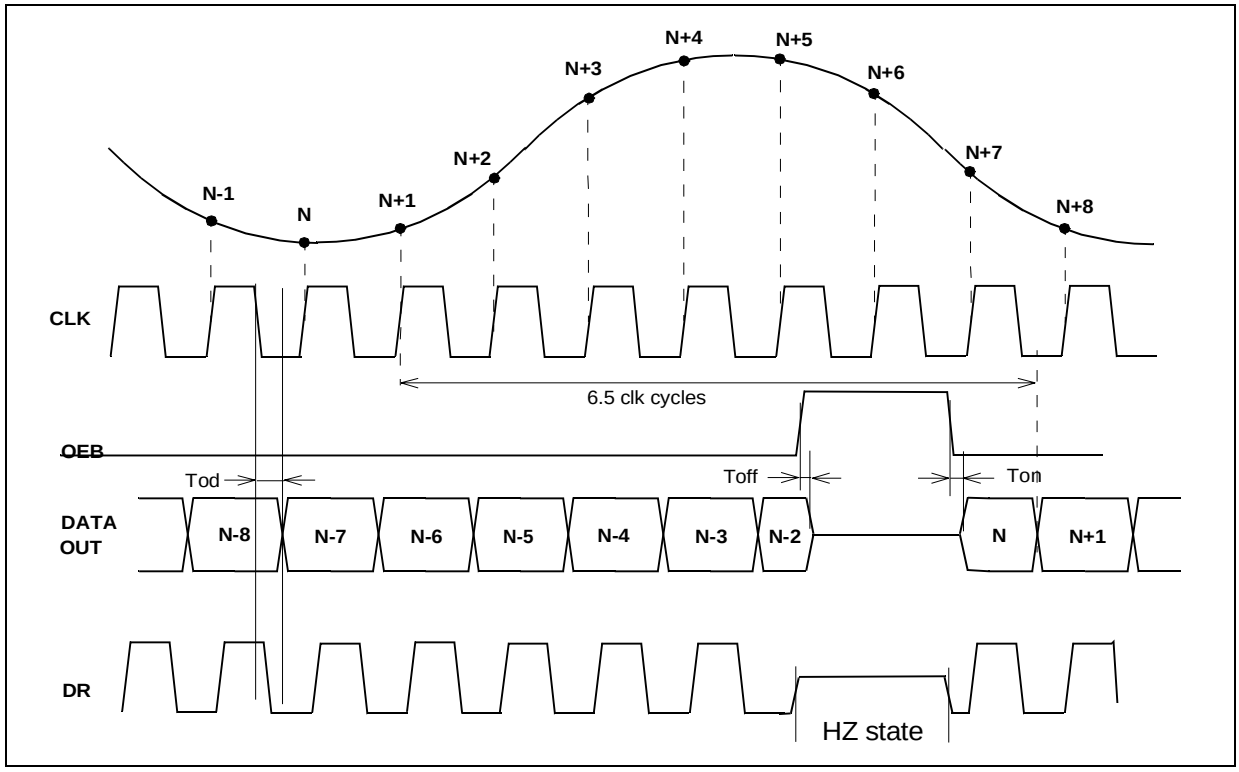
ELECTRICAL CHARACTERISTICS

AVCC = DVCC = VCCB = 2.5V, Fs= 25Msps, Fin=1MHz, Vin@ -1.0dBFS, VREFM = 0V
Tamb = 25°C (unless otherwise specified)

TIMING CHARACTERISTICS

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
FS	Sampling Frequency		0.5		25	MHz
DC	Clock Duty Cycle		45	50	55	%
TC1	Clock pulse width (high)		18	20		ns
TC2	Clock pulse width (low)		18	20		ns
Tod	Data Output Delay (Fall of Clock to Data Valid)	10pF load capacitance		5		ns
Tpd	Data Pipeline delay			6.5		cycles
Ton	Falling edge of OEB to digital output valid data			1		ns
Toff	Rising edge of OEB to digital output tri-state			1		ns

TIMING DIAGRAM



CONDITIONS:
AVCC = DVCC = VCCB = 2.5V, Fs= 25Msps, Fin= 1MHz, Vin@ -1.0dBFS, VREFM= 0V
Tamb = 25°C (unless otherwise specified)

ANALOG INPUTS

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
VIN-VINB	Full scale reference voltage			2.0		Vpp
Cin	Input capacitance			7.		pF
BW	Analog Input Bandwitdh	Vin@Full Scale, FS=25Msps		100		MHz
ERB	Effective Resolution Bandwidth[1)]			60		MHz

1). See parameters definition for more information

REFERENCE VOLTAGE

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
VREFP	Top internal reference voltage		0.91	1.03	1.15	V
		Tmin= -40°C to Tmax= 85°C[1)]	0.90		1.16	V
Vpol	Analog bias voltage		1.20	1.27	1.35	V
		Tmin= -40°C to Tmax= 85°C[1)]	1.19		1.36	V
Ipol	Analog bias current	Normal operating mode	25	50	70	µA
Ipol	Analog bias current	Shutdown mode		0		µA
VINCM	Input common mode voltage		0.48	0.57	0.65	V
		Tmin= -40°C to Tmax= 85°C[1)]	0.48		0.66	V

1). Not fully tested over the temperature range. Guaranted by sampling.

CONDITIONS:
AVCC = DVCC = VCCB = 2.5V, Fs= 25Msps, Fin= 1MHz, Vin@ -1.0dBFS, VREFP=1V, VREFM= 0V
Tamb = 25°C (unless otherwise specified)

POWER CONSUMPTION

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ICCA	Analog Supply current	1)		11.8	14	mA
		Tmin= -40°C to Tmax= 85°C 2)			14	mA
ICCD	Digital Supply Current	1)		1	2	mA
		Tmin= -40°C to Tmax= 85°C 2)			2	mA
ICCB	Digital Buffer Supply Current	1)		1.4	5	mA
		Tmin= -40°C to Tmax= 85°C 2)			5	mA
ICCBZ	Digital Buffer Supply Current in High Impedance Mode	1)		40	100	µA
Pd	Power consumption in normal operation mode	1)		35	47	mW
		Tmin= -40°C to Tmax= 85°C 2)			47	mW
PdZ	Power consumption in High Impedance mode	1)		32	37	mW
Rthja	Junction-ambient thermal resistor (TQFP48)			80		°C/W
Rthjc	Junction-case thermal resistor (TQFP48)			18		°C/W

1). Rpol= 25KΩ. Equivalent load: Rload= 470Ω and Cload= 6pF

2). Not fully tested over the temperature range. Guaranted by sampling.

DIGITAL INPUTS AND OUTPUTS

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Digital inputs						
VIL	Logic "0" voltage				0.8	V
VIH	Logic "1" voltage		2.0			V
Digital Outputs						
VOL	Logic "0" voltage	Iol=10µA			0.4	V
VOH	Logic "1" voltage	Ioh=10µA	2.4			V
IOZ	High Impedance leakage current	OEB set to VIH	-1.5		1.5	µA
C_L	Output Load Capacitance				15	pF

ACCURACY

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
OE	Offset Error		-5	±0.1	+5	%
DNL	Differential Non Linearity		-0.7	±0.3	+0.7	LSB
INL	Integral Non Linearity		-0.8	±0.3	+0.8	LSB
-	Monotonicity and no missing codes		Guaranted			

CONDITIONS:
AVCC = DVCC = 2.5V, Fs= 25Msps Vin@ -1.0dBFS, VREFP=1V, VREFM= 0V
Tamb = 25°C (unless otherwise specified)

DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
SFDR	Spurious Free Dynamic Range	Fin= 5MHz 1) Fin= 10MHz	66 66	80.5 76		dBc
		Fin= 5MHz 2) Fin= 10MHz	66 66			dBc
SNR	Signal to Noise Ratio	Fin= 5MHz 1) Fin= 10MHz	58 58	59.3 59.3		dB
		Fin= 5MHz 2) Fin= 10MHz	58 58			dB
THD	Total Harmonic Distortion	Fin= 5MHz 1) Fin= 10MHz	63 63	79.5 75		dB
		Fin= 5MHz 2) Fin= 10MHz	62 62			dB
SINAD	Signal to Noise and Distortion-Ratio	Fin= 5MHz 1) Fin= 10MHz	58 58	59.0 59.0		dB
		Fin= 5MHz 2) Fin= 10MHz	58 58			dB
ENOB	Effective Number of Bits	Fin= 5MHz 1) Fin= 10MHz	9.5 9.5	9.70 9.70		bits
		Fin= 5MHz 2) Fin= 10MHz	9.5 9.5			bits

1). Rpol= 25KΩ. Equivalent load: Rload= 470Ω and Cload= 6pF
2). Tmin= -40°C to Tmax= 85°C. Not fully tested over the temperature range. Guaranted by sampling.

DEFINITIONS OF SPECIFIED PARAMETERS

STATIC PARAMETERS

Static measurements are performed through method of histograms on a 2MHz input signal, sampled at 25Msps, which is high enough to fully characterize the test frequency response. The input level is +1dBFS to saturate the signal.

Differential Non Linearity (DNL)

The average deviation of any output code width from the ideal code width of 1LSB.

Integral Non linearity (INL)

An ideal converter presents a transfer function as being the straight line from the starting code to the ending code. The INL is the deviation for each transition from this ideal curve.

DYNAMIC PARAMETERS

Dynamic measurements are performed by spectral analysis, applied to an input sinewave of various frequencies and sampled at 25Msps.

Spurious Free Dynamic Range (SFDR)

The ratio between the amplitude of fundamental tone (signal power) and the power of the worst spurious signal (not always an harmonic) over the full Nyquist band. It is expressed in dBc.

Total Harmonic Distortion (THD)

The ratio of the rms sum of the first five harmonic distortion components to the rms value of the fundamental line. It is expressed in dB.

Signal to Noise Ratio (SNR)

The ratio of the rms value of the fundamental component to the rms sum of all other spectral components in the Nyquist band ($f_S/2$) excluding DC, fundamental and the first five harmonics. SNR is reported in dB.

Signal to Noise and Distorsion Ratio (SINAD)

Similar ratio as for SNR but including the harmonic distortion components in the noise figure (not DC signal). It is expressed in dB.
From the SINAD, the Effective Number of Bits (ENOB) can easily be deduced using the formula:
$SINAD = 6.02 \times ENOB + 1.76$ dB.
When the applied signal is not Full Scale (FS), but has an A_0 amplitude, the SINAD expression becomes:
$SINAD = 6.02 \times ENOB + 1.76 \text{ dB} + 20 \log (2A_0/FS)$
The ENOB is expressed in bits.

Analog Input Bandwidth

The maximum analog input frequency at which the spectral response of a full power signal is reduced by 3dB. Higher values can be achieved with smaller input levels.

Effective Resolution Bandwidth (ERB)

The band of input signal frequencies that the ADC is intended to convert without loosing linearity i.e. the maximum analog input frequency at which the SINAD is decreased by 3dB or the ENOB by 1/2 bit.

Pipeline delay

Delay between time when the analog input is initially sampled and time when the corresponding digital data output is valid on the output bus. Also called data latency. It is expressed as a number of clock cycles.

EQUIVALENT CIRCUITS

Figure 1 : Analog Input Circuit

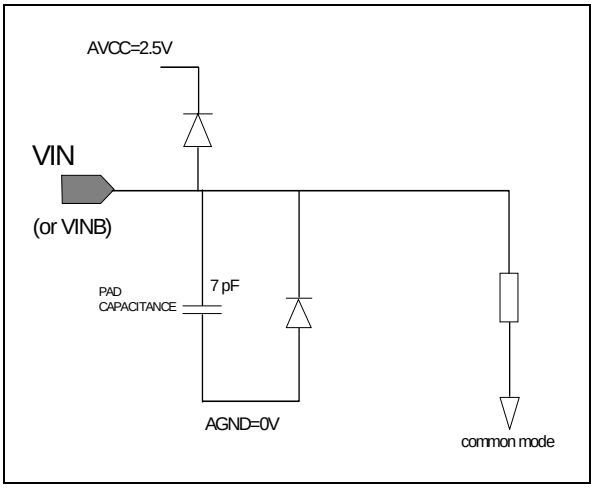


Figure 2 : Input clock circuit

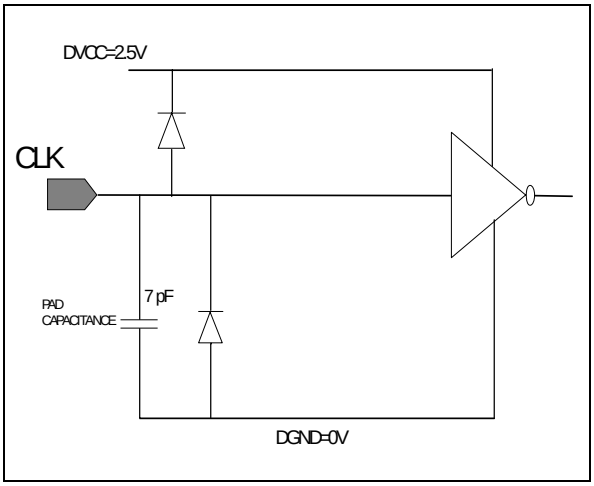


Figure 3 : Input buffers

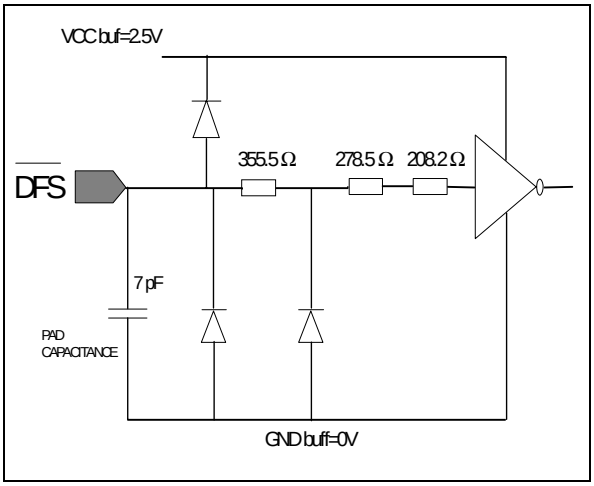
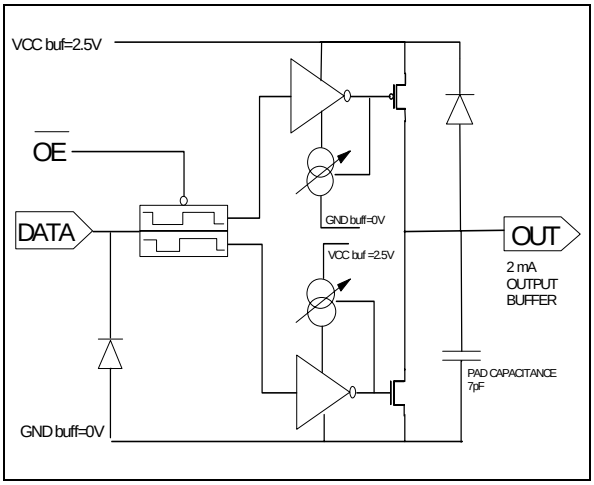
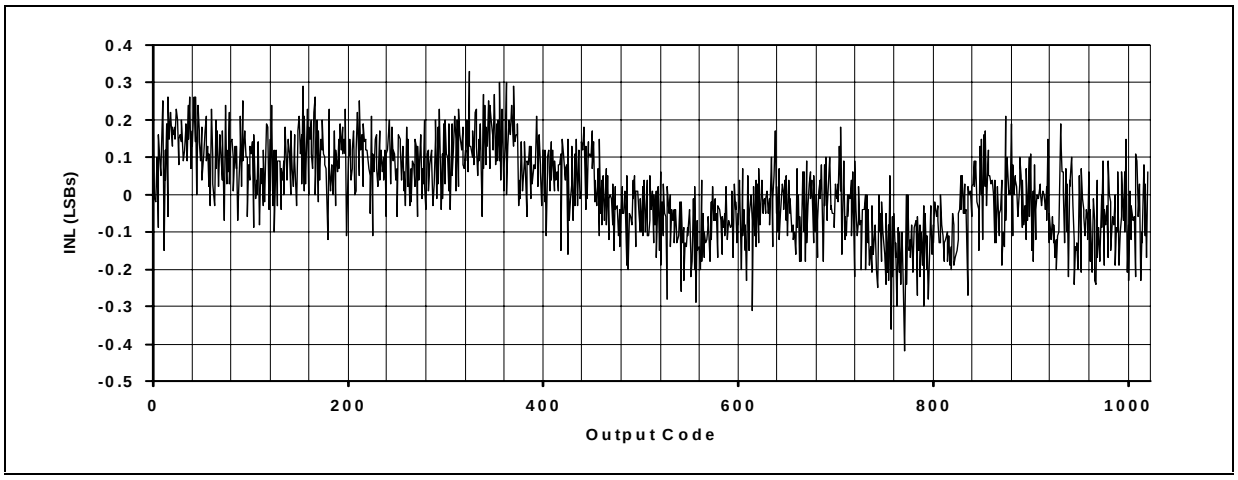


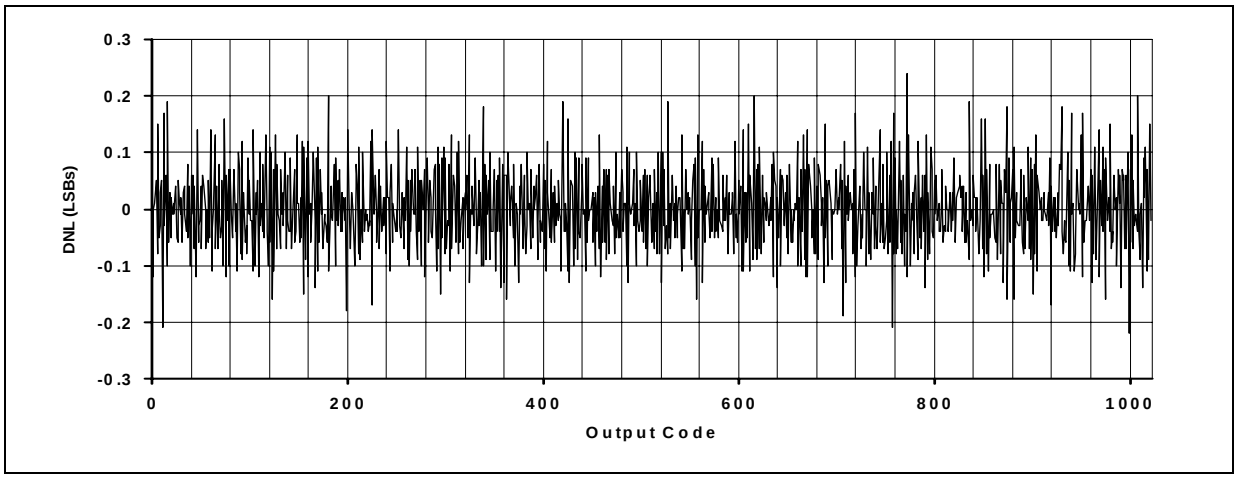
Figure 4 : Tri-state output buffers



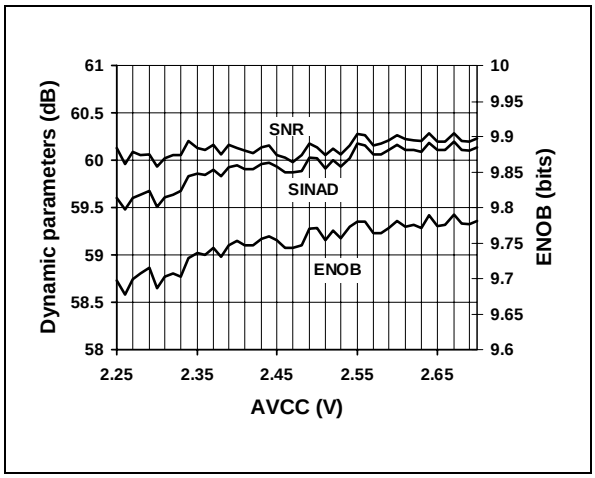
Static parameter: Integral Non Linearity
Fs=25MSPS; Fin=1MHz; Icca=11mA; N=131072pts



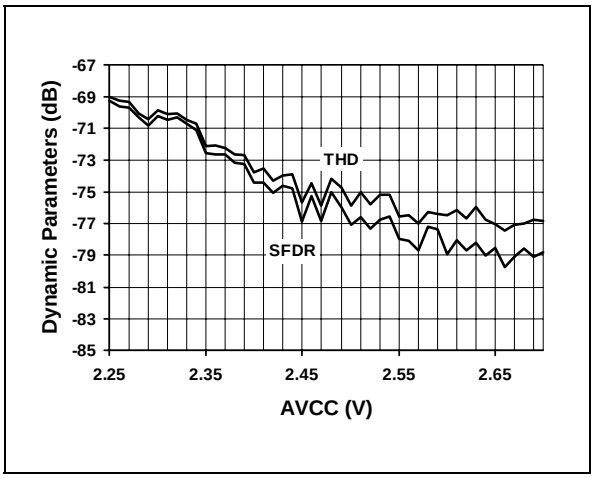
Static parameter: Differential Non Linearity
Fs=25MSPS; Fin=1MHz; Icca=11mA; N=131072 pts



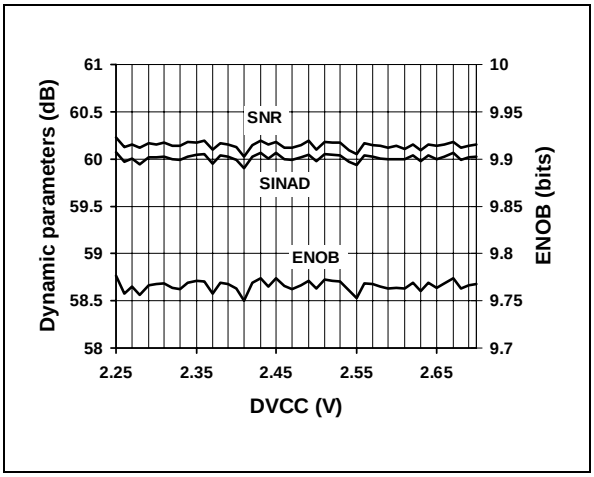
Linearity vs. AVcc
Fs=25MSPS; Icca=11mA; Fin=1MHz



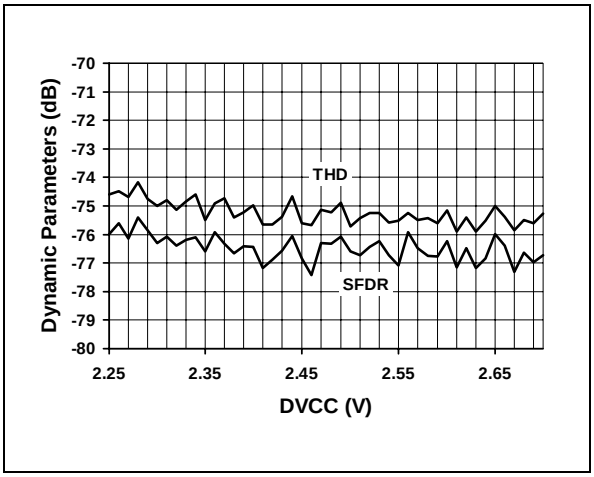
Distortion vs. AVcc
Fs=25MSPS; Icca=11mA; Fin=1MHz



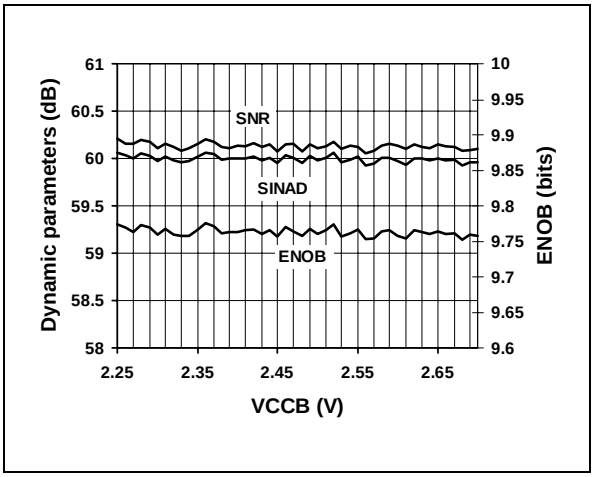
Linearity vs. DVcc
Fs=25MSPS; Icca=11mA; Fin=1MHz



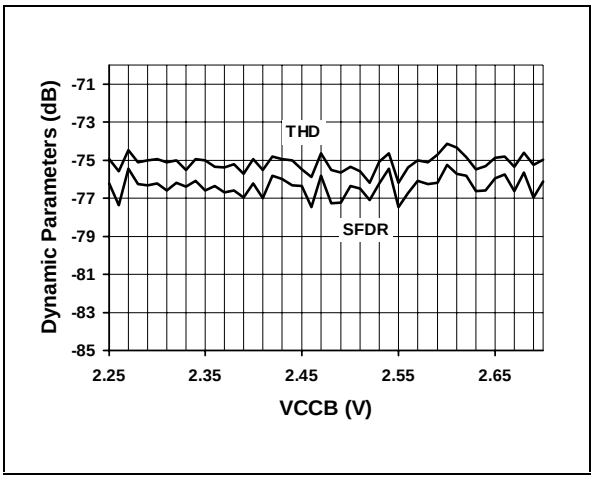
Distortion vs. DVcc
Fs=25MSPS; Icca=11mA; Fin=1MHz



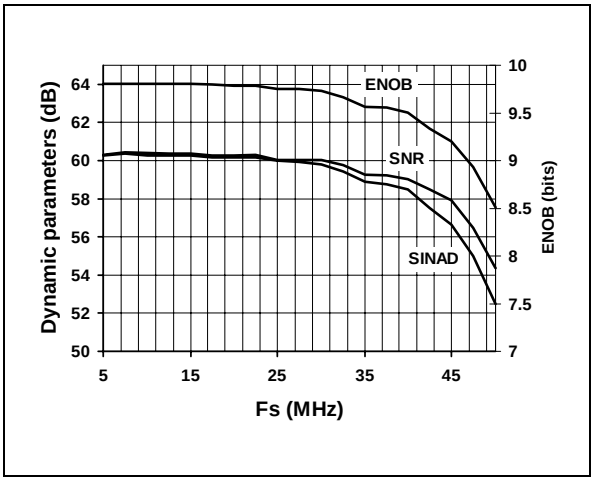
Linearity vs. VccB
Fs=25MSPS; Icca=11mA; Fin=1MHz



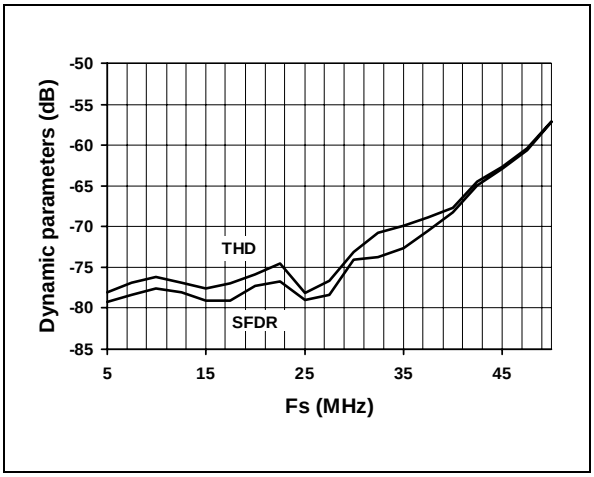
Distortion vs. VccB
Fs=25MSPS; Icca=11mA; Fin=1MHz



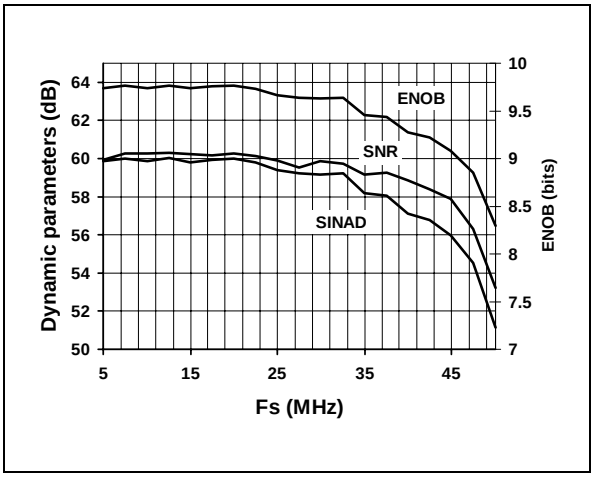
Linearity vs. Fs
Icca=11mA; Fin=1MHz



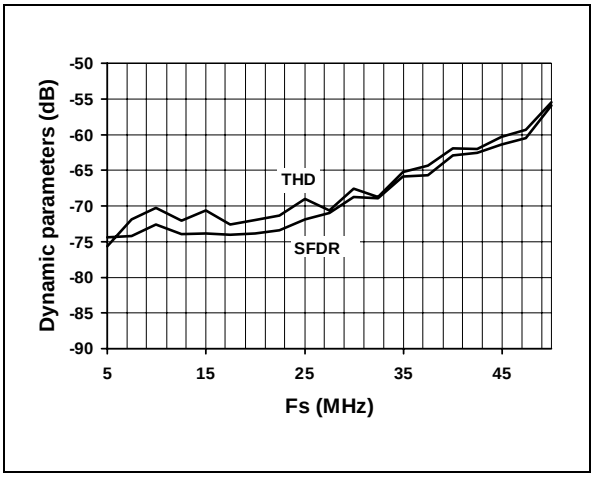
Distortion vs. Fs
Icca=11mA; Fin=1MHz



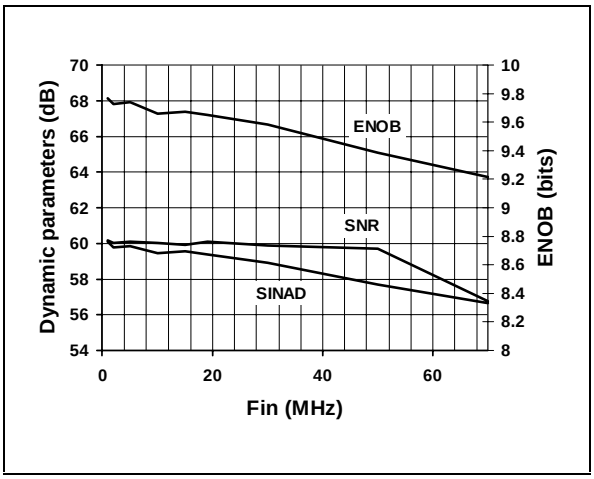
Linearity vs. Fs
Icca=11mA; Fin=15MHz



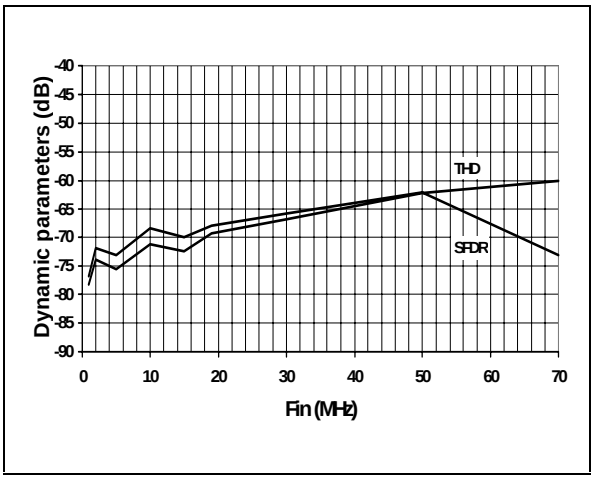
Distortion vs. Fs
Icca=11mA; Fin=15MHz



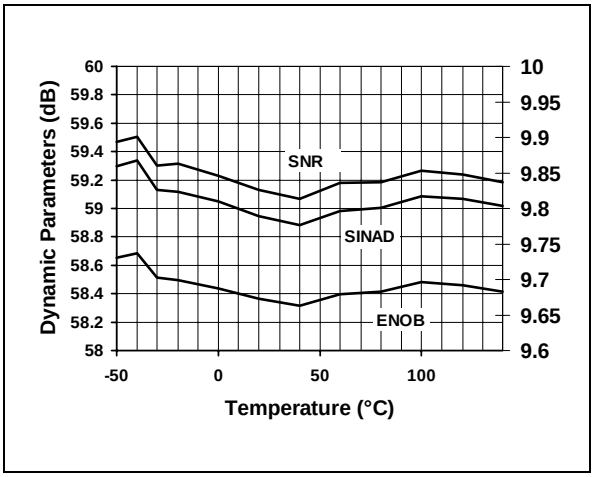
Linearity vs. Fin
Fs=25MSPS; Icca=11mA



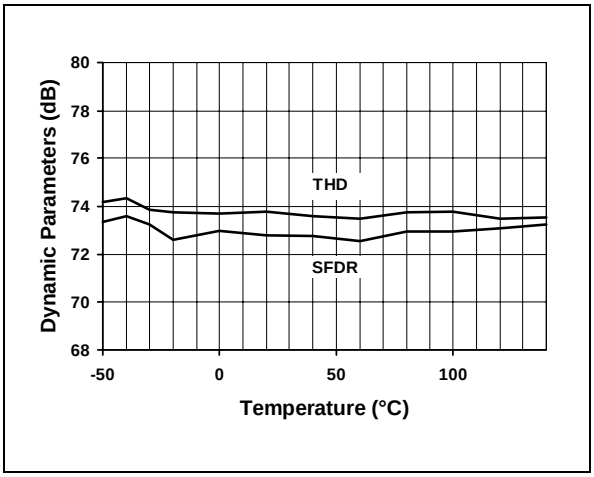
Distortion vs. Fin
Fs=25MSPS; Icca=11mA



Linearity vs.Temperature
Fs=25MSPS; Icca=11mA; Fin=5MHz



Distortion vs. Temperature
Fs=25MSPS; Icca=11mA; Fin=5MHz;



DETAILED INFORMATION

The TSA1001 is a High Speed analog to digital converter based on a pipeline architecture and the latest deep submicron CMOS process to achieve the best performances in terms of linearity and power consumption.

The pipeline structure consists of 9 internal conversion stages in which the analog signal is fed and sequencially converted into digital data.

Each 8 first stages consists of an Analog to Digital converter, a Digital to Analog converter, a Sample and Hold and a gain of 2 amplifier. A 1.5bit conversion resolution is achieved in each stage. The latest stage simply is a comparator. Each resulting LSB-MSB couple is then time shifted to recover from the conversion delay. Digital data correction completes the processing by recovering from the redundancy of the (LSB-MSB) couple for each stage. The corrected data are outputed through the digital buffers.

Signal input is sampled on the rising edge of the clock while digital outputs are delivered on the falling edge of the Data Ready signal.

The advantages of such a converter reside in the combination of pipeline architecture and the most advanced technologies. The highest dynamic performances are achieved while consumption remains at the lowest level.

Some functionalities have been added in order to simplify as much as possible the application board. These operational modes are described in the following table.

The TSA1001 is pin to pin compatible with the 8bits/40Msps TSA0801, the 10bits/50Msps TSA1002 and the 12bits/50Msps TSA1201. This ensures a conformity within the product family and above all, an easy upgrade of the application.

OPERATIONAL MODES DESCRIPTION

Inputs					Outputs		
Analog input differential level			DFSB	OEB	OR	DR	Most Significant Bit (MSB)
(VIN-VINB)	>	RANGE	H	L	H	CLK	D9
-RANGE	>	(VIN-VINB)	H	L	H	CLK	D9
RANGE>	(VIN-VINB)	>-RANGE	H	L	L	CLK	D9
(VIN-VINB)	>	RANGE	L	L	H	CLK	Complemented D9
-RANGE	>	(VIN-VINB)	L	L	H	CLK	Complemented D9
RANGE>	(VIN-VINB)	>-RANGE	L	L	L	CLK	Complemented D9
X			X	H	HZ	HZ	HZ

Data Format Select (DFSB)

When set to low level (VIL), the digital input DFSB provides a two's complement digital output MSB. This can be of interest when performing some further signal processing.

When set to high level (VIH), DFSB provides a standard binary output coding.

Output Enable (OEB)

When set to low level (VIL), all digital outputs remain active and are in low impedance state. When set to high level (VIH), all digital outputs buffers are in high impedance state. This results in lower consumption while the converter goes on sampling.

When OEB is set to low level again, , the data is then valid on the output with a very short Ton delay.

The timing diagram summarizes this operating cycle.

Out of Range (OR)

This function is implemented on the output stage in order to set up an "Out of Range" flag whenever the digital data are over the full scale range.

Typically, there is a detection of all the data being at '0' or all the data being at '1'. This ends up with an output signal OR which is in low level state

(VOL) when the data stay within the range, or in high level state (VOH) when the data is out of the range.

Data Ready (DR)

The Data Ready output is an image of the clock being synchronized on the output data (D0 to D9). This is a very helpful signal that simplifies the synchronization of the measurement equipment or the controlling DSP.

As digital output, DR goes in high impedance state when OEB is asserted to High level as described in the timing diagram.

DRIVING THE ANALOG INPUT

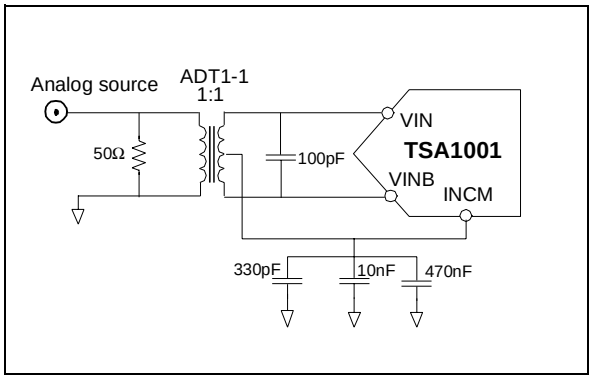
Differential inputs

The TSA1001 has been designed to obtain optimum performances when being differentially driven. An RF transformer is a good way to achieve such performances.

Figure 5 describes the schematics. The input signal is fed to the primary of the transformer, while the secondary drives both ADC inputs. The common mode voltage of the ADC (INCM) is connected to the center-tap of the secondary of the transformer in order to bias the input signal around this common voltage, internally set to 0.56V. The INCM is decoupled to maintain a low noise level on this node. Our evaluation board is mounted with a 1:1 ADT1-1 transformer from Minicircuits. You might also use a higher impedance ratio (1:2 or 1:4) to reduce the driving requirement on the analog signal source.

Each analog input can drive a 1Vpp amplitude input signal, so the resultant differential amplitude is 2Vpp.

Figure 5 : Differential input configuration

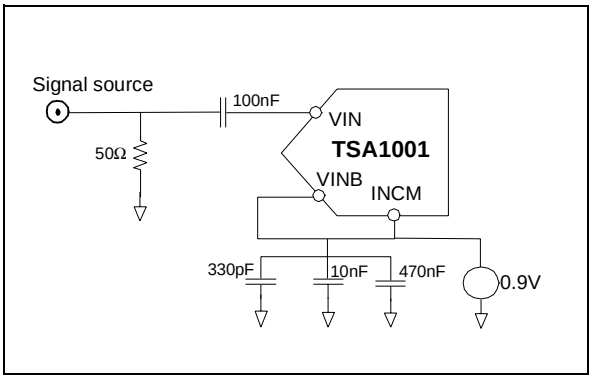


Single-ended input configuration

Some applications may require a single-ended input which is easily achieved with the configuration reported on Figure 6.

In this case, it is recommended to use an AC-coupled analog input and connect the other analog input to the common mode voltage of the circuit (INCM) so as to properly bias the ADC. The INCM may remain at the same internal level (0.56V) thus driving only a 1Vpp input amplitude, or it must be increased to 0.9V to drive a 2Vpp input amplitude. You will get higher performances using a 2Vpp signal.

Figure 6 : Single-ended input configuration



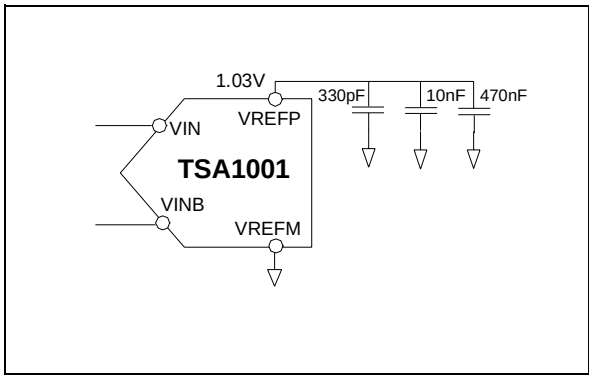
Dynamic characteristics, while not being as remarkable as for differential configuration, are still of very good quality. Measurements done at 25Msps, 1MHz input frequency, -1dBFS input level sum up these performances. An SFDR of -69.5dBc, an SNR of 59.5dB and an ENOB Full Scale of 9.7bits are achieved.

REFERENCE CONNECTION

Internal reference

In the standard configuration, the ADC is biased with the internal reference voltage. VREFM pin is connected to Analog Ground while VREFP is internally set to a voltage of 1.03V. It is recommended to decouple the VREFP in order to minimize low and high frequency noise. Refer to Figure 7 for the schematics.

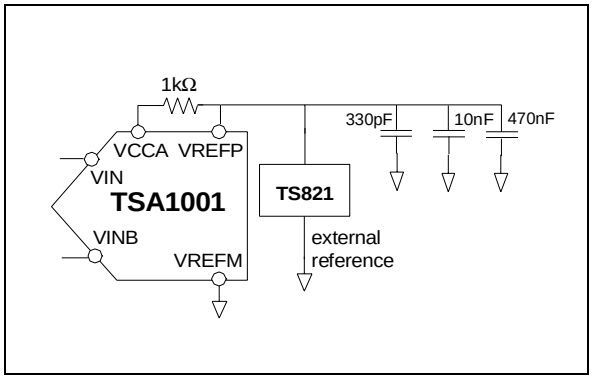
Figure 7 : Internal reference setting



External reference

It is possible to use an external reference voltage instead of the internal one for specific applications requiring even better linearity or enhanced temperature behaviour. In this case, the amplitude of the external voltage must be at least equal to the internal one (1.03V). Using the STMicroelectronics Vref TS821 leads to optimum performances when configured as shown on Figure 8.

Figure 8 : External reference setting



At 15Msps sampling frequency, 1MHz input frequency and -1dBFS amplitude signal, performances can be improved of up to 2dBc on SFDR and 0.3dB on SINAD. At 25Msps sampling frequency, 1MHz input frequency and -1dBFS amplitude signal, performances can be improved of up to 1dBc on SFDR and 0.5dB on SINAD.

This can be very helpful for example for multichannel application to keep a good matching among the sampling frequency range.

Clock input

The quality of your converter is very dependant on your clock input accuracy, in terms of aperture jitter; the use of low jitter crystal controlled oscillator is recommended.

The duty cycle must be between 45% and 55%.

The clock power supplies must be separated from the ADC output ones to avoid digital noise modulation at the output.

It is recommended to always keep the circuit clocked, even at the lowest specified sampling frequency of 0.5Msps, before applying the supply voltages.

Power consumption optimization

The internal architecture of the TSA1001 enables to optimize the power consumption according to the sampling frequency of the application. For this purpose, a resistor is placed between IPOL and the analog Ground pins.

The TSA1001 will combine highest performances and lowest consumption at 25Msps when Rpol is equal to 25kΩ.

At lower sampling frequency range (< 10Msps), this value of resistor may be adjusted in order to decrease the analog current without any degradation of dynamic performances.

As an example, 10mW total power consumption is achieved at 5 Msps with Rpol equal to 390kΩ.

The table below sums up the relevant data.

Total power consumption optimization depending on Rpol value

Fs (Msps)	5	15	25
Rpol (kΩ)	390	40	25
Optimized power (mW)	10	25	35

Layout precautions

To use the ADC circuits in the best manner at high frequencies, some precautions have to be taken for power supplies:

- First of all, the implementation of 4 separate proper supplies and ground planes (analog, digital, internal and external buffer ones) on the PCB is mandatory for high speed circuit applications to provide low inductance and low resistance common return.

The separation of the analog signal from the digital part is essential to prevent noise from coupling onto the input signal.

- Power supply bypass capacitors must be placed as close as possible to the IC pins in order to improve high frequency bypassing and reduce harmonic distortion.

- Proper termination of all inputs and outputs must be incorporated with output termination resistors; then the amplifier load will be only resistive and the stability of the amplifier will be improved. All leads must be wide and as short as possible especially for the analog input in order to decrease parasitic capacitance and inductance.

- To keep the capacitive loading as low as possible at digital outputs, short lead lengths of routing are essential to minimize currents when the output changes. To minimize this output capacitance, buffers or latches close to the output pins will relax this constraint.

- Choose component sizes as small as possible (SMD).

EVAL1002 evaluation board

The characterization of the board has been made with a fully ADC devoted test bench as shown on Figure 10. The analog signal must be filtered to be very pure.

The dataready signal is the acquisition clock of the logic analyzer.
The ADC digital outputs are latched by the octal buffers 74LCX573.
All characterization measurements have been made with: SFSR=+0.2dB for static parameters.- SFSR=-0.5dB for dynamic parameters.

Figure 9 : Analog to Digital Converter characterization bench

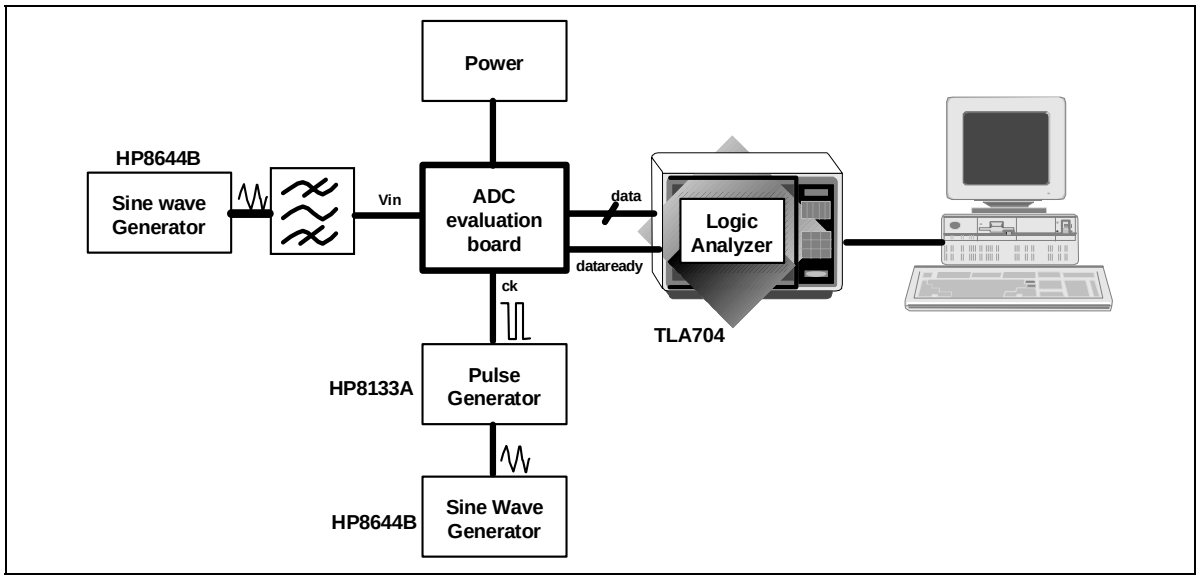


Figure 10 : TSA1001 Evaluation board schematic

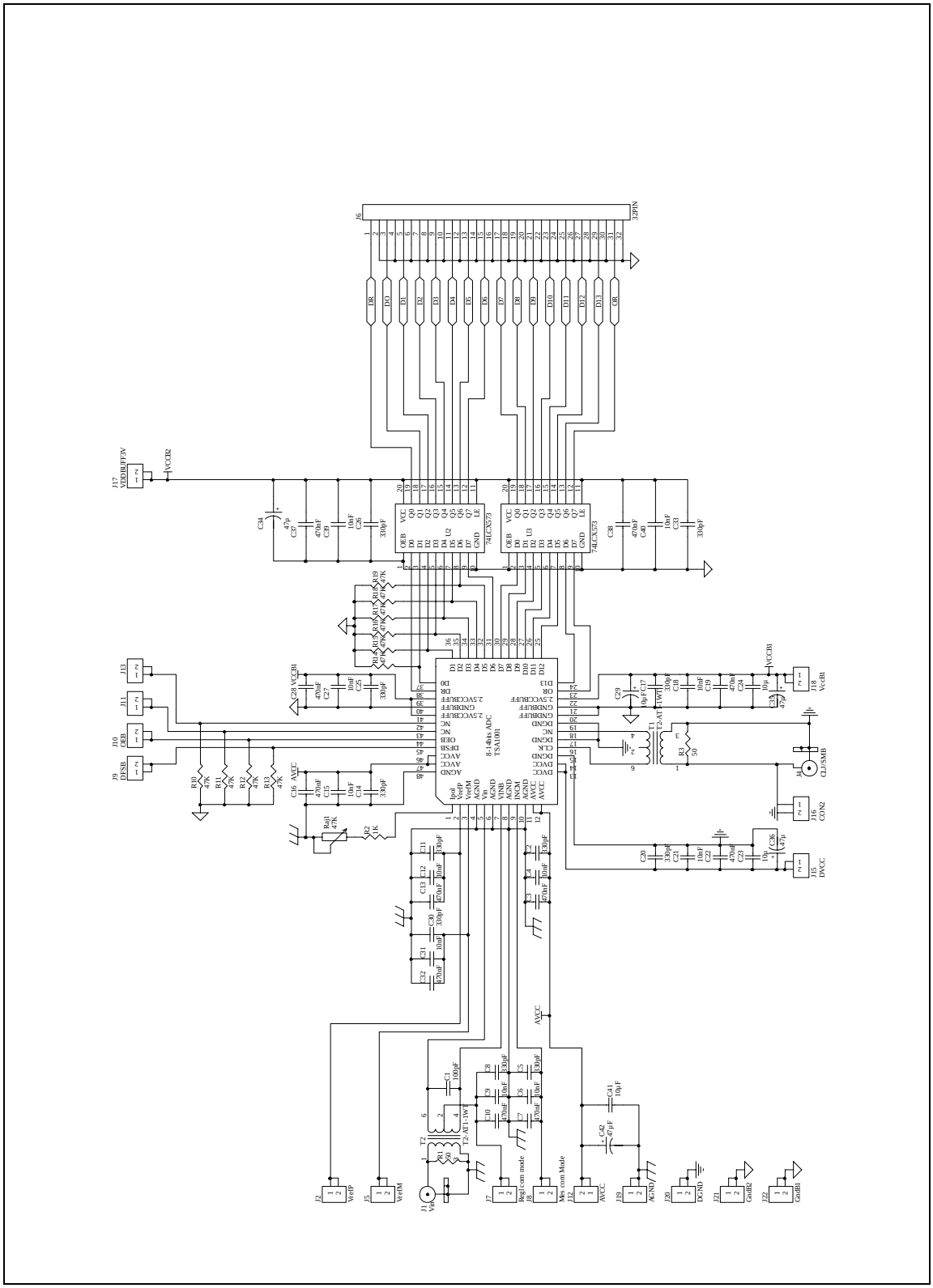
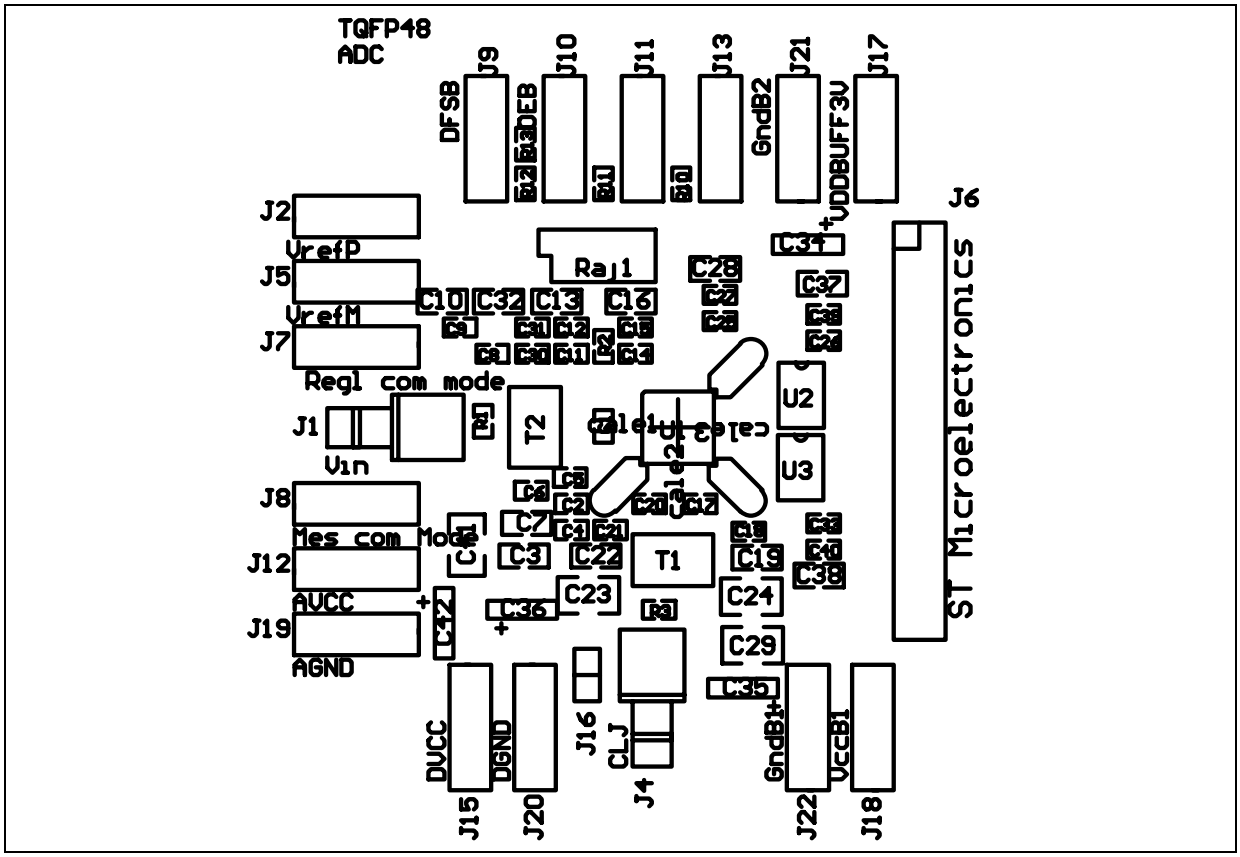


Figure 11 : Printed circuit board - Top side silkscreen

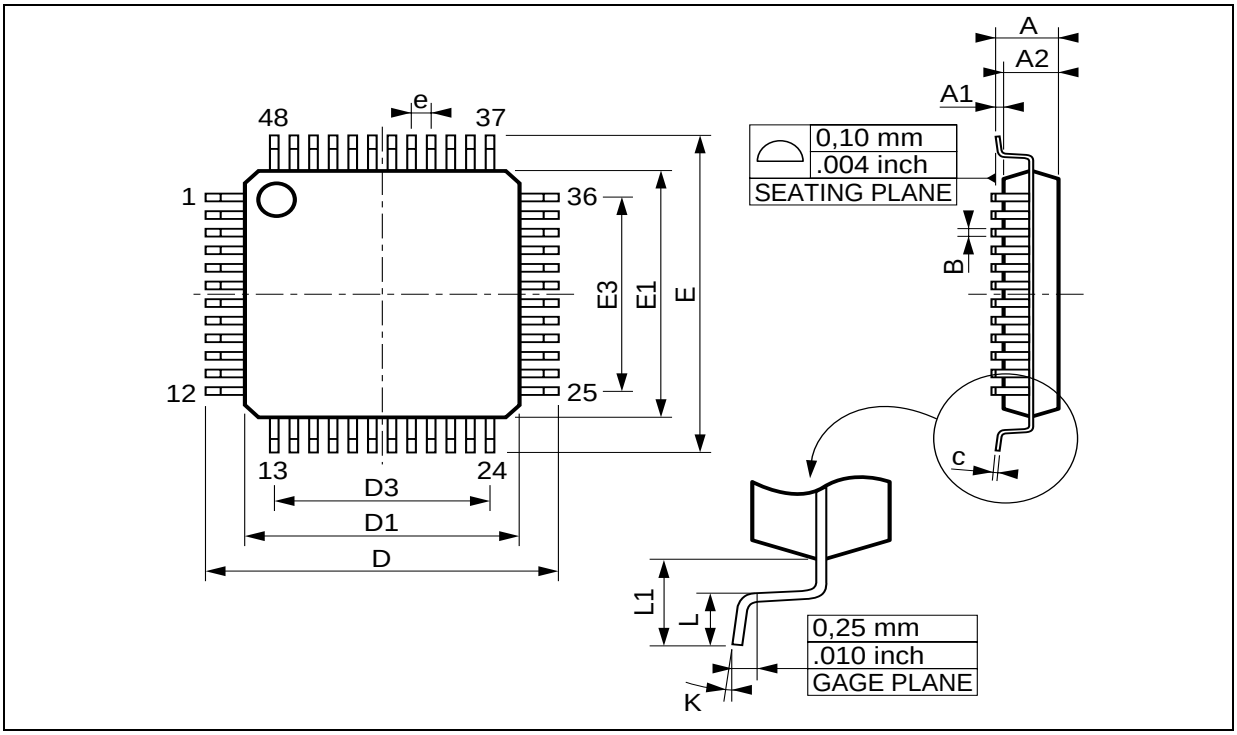


Printed circuit board - List of components

Part Type	Design ator	Footprint	Part Type	Design ator	Footprint	Part Type	Design ator	Footprint	Part Type	Design ator	Footprint
10uF	C24	1210	330pF	C33	603	470nF	C7	805	AVCC	J12	FICHE2MM
10uF	C23	1210	330pF	C20	603	470nF	C16	805	CLJ/SMB	J4	SMB/H
10uF	C41	1210	330pF	C8	603	470nF	C19	805	AGND	J19	FICHE2MM
10uF	C29	1210	330pF	C2	603	470nF	C3	805	DFSB	J9	FICHE2MM
100pF	C1	603	330pF	C5	603	47KΩ	R12	603	DGND	J20	FICHE2MM
10nF	C12	603	330pF	C11	603	47KΩ	R14	603	DVCC	J15	FICHE2MM
10nF	C39	603	330pF	C30	603	47KΩ	R11	603	GndB1	J22	FICHE2MM
10nF	C15	603	330pF	C17	603	47KΩ	Raj1	VR5	GndB2	J21	FICHE2MM
10nF	C40	603	330pF	C14	603	47KΩ	R10	603	Mes com mode	J8	FICHE2MM
10nF	C27	603	47uF	C36	CAP	47KΩ	R19	603	OEB	J10	FICHE2MM
10nF	C4	603	47uF	C34	CAP	47KΩ	R13	603	Regl com mode	J7	FICHE2MM
10nF	C21	603	47uF	C35	CAP	47KΩ	R15	603	T2-AT1-1WT	T2	ADT
10nF	C31	603	47uF	C42	CAP	47KΩ	R16	603	T2-AT1-1WT	T1	ADT
10nF	C6	603	470nF	C22	805	47KΩ	R17	603	VccB1	J18	FICHE2MM
10nF	C9	603	470nF	C32	805	47KΩ	R18	603	VDDBUFF3V	J17	FICHE2MM
10nF	C18	603	470nF	C37	805	50Ω	R3	603	Vin	J1	SMB/H
1KΩ	R2	603	470nF	C38	805	50Ω	R1	603	VrefM	J5	FICHE2MM
32PIN	J6	IDC32	470nF	C13	805	74LCX573	U3	TSSOP20	VrefP	J2	FICHE2MM
330pF	C25	603	470nF	C28	805	74LCX573	U2	TSSOP20	TSA1001	U1	TQFP48
330pF	C26	603	470nF	C10	805	CON2	J16	SIP2			

PACKAGE MECHANICAL DATA

48 PINS - PLASTIC PACKAGE



Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.17	0.22	0.27	0.007	0.009	0.011
C	0.09		0.20	0.004		0.008
D		9.00			0.354	
D1		7.00			0.276	
D3		5.50			0.216	
e		0.50			0.0197	
E		9.00			0.354	
E1		7.00			0.276	
E3		5.50			0.216	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
K	0° (min.), 7° (max.)					