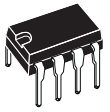
# TS271

## CMOS Programmable Low Power Single Operational Amplifier

- **Offset null capability (by external compensation)**
- **Dynamic characteristics adjustable $I_{SET}$**
- **Consumption current and dynamic parameters are stable regarding the voltage power supply variations**
- **Output voltage can swing to ground**
- **Very large $I_{SET}$ range**
- **Stable and low offset voltage**
- **Three input offset voltage selections**



**N**
**DIP8**
(Plastic Package)

**D**
**SO-8**
(Plastic Micropackage)

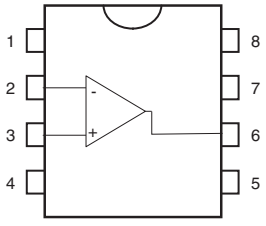
### Description

The TS271 is a low cost, low power single operational amplifier designed to operate with single or dual supplies. This operational amplifier uses the ST silicon gate CMOS process giving it an excellent consumption-speed ratio. This amplifier is ideally suited for low consumption applications.

The power supply is externally programmable with a resistor connected between pins 8 and 4. It allows to choose the best consumption-speed ratio and supply current can be minimized according to the required speed. This device is specified for the following $I_{SET}$ current values: 1.5µA, 25µA, 130µA.

This CMOS amplifier offers very high input impedance and extremely low input currents. The major advantage versus JFET devices is the very low input currents drift with temperature see *Figure 8*, *Figure 19*, *Figure 30*.

### Pin Connections (top view)



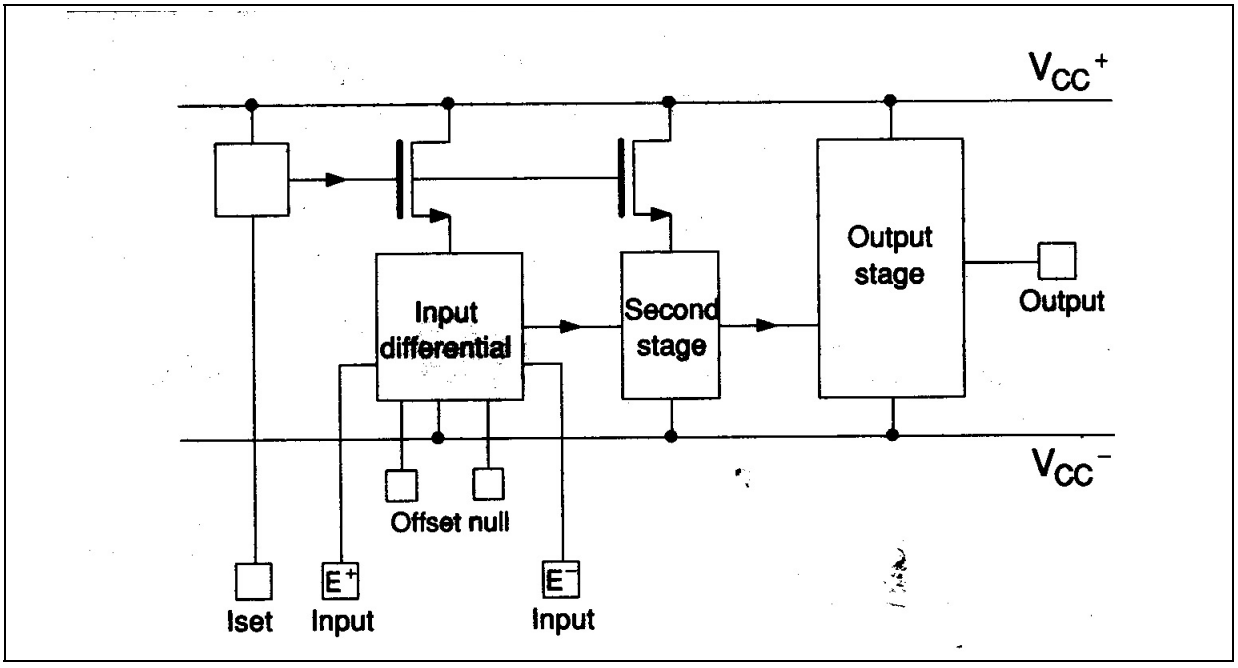

1 - Offset Null 1
2 - Inverting Input 1
3 - Non-inverting Input 1
4 - $V_{CC}^-$
5 - Offset Null 2
6 - Output
7 - $V_{CC}^+$
8 - $I_{Set}$

### Order Codes

| Part Number | Temperature Range | Package | Packaging |
|---|---|---|---|
| TS271CN/ACN | 0°C, +70°C | DIP | Tube |
| TS271CD/CDT/ACD/ACDT | | SO | Tube and Tape & Reel |
| TS271IN/AIN/ | -40°C, +125°C | DIP | Tube |
| TS271ID/IDT/AID/AIDT/BID/BIDT | | SO | Tube and Tape & Reel |
| TS271BMD | -55°C, +125°C | SO | Tube |

# 1 Block Diagram

**Figure 1. Application block diagram**



# 2 Absolute Maximum Ratings

**Table 1. Key parameters and their absolute maximum ratings**

| Symbol | Parameter | TS271C/AC/BC | TS271I/AI/BI | TS271M/AM/BM | Unit |
|---|---|---|---|---|---|
| $VCC^+$ | Supply Voltage [1] | 18 | | | V |
| Vid | Differential Input Voltage [2] | ±18 | | | V |
| $V_i$ | Input Voltage [3] | -0.3 to 18 | | | V |
| $I_o$ | Output Current for $V_{CC}^+ \geq 15V$ | ±30 | | | mA |
| $I_{in}$ | Input Current | ±5 | | | mA |
| $T_{oper}$ | Operating Free-Air Temperature Range | 0 to +70 | -40 to +125 | -55 to +125 | °C |
| $T_{stg}$ | Storage Temperature Range | -65 to +150 | | | °C |

1) All values, except differential voltage are with respect to network ground terminal.

2) Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.

3) The magnitude of the input and the output voltages must never exceed the magnitude of the positive supply voltage.

**Table 2. Operating conditions**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}^+$ | Supply Voltage | 3 to 16 | V |
| $V_{icm}$ | Common Mode Input Voltage Range | 0 to $V_{CC}^+$ - 1.5 | V |

**Figure 2. Schematic Diagram**

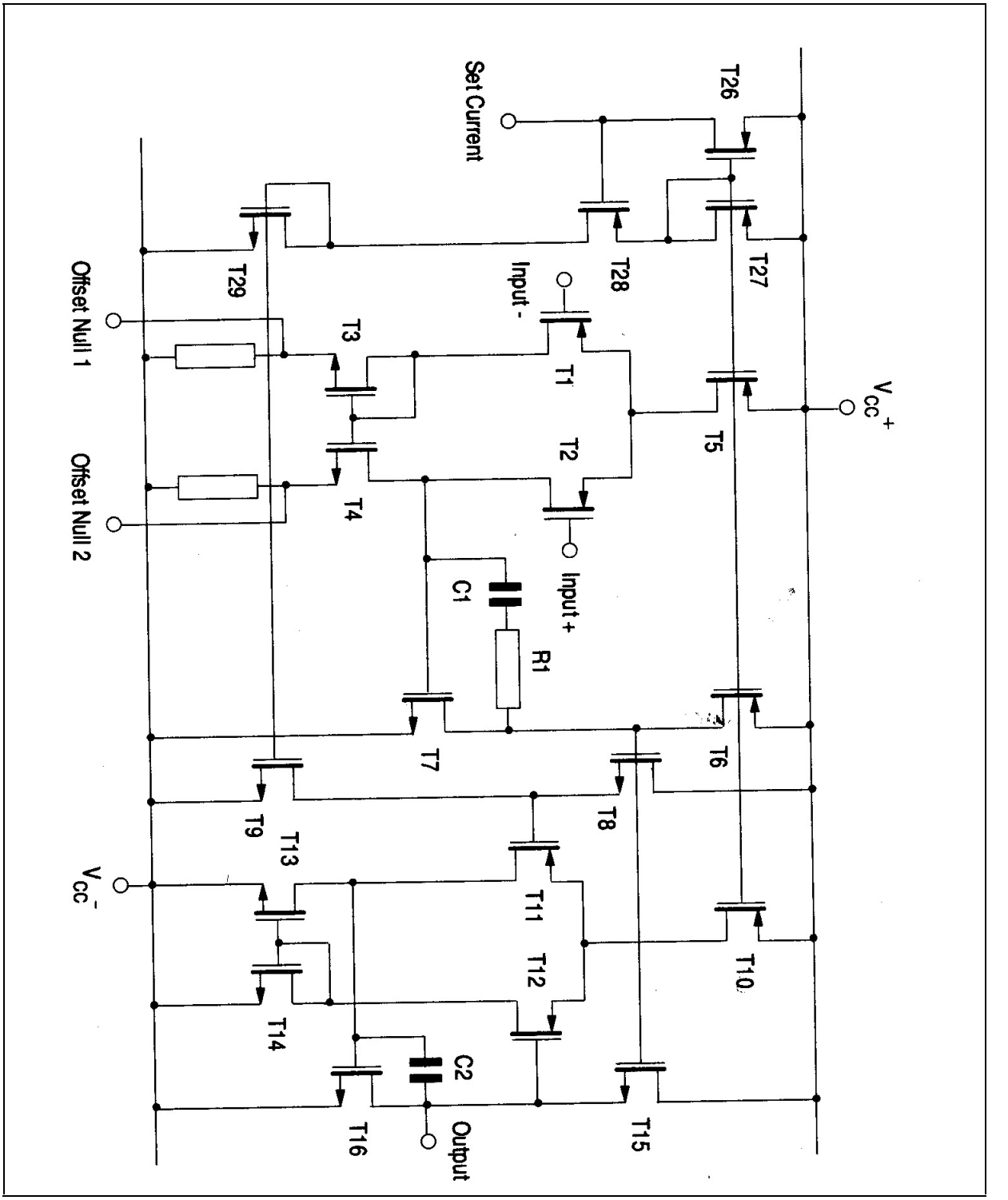
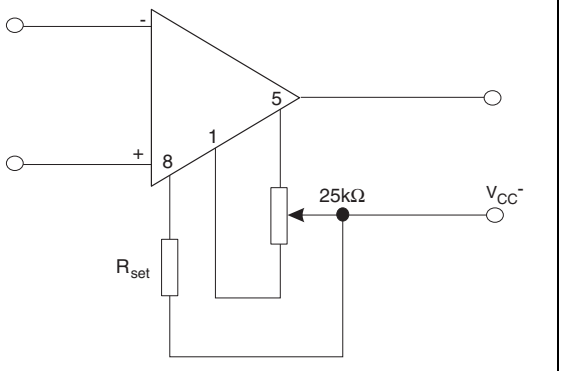
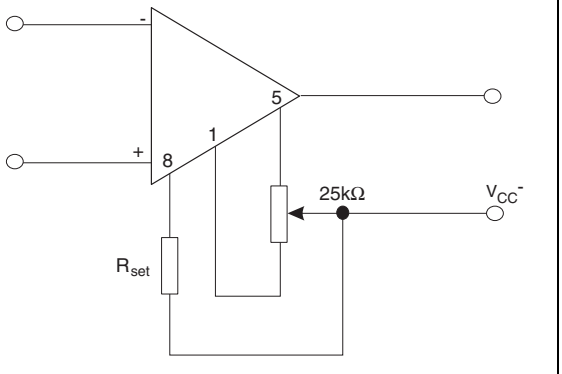


**Figure 3. Offset voltage null circuit**




OFFSET COMPENSATION GUARANTEED FOR
TS271BCX ($I_{SET}$ > 25µA), TS271ACX ($I_{SET}$ > 90µA)

**Figure 4. Offset voltage null circuit**




OFFSET COMPENSATION GUARANTEED FOR
TS271BCX ($I_{SET}$ > 25µA), TS271ACX ($I_{SET}$ > 90µA)

**Figure 5. Resistor biasing**

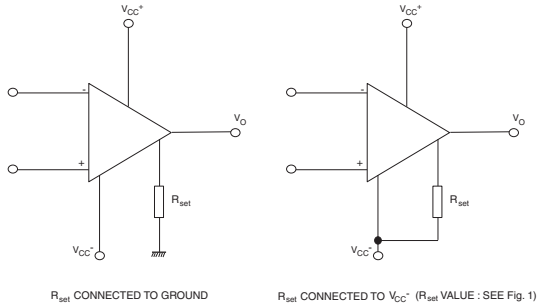
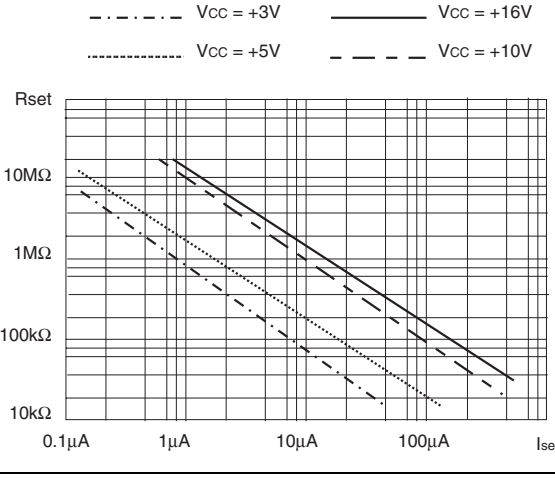



**Figure 6. Rset connected to Vcc-**



# 3 Electrical Characteristics

**Table 3. for $I_{SET}$ = 1.5µA - $V_{CC}^+$ = +10V, $V_{CC}^-$= 0V, $T_{amb}$ = +25°C (unless otherwise specified)**

| Symbol | Parameter | | TS271C/AC/BC | | | TS271I/AI/BI TS271M/AM/BM | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| $V_{io}$ | Input Offset Voltage<br>$V_O$ = 1.4V, $V_{ic}$ = 0V | TS271C/I/M<br>TS271AC/AI/AM<br>TS271BC/BI/BM | | 1.1<br>0.9<br>0.25 | 10<br>5<br>2 | | 1.1<br>0.9<br>0.25 | 10<br>5<br>2 | mV |
| | $T_{min} \le T_{amb} \le T_{max}$ | TS271C/I/M<br>TS271AC/AI/AM<br>TS271BC/BI/BM | | | 12<br>6.5<br>3 | | | 12<br>6.5<br>3.5 | |
| $DV_{io}$ | Input Offset Voltage Drift | | | 2 | | | 2 | | µV/°C |
| $I_{io}$ | Input Offset Current note [1]<br>$V_{ic}$ = 5V, $V_O$ = 5V | | | 1 | | | 1 | | pA |
| | $T_{min} \le T_{amb} \le T_{max}$ | | | | 100 | | | 200 | |
| $I_{ib}$ | Input Bias Current - see note 1<br>$V_{ic}$ = 5V, $V_O$ = 5V | | | 1 | | | 1 | | pA |
| | $T_{min} \le T_{amb} \le T_{max}$ | | | | 150 | | | 300 | |
| $V_{OH}$ | High Level Output Voltage<br>$V_{id}$ = 100mV, $R_L$ = 1MΩ | | 8.8 | 9 | | 8.8 | 9 | | V |
| | $T_{min} \le T_{amb} \le T_{max}$ | | 8.7 | | | 8.6 | | | |
| $V_{OL}$ | Low Level Output Voltage<br>$V_{id}$ = -100mV | | | | 50 | | | 50 | mV |
| $A_{vd}$ | Large Signal Voltage Gain<br>$V_{iC}$ = 5V, $R_L$ = 1MΩ, $V_o$ = 1V to 6V | | 30 | 100 | | 30 | 100 | | V/mV |
| | $T_{min} \le T_{amb} \le T_{max}$ | | 20 | | | 20 | | | |
| GBP | Gain Bandwidth Product<br>$A_v$ = 40dB, $R_L$ = 1MΩ, $C_L$ = 100pF, $f_{in}$ = 100kHz | | | 0.1 | | | 0.1 | | MHz |
| CMR | Common Mode Rejection Ratio<br>$V_{iC}$ = 1V to 7.4V, $V_o$ = 1.4V | | 60 | 80 | | 60 | 80 | | dB |
| SVR | Supply Voltage Rejection Ratio<br>$V_{CC}^+$ = 5V to 10V, $V_o$ = 1.4V | | 60 | 80 | | 60 | 80 | | dB |
| $I_{CC}$ | Supply Current (per amplifier)<br>$A_v$ = 1, no load, $V_o$ = 5V | | | 10 | 15 | | 10 | 15 | µA |
| | $T_{min} \le T_{amb} \le T_{max}$ | | | | 17 | | | 18 | |
| $I_o$ | Output Short Circuit Current<br>$V_o$ = 0V, $V_{id}$ = 100mV | | | 60 | | | 60 | | mA |
| $I_{sink}$ | Output Sink Current<br>$V_o$ = $V_{CC}$, $V_{id}$ = -100mV | | | 45 | | | 45 | | mA |
| SR | Slew Rate at Unity Gain<br>$R_L$ = 1MΩ, $C_L$ = 100pF, $V_i$ = 3 to 7V | | | 0.04 | | | 0.04 | | V/µs |
| $\phi m$ | Phase Margin at Unity Gain<br>$A_v$ = 40dB, $R_L$ = 1MΩ | $C_L$ = 10pF | | 35 | | | 35 | | Degrees |
| | | $C_L$ = 100pF | | 10 | | | 10 | | |
| $K_{OV}$ | Overshoot Factor<br>$A_v$ = 40dB, $R_L$ = 1MΩ | $C_L$ = 10pF | | 40 | | | 40 | | % |
| | | $C_L$ = 100pF | | 70 | | | 70 | | |
| $e_n$ | Equivalent Input Noise Voltage<br>f = 1kHz, $R_s$ = 100Ω | | | 30 | | | 30 | | $\frac{nV}{\sqrt{Hz}}$ |

1) Maximum values including unavoidable inaccuracies of the industrial test.

## Typical characteristics for $I_{SET}$ = 1.5µA

**Figure 7. Supply current versus supply voltage**

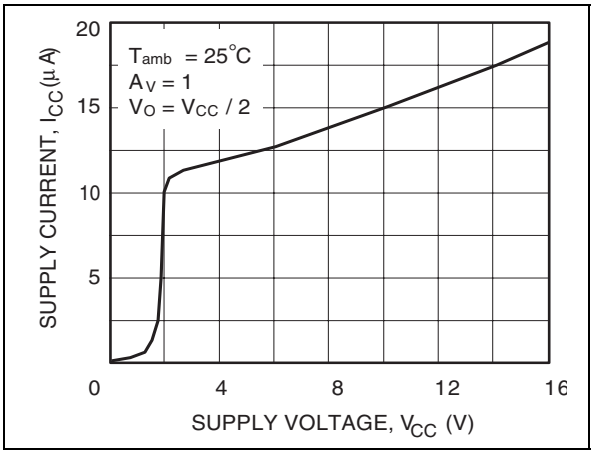



**Figure 8. Input bias current versus free air temperature**

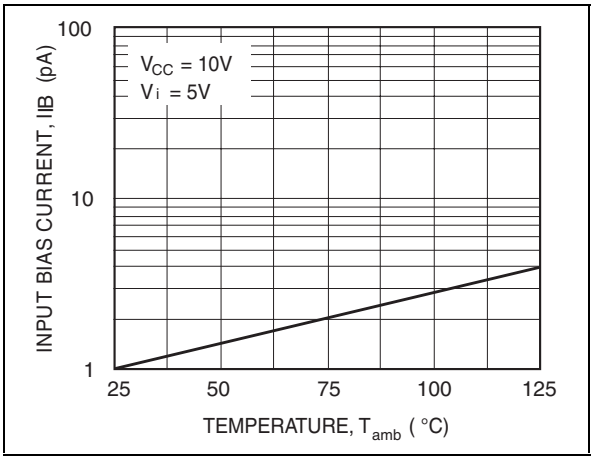



**Figure 9. High level output voltage versus high level output current**

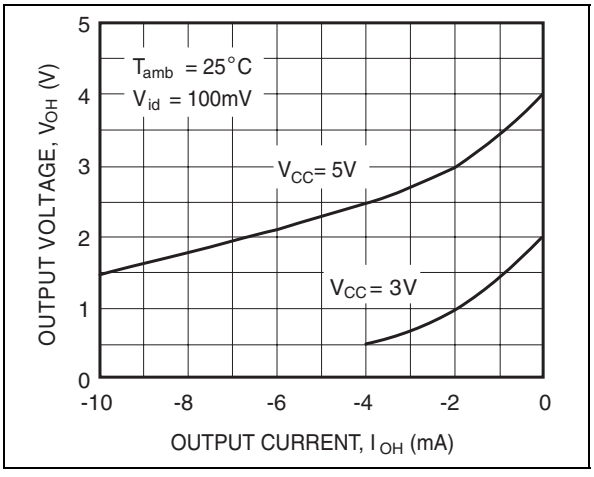



**Figure 10. High level output voltage versus high level output current**

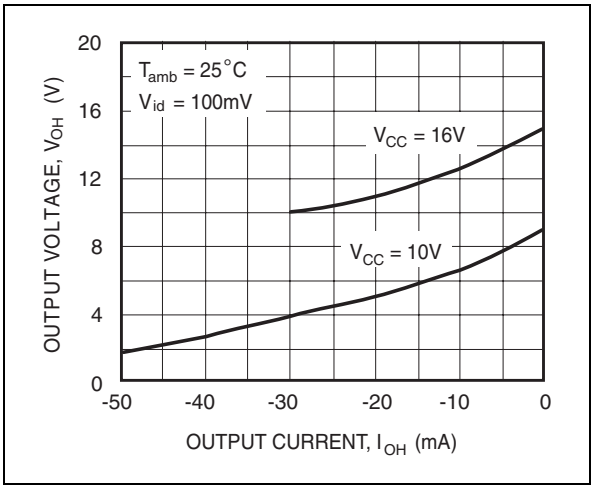



**Figure 11. Low level output voltage versus low level output current**

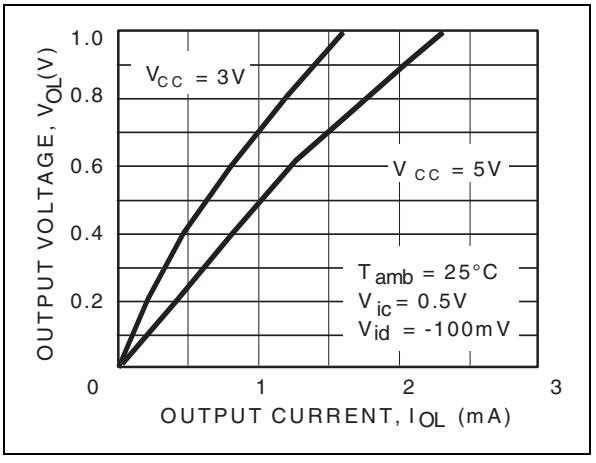



**Figure 12. Low level output voltage versus low level output current**

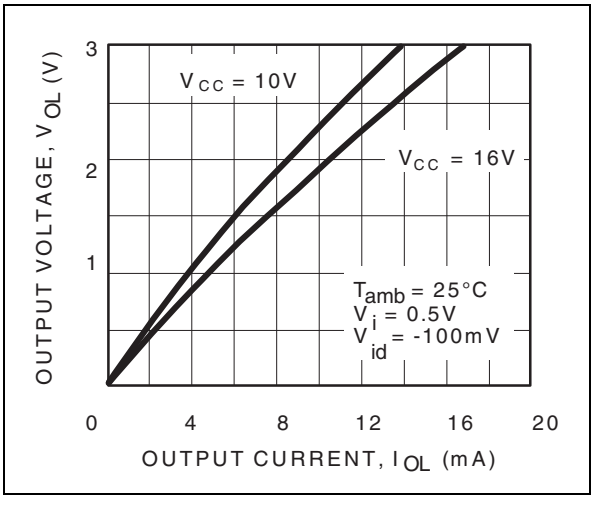


**Figure 13. Open loop frequency response and phase shift**

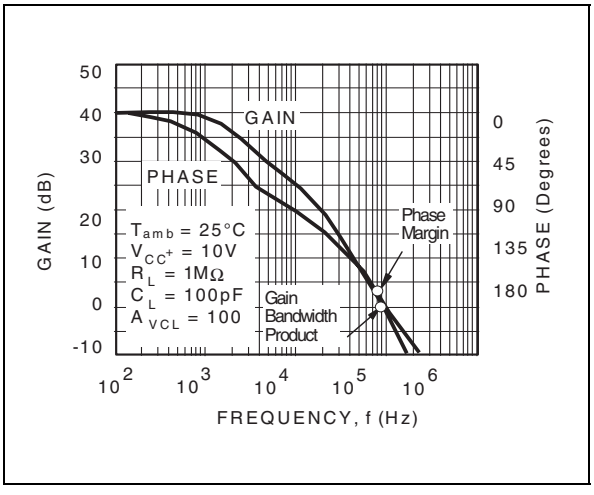



**Figure 14. Gain bandwidth product versus supply voltage**

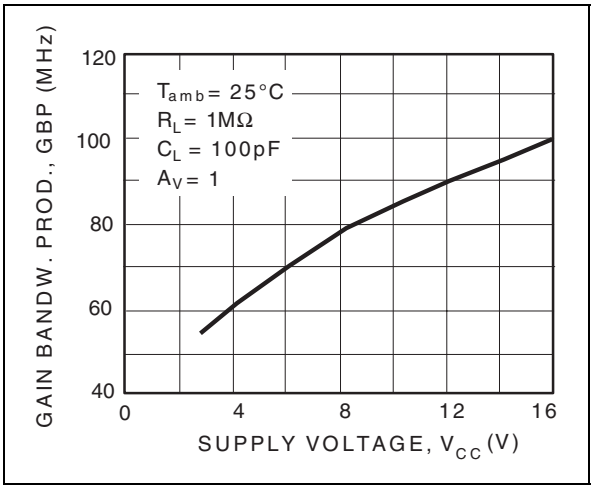



**Figure 15. Phase margin versus supply voltage**

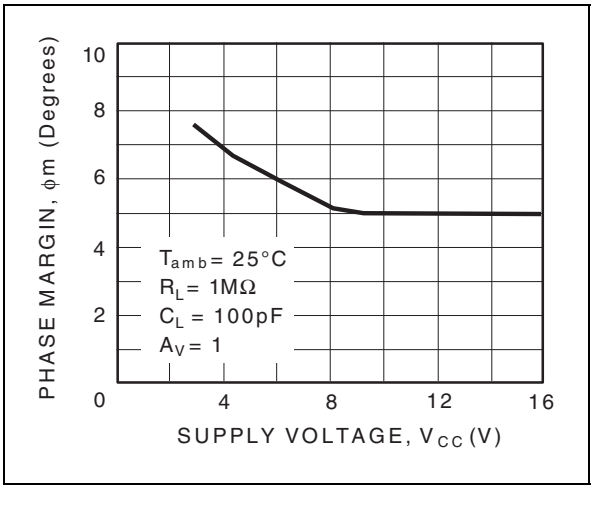



**Figure 16. Phase margin versus capacitive load**

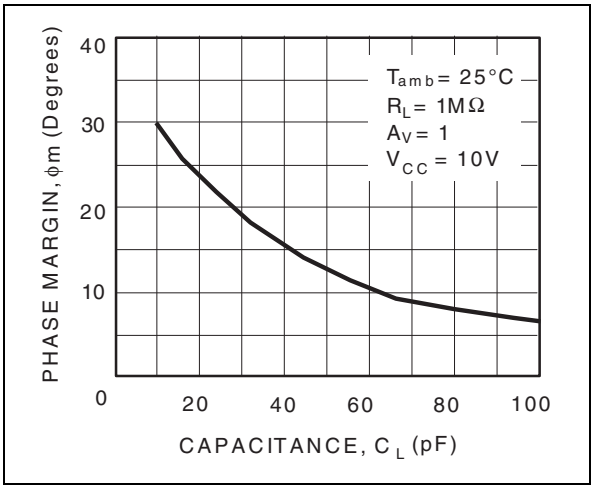
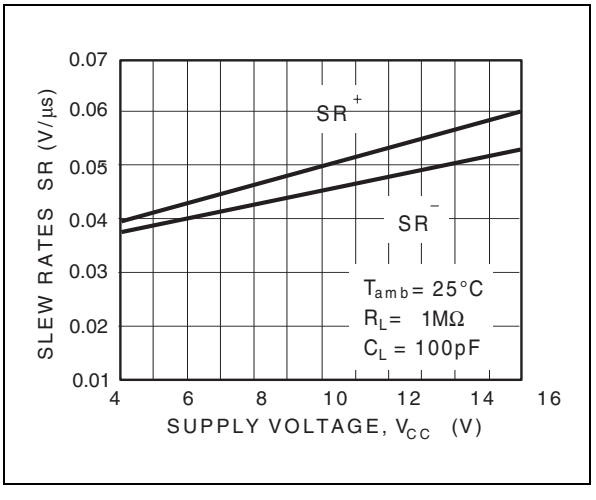



**Figure 17. Slew rate versus supply voltage**



# 4 Electrical Characteristics

**Table 4. for $I_{SET}$ = 25µA - $V_{CC}^+$ = +10V, $V_{CC}^-$= 0V, $T_{amb}$ = +25°C (unless otherwise specified)**

| Symbol | Parameter | | TS271C/AC/BC | | | TS271I/AI/BI TS271M/AM/BM | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| $V_{io}$ | Input Offset Voltage<br>$V_O$ = 1.4V, $V_{ic}$ = 0V | TS271C/I/M<br>TS271AC/AI/AM<br>TS271BC/BI/BM | | 1.1<br>0.9<br>0.25 | 10<br>5<br>2 | | 1.1<br>0.9<br>0.25 | 10<br>5<br>2 | mV |
| | $T_{min} \le T_{amb} \le T_{max}$ | TS271B/C/I/M<br>TS271AC/AI/AM<br>TS271BC/BI/BM | | | 12<br>6.5<br>3 | | | 12<br>6.5<br>3.5 | |
| $DV_{io}$ | Input Offset Voltage Drift | | | 2 | | | 2 | | µV/°C |
| $I_{io}$ | Input Offset Current note [1]<br>$V_{ic}$ = 5V, $V_O$ = 5V | | | 1 | | | 1 | | pA |
| | $T_{min} \le T_{amb} \le T_{max}$ | | | | 100 | | | 200 | |
| $I_{ib}$ | Input Bias Current - see note 1<br>$V_{ic}$ = 5V, $V_O$ = 5V | | | 1 | | | 1 | | pA |
| | $T_{min} \le T_{amb} \le T_{max}$ | | | | 150 | | | 300 | |
| $V_{OH}$ | High Level Output Voltage<br>$V_{id}$ = 100mV, $R_L$ = 100kΩ | | 8.7 | 8.9 | | 8.7 | 8.9 | | V |
| | $T_{min} \le T_{amb} \le T_{max}$ | | 8.6 | | | 8.5 | | | |
| $V_{OL}$ | Low Level Output Voltage<br>$V_{id}$ = -100mV | | | | 50 | | | 50 | mV |
| $A_{vd}$ | Large Signal Voltage Gain<br>$V_{iC}$ = 5V, $R_L$ = 100kΩ, $V_o$ = 1V to 6V | | 30 | 50 | | 30 | 50 | | V/mV |
| | $T_{min} \le T_{amb} \le T_{max}$ | | 20 | | | 10 | | | |
| GBP | Gain Bandwidth Product<br>$A_v$ = 40dB, $R_L$ = 100kΩ, $C_L$ = 100pF, $f_{in}$ = 100kHz | | | 0.7 | | | 0.7 | | MHz |
| CMR | Common Mode Rejection Ratio<br>$V_{iC}$ = 1V to 7.4V, $V_o$ = 1.4V | | 60 | 80 | | 60 | 80 | | dB |
| SVR | Supply Voltage Rejection Ratio<br>$V_{CC}^+$ = 5V to 10V, $V_o$ = 1.4V | | 60 | 80 | | 60 | 80 | | dB |
| $I_{CC}$ | Supply Current (per amplifier)<br>$A_v$ = 1, no load, $V_o$ = 5V | | | 150 | 200 | | 150 | 200 | µA |
| | $T_{min} \le T_{amb} \le T_{max}$ | | | | 250 | | | 300 | |
| $I_o$ | Output Short Circuit Current<br>$V_o$ = 0V, $V_{id}$ = 100mV | | | 60 | | | 60 | | mA |
| $I_{sink}$ | Output Sink Current<br>$V_o$ = $V_{CC}$, $V_{id}$ = -100mV | | | 45 | | | 45 | | mA |
| SR | Slew Rate at Unity Gain<br>$R_L$ = 100kΩ, $C_L$ = 100pF, $V_i$ = 3 to 7V | | | 0.6 | | | 0.6 | | V/µs |
| $\phi m$ | Phase Margin at Unity Gain<br>$A_v$ = 40dB, $R_L$ = 100kΩ | $C_L$ = 10pF | | 50 | | | 50 | | Degrees |
| | | $C_L$ = 100pF | | 30 | | | 30 | | |
| $K_{OV}$ | Overshoot Factor<br>$A_v$ = 40dB, $R_L$ = 100kΩ | $C_L$ = 10pF | | 30 | | | 30 | | % |
| | | $C_L$ = 100pF | | 50 | | | 50 | | |
| $e_n$ | Equivalent Input Noise Voltage<br>f = 1kHz, $R_s$ = 100Ω | | | 38 | | | 38 | | $\frac{nV}{\sqrt{Hz}}$ |

1) Maximum values including unavoidable inaccuracies of the industrial test.

## Typical characteristics for $I_{SET}$ = 25µA

**Figure 18. Supply current versus supply voltage**

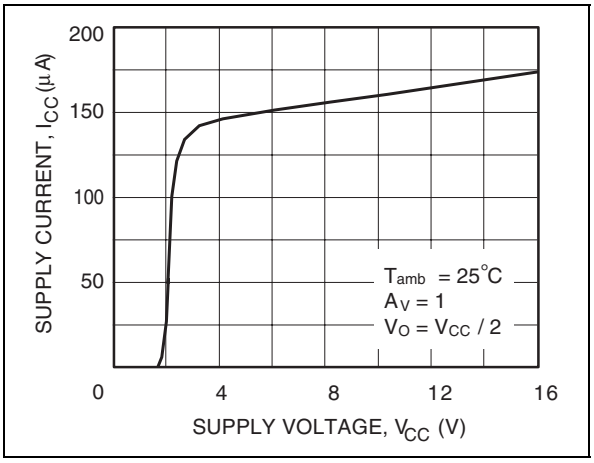



**Figure 19. Input bias current versus free air temperature**

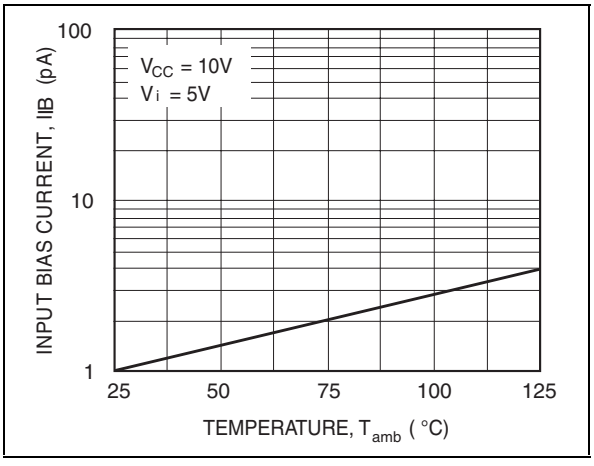



**Figure 20. High level output voltage versus high level output current**

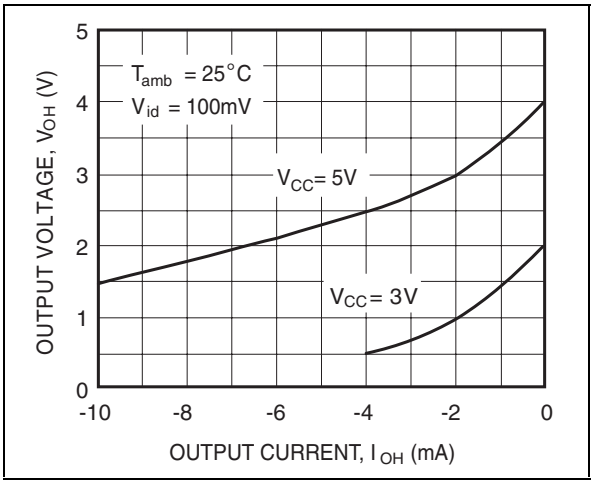



**Figure 21. High level output voltage versus high level output current**

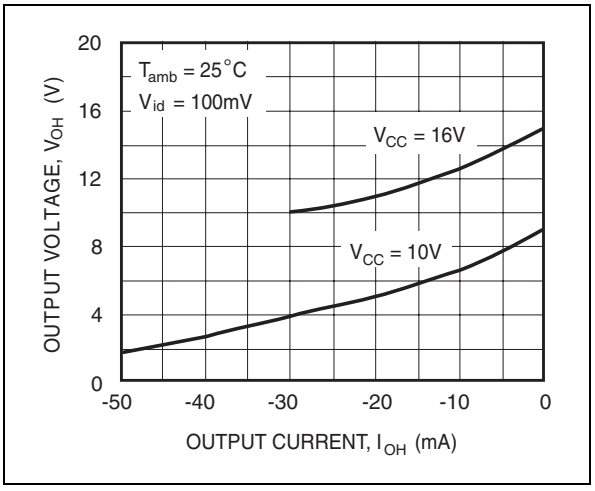



**Figure 22. Low level output voltage versus low level output current**

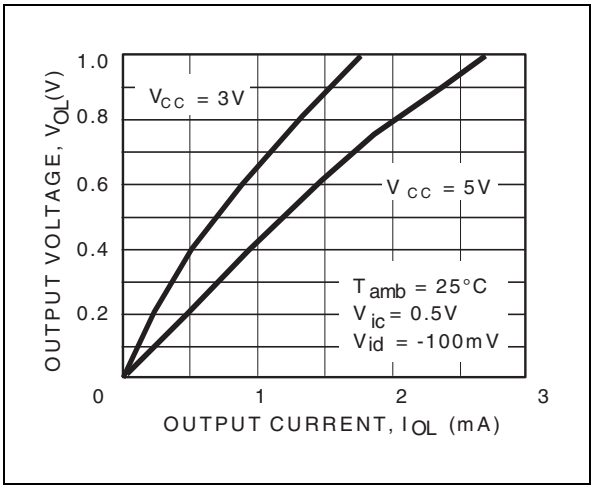



**Figure 23. Low level output voltage versus low level output current**

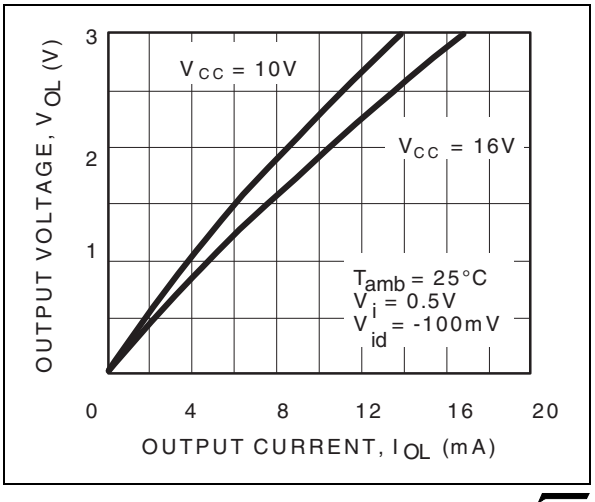


**Figure 24. Open loop frequency response and phase shift**

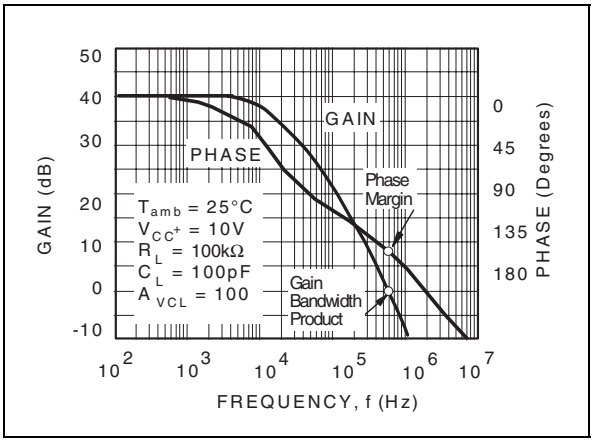



**Figure 25. Gain bandwidth product versus supply voltage**

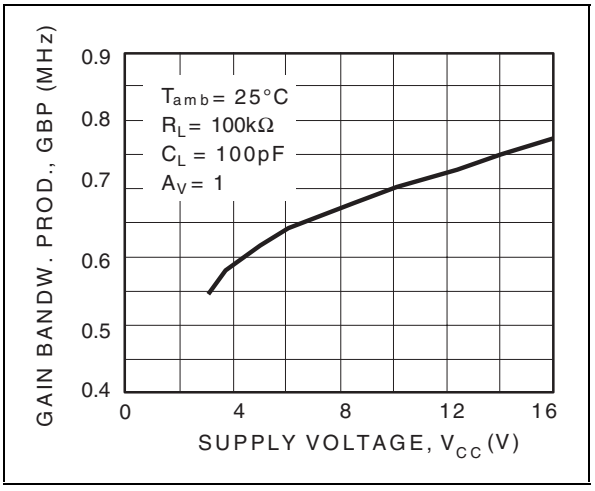



**Figure 26. Phase margin versus supply voltage**

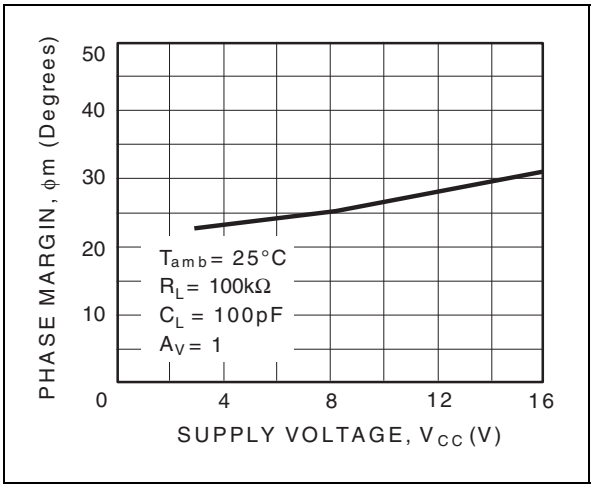



**Figure 27. Phase margin versus capacitive load**

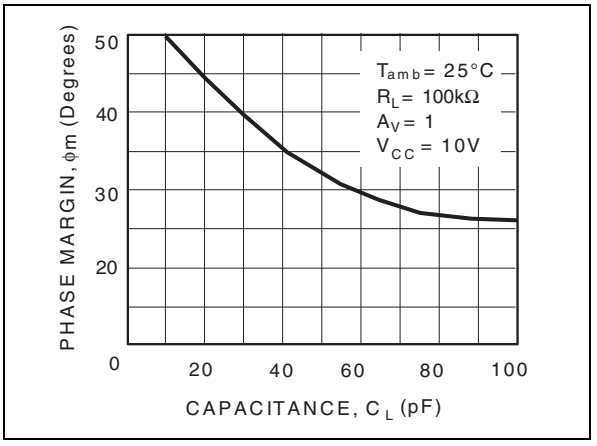
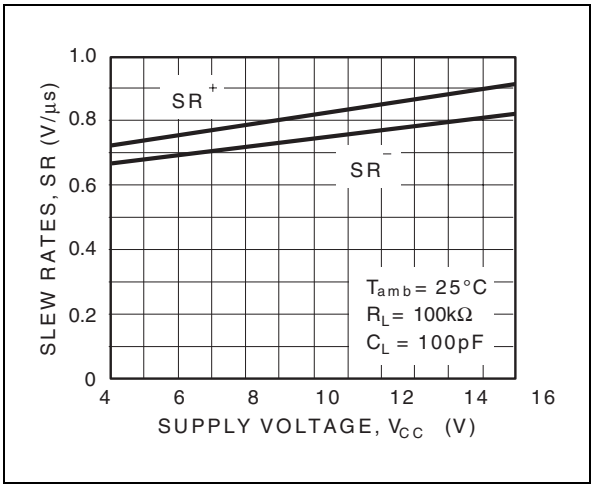



**Figure 28. Slew rate versus supply voltage**



# 5 Electrical Characteristics

**Table 5. for $I_{SET}$ = 130µA - $V_{CC}^+$ = +10V, $V_{CC}^-$= 0V, $T_{amb}$ = +25°C (unless otherwise specified)**

| Symbol | Parameter | | TS271C/AC/BC | | | TS271I/AI/BI TS271M/AM/BM | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| $V_{io}$ | Input Offset Voltage<br>$V_O$ = 1.4V, $V_{ic}$ = 0V | TS271C/I/M<br>TS271AC/AI/AM<br>TS271BC/BI/BM | | 1.1<br>0.9<br>0.25 | 10<br>5<br>2 | | 1.1<br>0.9<br>0.25 | 10<br>5<br>2 | mV |
| | $T_{min} \le T_{amb} \le T_{max}$ | TS271B/C/I/M<br>TS271AC/AI/AM<br>TS271BC/BI/BM | | | 12<br>6.5<br>3 | | | 12<br>6.5<br>3.5 | |
| $DV_{io}$ | Input Offset Voltage Drift | | | 2 | | | 2 | | µV/°C |
| $I_{io}$ | Input Offset Current note [1]<br>$V_{ic}$ = 5V, $V_O$ = 5V | | | 1 | | | 1 | | pA |
| | $T_{min} \le T_{amb} \le T_{max}$ | | | | 100 | | | 200 | |
| $I_{ib}$ | Input Bias Current - see note 1<br>$V_{ic}$ = 5V, $V_O$ = 5V | | | 1 | | | 1 | | pA |
| | $T_{min} \le T_{amb} \le T_{max}$ | | | | 150 | | | 300 | |
| $V_{OH}$ | High Level Output Voltage<br>$V_{id}$ = 100mV, $R_L$ = 10kΩ | | 8.2 | 8.4 | | 8.2 | 8.4 | | V |
| | $T_{min} \le T_{amb} \le T_{max}$ | | 8.1 | | | 8 | | | |
| $V_{OL}$ | Low Level Output Voltage<br>$V_{id}$ = -100mV | | | | 50 | | | 50 | mV |
| $A_{vd}$ | Large Signal Voltage Gain<br>$V_{iC}$ = 5V, $R_L$ = 10kΩ, $V_o$ = 1V to 6V | | 10 | 15 | | 10 | 15 | | V/mV |
| | $T_{min} \le T_{amb} \le T_{max}$ | | 7 | | | 6 | | | |
| GBP | Gain Bandwidth Product<br>$A_v$ = 40dB, $R_L$ = 10kΩ, $C_L$ = 100pF, $f_{in}$ = 100kHz | | | 2.3 | | | 2.3 | | MHz |
| CMR | Common Mode Rejection Ratio<br>$V_{iC}$ = 1V to 7.4V, $V_o$ = 1.4V | | 60 | 80 | | 60 | 80 | | dB |
| SVR | Supply Voltage Rejection Ratio<br>$V_{CC}^+$ = 5V to 10V, $V_o$ = 1.4V | | 60 | 70 | | 60 | 70 | | dB |
| $I_{CC}$ | Supply Current (per amplifier)<br>$A_v$ = 1, no load, $V_o$ = 5V | | | 800 | 1300 | | 800 | 1300 | µA |
| | $T_{min} \le T_{amb} \le T_{max}$ | | | | 1400 | | | 1500 | |
| $I_o$ | Output Short Circuit Current<br>$V_o$ = 0V, $V_{id}$ = 100mV | | | 60 | | | 60 | | mA |
| $I_{sink}$ | Output Sink Current<br>$V_o$ = $V_{CC}$, $V_{id}$ = -100mV | | | 45 | | | 45 | | mA |
| SR | Slew Rate at Unity Gain<br>$R_L$ = 10kΩ, $C_L$ = 100pF, $V_i$ = 3 to 7V | | | 4.5 | | | 4.5 | | V/µs |
| $\phi m$ | Phase Margin at Unity Gain<br>$A_v$ = 40dB, $R_L$ = 10kΩ | $C_L$ = 10pF | | 65 | | | 65 | | Degrees |
| | | $C_L$ = 100pF | | 30 | | | 30 | | |
| $K_{OV}$ | Overshoot Factor<br>$A_v$ = 40dB, $R_L$ = 10kΩ | $C_L$ = 10pF | | 30 | | | 30 | | % |
| | | $C_L$ = 100pF | | 50 | | | 50 | | |
| $e_n$ | Equivalent Input Noise Voltage<br>f = 1kHz, $R_s$ = 100Ω | | | 30 | | | 30 | | $\frac{nV}{\sqrt{Hz}}$ |

1) Maximum values including unavoidable inaccuracies of the industrial test.

## Typical characteristics for $I_{SET}$ = 130µA

**Figure 29. Supply current (each amplifier) versus supply voltage**

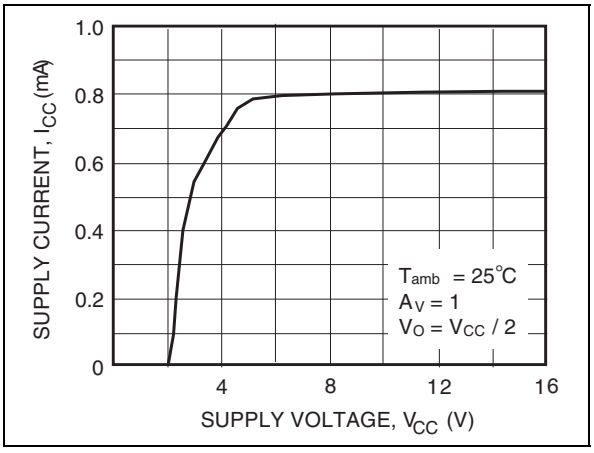



**Figure 30. Input bias current versus free air temperature**

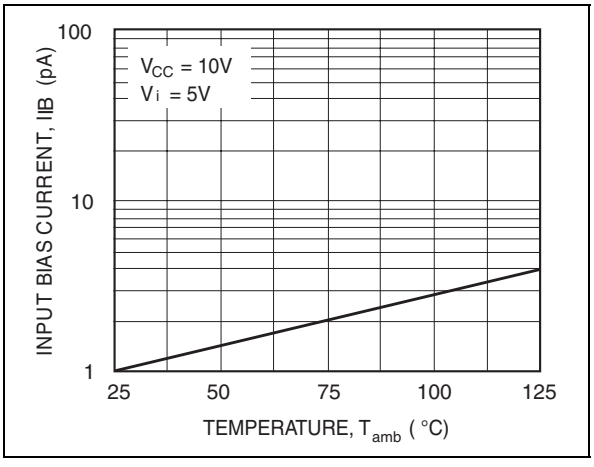



**Figure 31. High level output voltage versus high level output current**

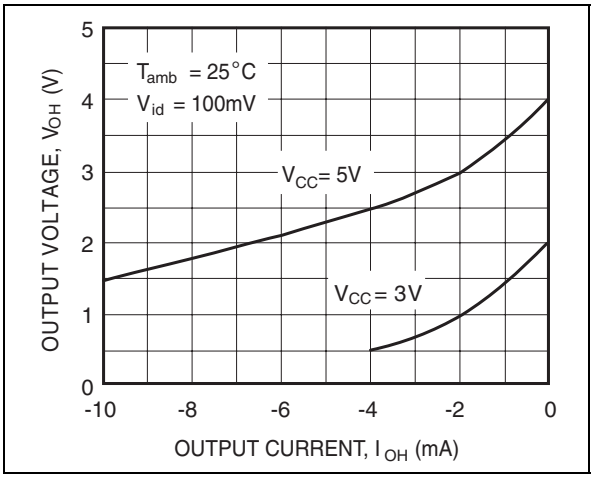



**Figure 32. High level output voltage versus high level output current**

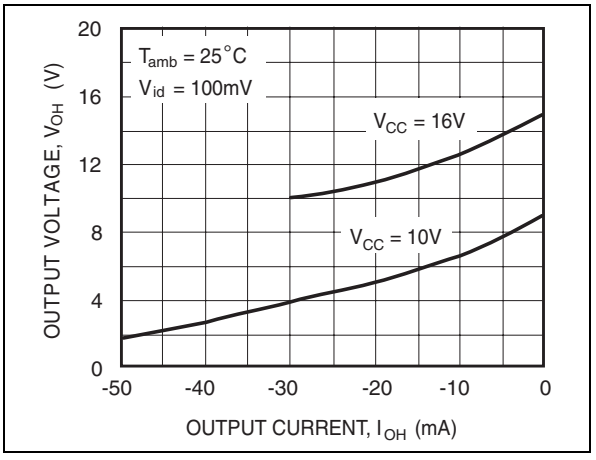



**Figure 33. Low level output voltage versus low level output current**

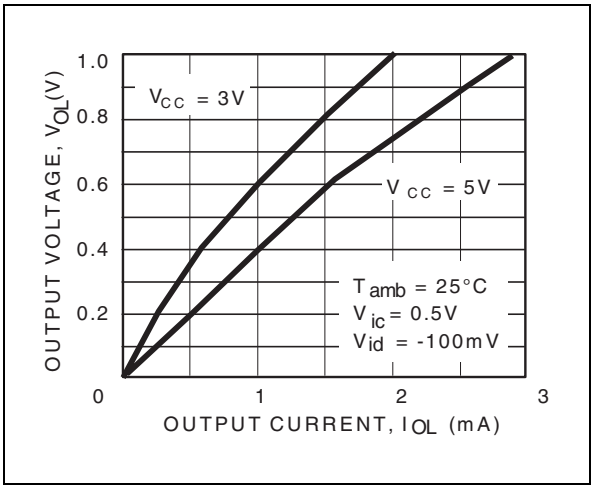



**Figure 34. Low level output voltage versus low level output current**

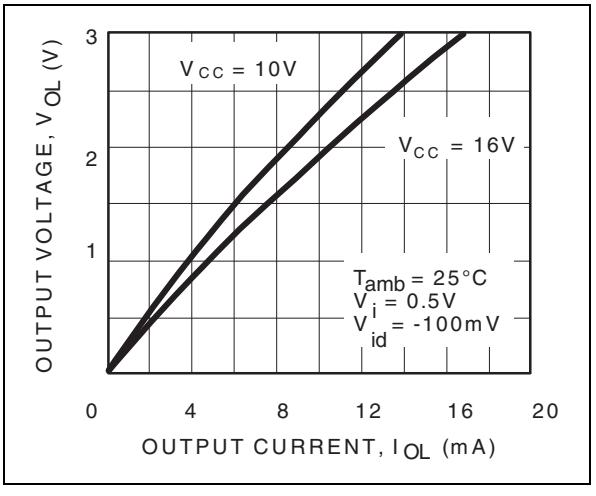


**Figure 35. Open loop frequency response and phase shift**

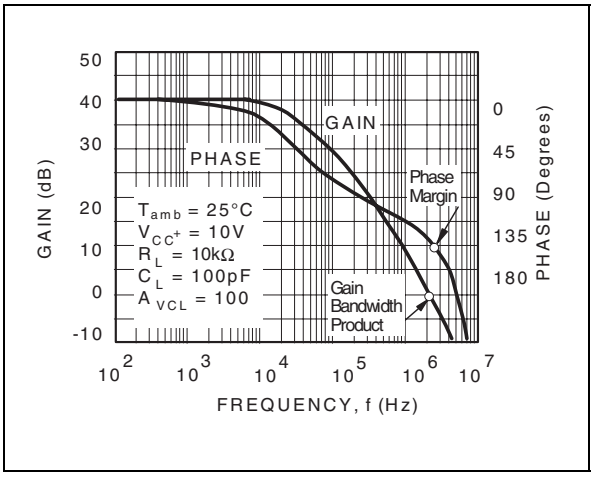



**Figure 36. Gain bandwidth product versus supply voltage**

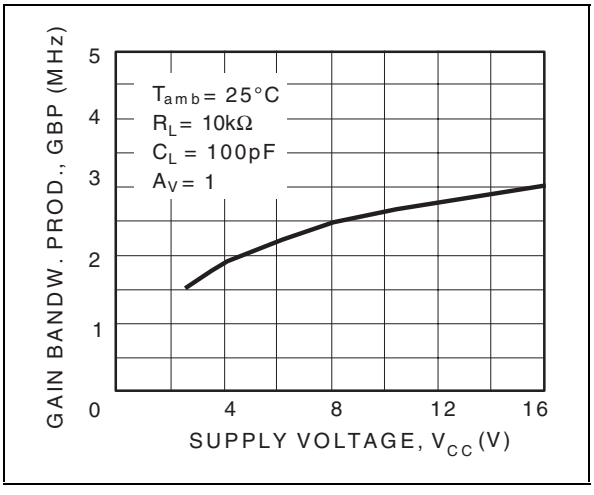



**Figure 37. Phase margin versus supply voltage**

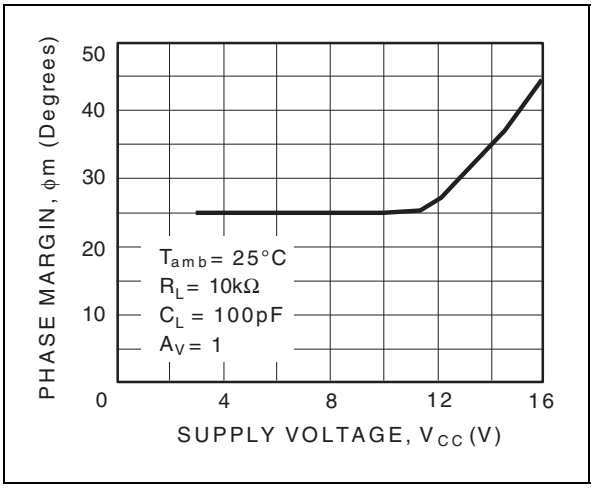



**Figure 38. Phase margin versus capacitive load**

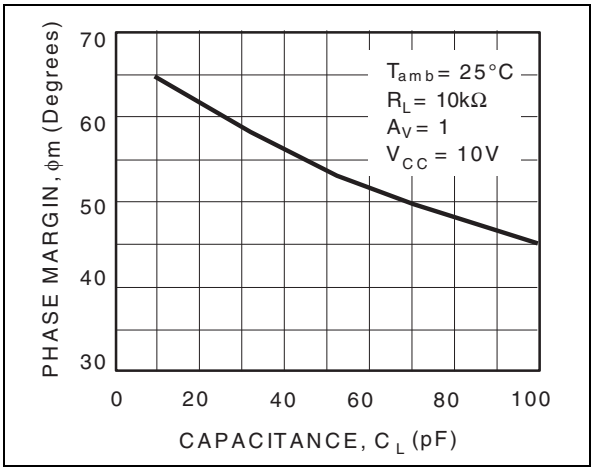
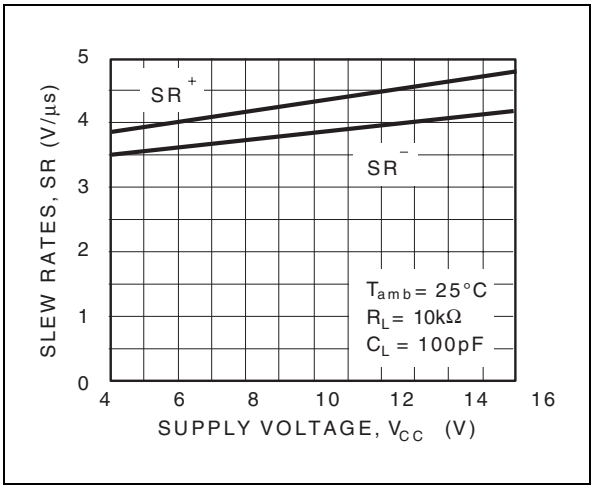


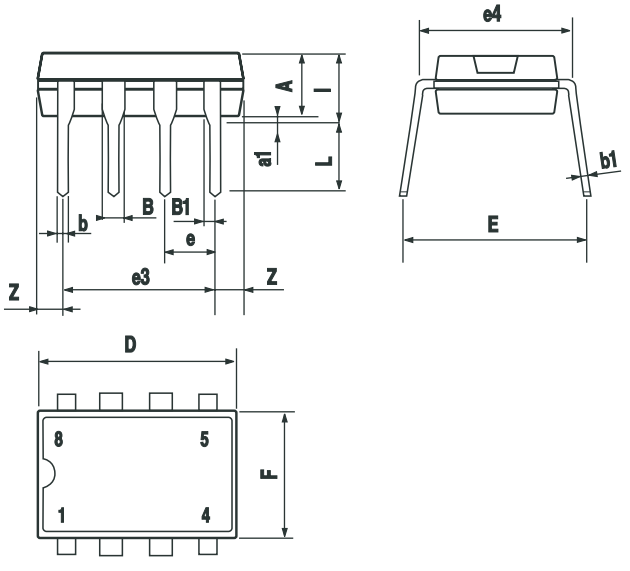

**Figure 39. Slew rate versus supply voltage**



# 6 Package Mechanical Data

**Plastic DIP-8 MECHANICAL DATA**

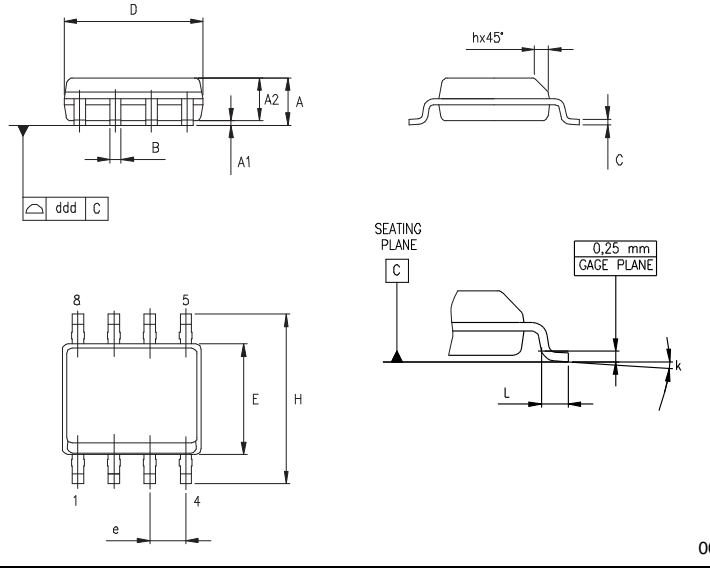
| DIM. | mm. | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | | 3.3 | | | 0.130 | |
| a1 | 0.7 | | | 0.028 | | |
| B | 1.39 | | 1.65 | 0.055 | | 0.065 |
| B1 | 0.91 | | 1.04 | 0.036 | | 0.041 |
| b | | 0.5 | | | 0.020 | |
| b1 | 0.38 | | 0.5 | 0.015 | | 0.020 |
| D | | | 9.8 | | | 0.386 |
| E | | 8.8 | | | 0.346 | |
| e | | 2.54 | | | 0.100 | |
| e3 | | 7.62 | | | 0.300 | |
| e4 | | 7.62 | | | 0.300 | |
| F | | | 7.1 | | | 0.280 |
| I | | | 4.8 | | | 0.189 |
| L | | 3.3 | | | 0.130 | |
| Z | 0.44 | | 1.6 | 0.017 | | 0.063 |




P001F

# Package Mechanical Data

| SO-8 MECHANICAL DATA | | | | | | |
|---|---|---|---|---|---|---|
| DIM. | mm. | | | inch | | |
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | 1.35 | | 1.75 | 0.053 | | 0.069 |
| A1 | 0.10 | | 0.25 | 0.04 | | 0.010 |
| A2 | 1.10 | | 1.65 | 0.043 | | 0.065 |
| B | 0.33 | | 0.51 | 0.013 | | 0.020 |
| C | 0.19 | | 0.25 | 0.007 | | 0.010 |
| D | 4.80 | | 5.00 | 0.189 | | 0.197 |
| E | 3.80 | | 4.00 | 0.150 | | 0.157 |
| e | | 1.27 | | | 0.050 | |
| H | 5.80 | | 6.20 | 0.228 | | 0.244 |
| h | 0.25 | | 0.50 | 0.010 | | 0.020 |
| L | 0.40 | | 1.27 | 0.016 | | 0.050 |
| k | 8° (max.) | | | | | |
| ddd | | | 0.1 | | | 0.04 |



# 7 Revision History

| Date | Revision | Description of Changes |
|---|---|---|
| 01 Nov. 2001 | 1 | First Release |
| 01 March 2005 | 2 | • Application block diagram updated on *Figure 2 on page 4*<br>• Schematic Diagram updated on *Figure 4 on page 5* |