# TMS320F28032, TMS320F28033, TMS320F28034, TMS320F28035 Piccolo MCU

# Silicon Errata

Literature Number: SPRZ295A
April 2009–Revised May 2009

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# TMS320F2803x Piccolo MCU Silicon Errata

## 1 Introduction

This document describes the silicon updates to the functional specifications for the TMS320F2803x microcontrollers (MCUs).

The updates are applicable to:

- 64-pin Plastic Small-Outline Package, PAG Suffix
- 80-pin Plastic Quad Flatpack, PN Suffix

## 2 Device and Development Tool Support Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all [TMS320] DSP devices and support tools. Each TMS320™ DSP commercial family member has one of three prefixes: TMX, TMP, or TMS (e.g., **TMS**320F28035). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX/TMDX) through fully qualified production devices/tools (TMS/TMDS).

**TMX** Experimental device that is not necessarily representative of the final device's electrical specifications

**TMP** Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification

**TMS** Fully qualified production device

Support tool development evolutionary flow:

**TMDX** Development-support product that has not yet completed Texas Instruments internal qualification testing

**TMDS** Fully qualified development-support product

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:
"Developmental product is intended for internal evaluation purposes."

TMS devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, PN) and temperature range (for example, T).

## 3 Device Markings

Figure 1 provides an example of the 2803x device markings and defines each of the markings. The device revision can be determined by the symbols marked on the top of the package as shown in Figure 1. Some prototype devices may have markings different from those illustrated. Figure 2 shows an example of the device nomenclature.

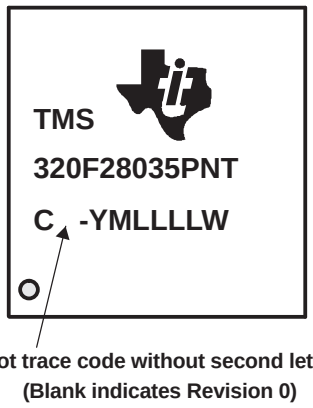


**Figure 1. Example of Device Markings**

**Table 1. Determining Silicon Revision From Lot Trace Code (2803x devices)**

| SECOND LETTER IN PREFIX OF LOT TRACE CODE | SILICON REVISION | REVISION ID (0x0883) | COMMENTS |
|---|---|---|---|
| Blank (no second letter in prefix) | Indicates Revision 0 | 0x0000 | This silicon revision is available as TMX. |

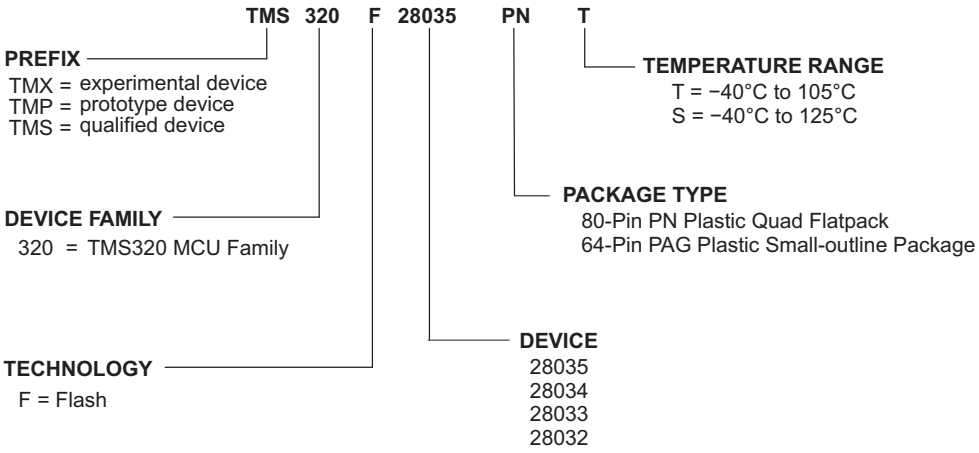


**Figure 2. Example of Device Nomenclature**

# 4 Rev 0 Known Design Marginality/Exceptions to Functional Specifications

**Table 2. Advisory List for Rev 0 Silicon**

## Advisory — *ADC: Initial Conversion*

**Revision(s) Affected** 0

**Details** When the ADC conversions are initiated by any source of trigger, the first sample may not be the correct conversion result.

**Workaround(s)** Discard the first sample at the beginning of every series of conversions. For instance, if the application calls for a given series of conversions, SOC0→SOC1→SOC2, to initiate periodically, then setup the series instead as SOC0→SOC1→SOC2→SOC3 and only use the last three conversions, ADCRESULT1, ADCRESULT2, ADCRESULT3, thereby discarding ADCRESULT0.

Each application should validate this as acceptable in their application.

## Advisory — *Memory: Prefetching Beyond Valid Memory*

**Revision(s) Affected** 0

**Details** The C28x CPU prefetches instructions beyond those currently active in its pipeline. If the prefetch occurs past the end of valid memory, then the CPU may receive an invalid opcode.

**Workaround** The prefetch queue is 8 x16 words in depth. Therefore, code should not come within 8 words of the end of valid memory. This restriction applies to all memory regions and all memory types (flash, OTP, SARAM) on the device. Prefetching across the boundary between two valid memory blocks is all right.

Example 1: M1 ends at address 0x7FF and is not followed by another memory block. Code in M1 should be stored no farther than address 0x7F7. Addresses 0x7F8-0x7FF should not be used for code.

Example 2: M0 ends at address 0x3FF and valid memory (M1) follows it. Code in M0 can be stored up to and including address 0x3FF. Code can also cross into M1 up to and including address 0x7F7.

## Advisory — *eCAN: Abort Acknowledge Bit Not Set*

**Revision(s) Affected**

0

**Details**

After setting a Transmission Request Reset (TRR) register bit to abort a message, there are some rare instances where the TRRn and TRSn bits will clear without setting the Abort Acknowledge (AAn) bit. The transmission itself is correctly aborted, but no interrupt is asserted and there is no indication of a pending operation.

In order for this rare condition to occur, all of the following conditions must happen:

1. The previous message was not successful, either because of lost arbitration or because no node on the bus was able to acknowledge it or because an error frame resulted from the transmission. The previous message need not be from the same mailbox in which a transmit abort is currently being attempted.
2. The TRRn bit of the mailbox should be set in a CPU cycle immediately following the cycle in which the TRSn bit was set. The TRSn bit remaining set due to incompletion of transmission satisfies this condition as well. i.e. the TRSn bit could have been set in the past, but the transmission remains incomplete.
3. The TRRn bit must be set in the exact SYSCLKOUT cycle where the CAN module is in idle state for one cycle. The CAN module is said to be in idle state when it is not in the process of receiving/transmitting data.

If these conditions occur, then the TRRn and TRSn bits for the mailbox will clear $t_{clr}$ SYSCLKOUT cycles after the TRR bit is set where:

$$t_{clr} = [(\text{mailbox\_number}) * 2] + 3 \text{ SYSCLKOUT cycles}$$

The TAn and AAn bits will not be set if this condition occurs. Normally, either the TA or AA bit sets after the TRR bit goes to zero.

**Workaround(s)**

When this problem occurs, the TRRn and TRSn bits will clear within $t_{clr}$ SYSCLKOUT cycles. To check for this condition, first disable the interrupts. Check the TRRn bit $t_{clr}$ SYSCLKOUT cycles after setting the TRRn bit to make sure it is still set. A set TRRn bit indicates that the problem did not occur.

If the TRRn bit is cleared, it could be because of the normal end of a message and the corresponding TAn or AAn bit is set. Check both the TAn and AAn bits. If either one of the bits is set, then the problem did not occur. If they are both zero, then the problem did occur. Handle the condition like the interrupt service routine would except that the AAn bit does not need clearing now.

If the TAn or AAn bit is set, then the normal interrupt routine will happen when the interrupt is re-enabled.

## Advisory — *GPIO: GPIO Qualification*

**Revision(s) Affected** 0

**Details** If a GPIO pin is configured for "n" SYSCLKOUT cycle qualification period (where $1 \leq n \leq 510$) with "m" qualification samples (m = 3 or 6), it is possible that an input pulse of [n * m – (n – 1)] width may get qualified (instead of n * m). This depends upon the alignment of the asynchronous GPIO input signal with respect to the phase of the internal prescaled clock, and hence, is not deterministic. The probability of this kind of wrong qualification occurring is "1/n".

**Worst-case example:**

If n = 510, m = 6, a GPIO input width of (n * m) = 3060 SYSCLKOUT cycles is required to pass qualification. However, because of the issue described in this advisory, the minimum GPIO input width which may get qualified is [n * m – (n – 1)] = 3060 – 511 = 2549 SYSCLKOUT cycles.

**Workaround(s)** None. Ensure a sufficient margin is in the design for input qualification.

## Advisory — *Code Security Module: Memory Access Conflicts With Code Security Module (CSM) PWL Registers*

**Revision(s) Affected** 0

**Details** Reads of addresses 0x3D 7FF8–0x3D 7FFF will activate the CSM, locking the device.

**Workaround(s)** Do not read these addresses. If these addresses are read, causing the CSM to become active, the device can be unlocked either by first pulling reset or by setting the FORCESEC bit, and then performing the Password Match Flow described in the *TMS320x2803x Piccolo System Control and Interrupts Reference Guide* (literature number SPRUGL8).

**Note:** For TMS320F2803x devices, the PARTID register is located at 0x3D 7E80 (and not at 0x3D 7FFF, as on the TMS320F2802x devices).

# 5 Documentation Support

For device-specific data sheets and related documentation, visit the TI web site at: http://www.ti.com.

For further information regarding the Piccolo devices, see the *TMS320F28032, TMS320F28033, TMS320F28034, TMS320F28035 Piccolo Microcontrollers Data Manual* (literature number SPRS584).

# 6 Revision History

This revision history highlights the technical changes made to the SPRZ295 errata document to make it an SPRZ295A revision.

**Scope:** Added the "eCAN: Abort Acknowledge Bit Not Set" advisory.

Added the "Code Security Module: Memory Access Conflicts With Code Security Module (CSM) PWL Registers" advisory.

See table below.

| LOCATION | ADDITIONS, DELETIONS, AND MODIFICATIONS |
|---|---|
| Section 4 | Rev 0 Known Design Marginality/Exceptions to Functional Specifications:<br>• Removed the "CPU: PCLKCR0[14] Setting May Stall CPU" advisory<br>• Added the "eCAN: Abort Acknowledge Bit Not Set" advisory<br>• Added the "Code Security Module: Memory Access Conflicts With Code Security Module (CSM) PWL Registers" advisory |
| Section 5 | Documentation Support:<br>• Added link to SPRS584 |

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