# 2.7-V TO 5.5-V 10-BIT 3-μS QUADRUPLE DIGITAL-TO-ANALOG CONVERTERS

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- Four 10-Bit D/A Converters
- **Programmable Settling Time** of 3 μs or 9 μs Typ
- TMS320, (Q)SPI™, and Microwire™ Compatible Serial Interface
- **Internal Power-On Reset**
- **Low Power Consumption:**

5.5 mW, Slow Mode - 5-V Supply 3.3 mW, Slow Mode - 3-V Supply

- **Reference Input Buffers**
- **Voltage Output Range . . . 2× the Reference Input Voltage**
- **Monotonic Over Temperature**
- Dual 2.7-V to 5.5-V Supply (Separate Digital and Analog Supplies)

#### description

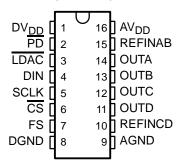
The TLV5604 is a quadruple 10-bit voltage output digital-to-analog converter (DAC) with a flexible 4-wire serial interface. The 4-wire serial interface allows glueless interface to TMS320, SPI, QSPI, and Microwire serial ports. The TLV5604 is programmed with a 16-bit serial word comprised of a DAC address, individual DAC control bits, and a 10-bit DAC value.

- Hardware Power Down (10 nA)
- Software Power Down (10 nA)
- Simultaneous Update

#### applications

- **Battery Powered Test Instruments**
- **Digital Offset and Gain Adjustment**
- **Industrial Process Controls**
- **Machine and Motion Control Devices**
- Communications
- **Arbitrary Waveform Generation**

#### D OR PW PACKAGE (TOP VIEW)



The device has provision for two supplies: one digital supply for the serial interface (via pins DV<sub>DD</sub> and DGND), and one for the DACs, reference buffers and output buffers (via pins AVDD and AGND). Each supply is independent of the other, and can be any value between 2.7 V and 5.5 V. The dual supplies allow a typical application where the DAC will be controlled via a microprocessor operating on a 3-V supply (also used on pins DV<sub>DD</sub> and DGND), with the DACs operating on a 5-V supply. Of course, the digital and analog supplies can be tied together.

The resistor string output voltage is buffered by a x2 gain rail-to-rail output buffer. The buffer features a Class AB output stage to improve stability and reduce settling time. A rail-to-rail output stage and a power-down mode makes it ideal for single voltage, battery based applications. The settling time of the DAC is programmable to allow the designer to optimize speed versus power dissipation. The settling time is chosen by the control bits within the 16-bit serial input string. A high-impedance buffer is integrated on the REFINAB and REFINCD terminals to reduce the need for a low source impedance drive to the terminal. REFINAB and REFINCD allow DACs A and B to have a different reference voltage then DACs C and D.

The device, implemented with a CMOS process, is available in 16-terminal SOIC and TSSOP packages. The TLV5604C is characterized for operation from 0°C to 70°C. The TLV5604I is characterized for operation from -40°C to 85°C.



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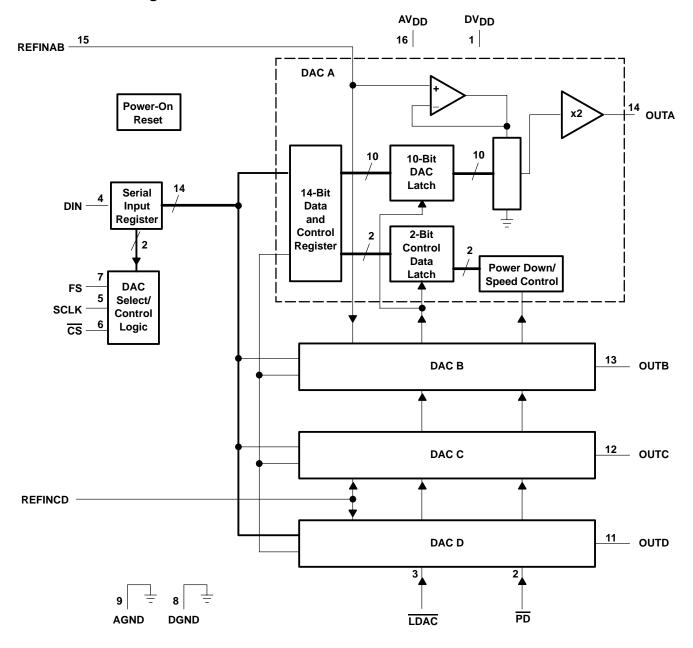


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	PACK	AGE
TA	SOIC (D)	TSSOP (PW)
0°C to 70°C	TLV5604CD	TLV5604CPW
−40°C to 85°C	TLV5604ID	TLV5604IPW

### functional block diagram





# TLV5604 2.7-V TO 5.5-V 10-BIT 3- $\mu$ S QUADRUPLE DIGITAL-TO-ANALOG CONVERTERS WITH POWER DOWN

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### **Terminal Functions**

TERMIN	AL	1/0	DESCRIPTION
NAME	NO.	1/0	DESCRIPTION
AGND	9		Analog ground
$AV_{DD}$	16		Analog supply
CS	6	1	Chip select. This terminal is active low.
DGND	8		Digital ground
DIN	4	1	Serial data input
$DV_{DD}$	1		Digital supply
FS	7	I	Frame sync input. The falling edge of the frame sync pulse indicates the start of a serial data frame shifted out to the TLV5604.
PD	2	I	Power-down pin. Powers down all DACs (overriding their individual power down settings), and all output stages. This terminal is active low.
LDAC	3	I	Load DAC. When the LDAC signal is high, no DAC output updates occur when the input digital data is read into the serial interface. The DAC outputs are only updated when LDAC is low.
REFINAB	15	I	Voltage reference input for DACs A and B.
REFINCD	10	I	Voltage reference input for DACs C and D.
SCLK	5	Ι	Serial Clock input
OUTA	14	0	DAC A output
OUTB	13	0	DAC B output
OUTC	12	0	DAC C output
OUTD	11	0	DAC D output

# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, (DV <sub>DD</sub> , AV <sub>DD</sub> to GND)	7 V
Supply voltage difference, (AV <sub>DD</sub> to DV <sub>DD</sub> )	2.8 V to 2.8 V
Digital input voltage range	0.3 V to DV <sub>DD</sub> + 0.3 V
Reference input voltage range	$-0.3 \text{ V to AV}_{DD}^{-1} + 0.3 \text{ V}$
Operating free-air temperature range, T <sub>A</sub> : TLV5604C	0°C to 70°C
TLV5604I	–40°C to 85°C
Storage temperature range, T <sub>stq</sub>	65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.



# TLV5604 2.7-V TO 5.5-V 10-BIT 3-μS QUADRUPLE DIGITAL-TO-ANALOG CONVERTERS WITH POWER DOWN

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#### recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage AV DV-	5-V supply	4.5	5	5.5	V
ad resistance, R <sub>L</sub> ad capacitance, C <sub>L</sub>	3-V supply	2.7	3	3.3	V
High level digital input valtage V	DV <sub>DD</sub> = 2.7 V	2			V
I night-level digital hiput voltage, VIH	DV <sub>DD</sub> = 5.5 V	2.4			V
Low lovel digital input valtage. Vu	DV <sub>DD</sub> = 2.7 V			0.6	V
Low-level digital input voltage, v[L	DV <sub>DD</sub> = 5.5 V			1	V
Peterones voltage V sta PEEINAR REFINICA terminal	5-V supply (see Note 1)	0	2.048	AV <sub>DD</sub> -1.5	V
Reference voltage, v <sub>ref</sub> to REFINAB, REFINED terminal	3-V supply (see Note 1)	0	1.024	AV <sub>DD</sub> -1.5	V
Load resistance, RL		2	10		kΩ
Load capacitance, CL				100	pF
Serial clock rate, SCLK				20	MHz
Operating free oir temperature	TLV5604C	0		70	°C
oad capacitance, CL	TLV5604I	-40		85	C

NOTE 1: Voltages greater than AVDD/2 will cause output saturation for large DAC codes.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

#### static DAC specifications

	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution			10			bits
	Integral nonlinearity (INL), end pe	oint adjusted	See Note 2			±1	LSB
	Differential nonlinearity (DNL)		See Note 3		±0.1	±1	LSB
EZS	Zero scale error (offset error at z	ero scale)	See Note 4			±12	mV
	Zero scale error temperature coe	efficient	See Note 5		10		ppm/°C
EG	Gain error		See Note 6			±0.6	%of FS voltage
	Gain error temperature coefficier	nt	See Note 7		10		ppm/°C
PSRR	Dower cumply rejection ratio	Zero scale gain	Soo Notoo 8 and 0		-80		dВ
FORK	Power supply rejection ratio	Gain	See Notes 8 and 9		-80		dB

- NOTES: 2. The relative accuracy or integral nonlinearity (INL) sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale excluding the effects of zero code and full-scale errors.
  - 3. The differential nonlinearity (DNL) sometimes referred to as differential error, is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.
  - 4. Zero-scale error is the deviation from zero voltage output when the digital input code is zero.

  - 5. Zero-scale-error temperature coefficient is given by:  $E_{ZS}$  TC =  $[E_{ZS}$  ( $T_{max}$ )  $E_{ZS}$  ( $T_{min}$ )]/ $V_{ref}$  × 10<sup>6</sup>/( $T_{max}$   $T_{min}$ ).

    6. Gain error is the deviation from the ideal output (2 $V_{ref}$  1 LSB) with an output load of 10 k $\Omega$  excluding the effects of the zero-error.
  - 7. Gain temperature coefficient is given by:  $E_G TC = [E_G(T_{max}) E_G(T_{min})]/V_{ref} \times 10^6/(T_{max} T_{min})$ .
  - 8. Zero-scale-error rejection ratio (EZS-RR) is measured by varying the AVDD from 5 ±0.5 V and 3 ±0.3 V dc, and measuring the proportion of this signal imposed on the zero-code output voltage.
  - Gain-error rejection ratio (EG-RR) is measured by varying the  $AV_{DD}$  from 5  $\pm 0.5$  V and 3  $\pm 0.3$  V dc and measuring the proportion of this signal imposed on the full-scale output voltage after subtracting the zero scale change.



# 2.7-V TO 5.5-V 10-BIT 3-μS QUADRUPLE DIGITAL-TO-ANALOG CONVERTERS WITH POWER DOWN

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# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

#### individual DAC output specifications

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VO	Voltage output	$R_L = 10 \text{ k}\Omega$	0		AV <sub>DD</sub> -0.4	V
	Output load regulation accuracy	$R_L = 2 \text{ k}\Omega \text{ vs } 10 \text{ k}\Omega$		0.1	0.25	% of FS voltage

### reference input (REFINAB, REFINCD)

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
٧ <sub>I</sub>	Input voltage range	See Note 10		0		AV <sub>DD</sub> -1.5	V
R <sub>I</sub>	Input resistance				10		MΩ
Cl	Input capacitance				5		pF
	Reference feed through	REFIN = 1 V <sub>pp</sub> at 1 kHz + 1.024 V dc (see Note 11)			-75		dB
	Reference input bandwidth	PEEIN - 0.3 V + 1.034 V do	Slow		0.5		MHz
	Reference input bandwidth	REFIN = $0.2 \text{ V}_{pp} + 1.024 \text{ V dc}$	Fast		1		IVIHZ

NOTES: 10. Reference input voltages greater than  $V_{DD}/2$  will cause output saturation for large DAC codes.

# digital inputs (D0-D11, $\overline{\text{CS}}$ , WEB, $\overline{\text{LDAC}}$ , $\overline{\text{PD}}$ )

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
lіН	High-level digital input current	$V_I = DV_{DD}$			±1	μΑ
I <sub>I</sub> L	Low-level digital input current	V <sub>I</sub> = 0 V			±1	μΑ
Cl	Input capacitance			3	Ö	pF

### power supply

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
		5-V supply, No load, Clock running	Slow		1.4	2.2	mA
		5-V supply, No load, Clock fulllling	Fast		3.5	5.5	IIIA
IDD	Power supply current	2 Vaunning Na load Clask running	Slow		1	1.5	A
		3-V supply, No load, Clock running	Fast		3	4.5	mA
	Power down supply current, See Figure 12				10		nA

<sup>11.</sup> Reference feedthrough is measured at the DAC output with an input code = 000 hex and a  $V_{ref(REFINAB \text{ or }REFINCD)}$  input = 1.024 Vdc + 1  $V_{pp}$  at 1 kHz.

# TLV5604

# 2.7-V TO 5.5-V 10-BIT 3- $\mu$ S QUADRUPLE DIGITAL-TO-ANALOG CONVERTERS WITH POWER DOWN

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# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

#### analog output dynamic performance

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Output slew rate	$C_L = 100 \text{ pF}, R_L = 10 \text{ k}\Omega,$ $V_O = 10\% \text{ to } 90\%,$	Fast		5		V/μs
SIX	Output siew rate	$V_{ref} = 2.048 \text{ V}, 1024 \text{ V}$	Slow		1		V/μs
	Output pottling time	To $\pm 0.5$ LSB, $C_L = 100$ pF,	Fast		2.5	4	
t <sub>S</sub>	Output settling time	$R_L = 10 \text{ k}\Omega$ , See Notes 12 and 14	Slow		8.5	18	μs
	Output potition time, and to and	To $\pm 0.5$ LSB, $C_L = 100$ pF,	Fast		1		
ts(c)	Output settling time, code to code	$R_L = 10 \text{ k}\Omega$ , See Note 13	Slow		2		μs
	Glitch energy	Code transition from 7FF to 800			10		nV-sec
SNR	Signal-to-noise ratio	Sinewave generated by DAC,			68		
S/(N+D)	Signal to noise + distortion	Reference voltage = 1.024 at 3 V and 2. $f_S = 400 \text{ KSPS}$ ,	.048 at 5 V,		65		
THD	Total harmonic Distortion	$f_{OUT} = 1.1 \text{ kHz sinewave},$ $C_{I} = 100 \text{ pF},$ $R_{I} = 10 \text{ k}\Omega,$			-68		dB
SFDR	Spurious free dynamic range	BW = 20 kHz			70		

NOTES: 12. Settling time is the time for the output signal to remain within  $\pm$  0.5LSB of the final measured value for a digital input code change of 020 hex to 3FF hex or 3FF hex to 020 hex.



<sup>13.</sup> Settling time is the time for the output signal to remain within  $\pm$  0.5LSB of the final measured value for a digital input code change of one count, 1FF hex to 200 hex.

<sup>14.</sup> Limits are ensured by design and characterization, but are not production tested.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

### digital input timing requirements

		MIN	NOM	MAX	UNIT
t <sub>su(CS-FS)</sub>	Setup time, CS low before FS↓	10			ns
tsu(FS–CK)	Setup time, FS low before first negative SCLK edge	8			ns
tsu(C16–FS)	Setup time, sixteenth negative SCLK edge after FS low on which bit D0 is sampled before rising edge of FS	10			ns
tsu(C16–CS)	Setup time. The first positive SCLK edge after D0 is sampled before $\overline{CS}$ rising edge. If FS is used instead of the SCLK positive edge to update the DAC, then the setup time is between the FS rising edge and $\overline{CS}$ rising edge.	10			ns
t <sub>wH</sub>	Pulse duration, SCLK high	25			ns
t <sub>wL</sub>	Pulse duration, SCLK low	25			ns
t <sub>su(D)</sub>	Setup time, data ready before SCLK falling edge	8			ns
t <sub>h(D)</sub>	Hold time, data held valid after SCLK falling edge	5			ns
twH(FS)	Pulse duration, FS high	20			ns

### PARAMETER MEASUREMENT INFORMATION

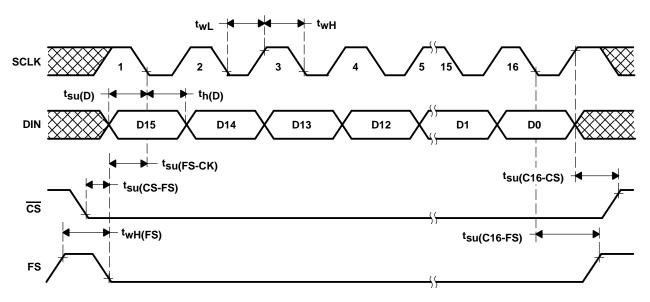


Figure 1. Timing Diagram

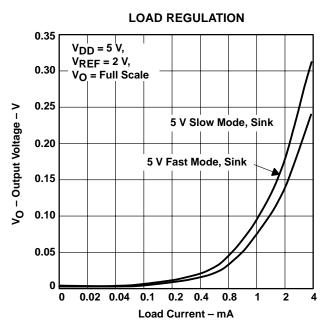


Figure 2

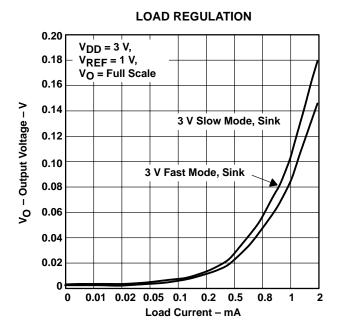


Figure 3

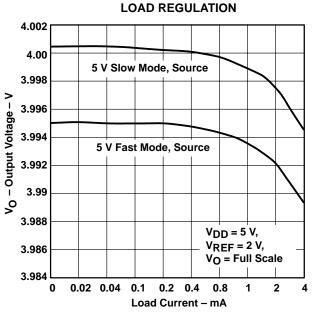


Figure 4

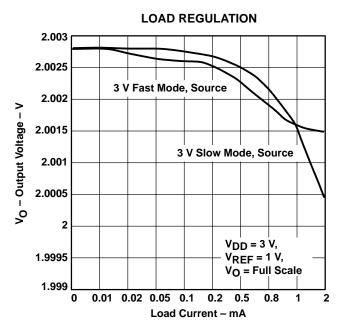
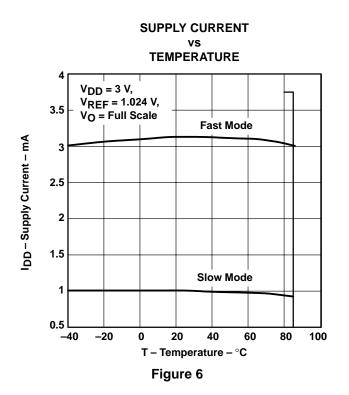
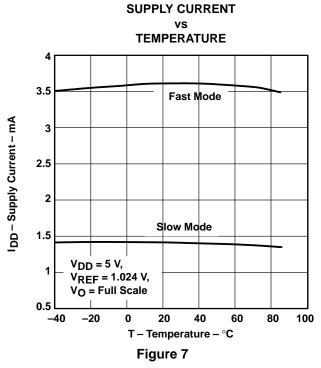
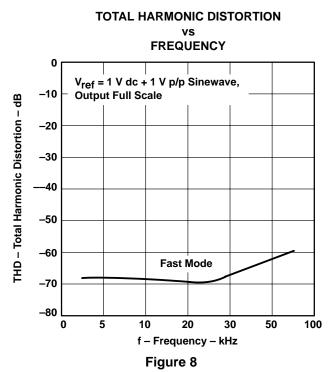


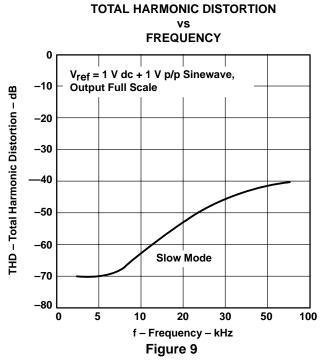
Figure 5





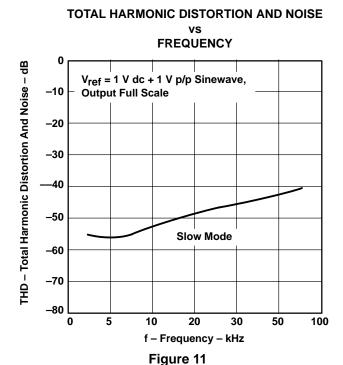




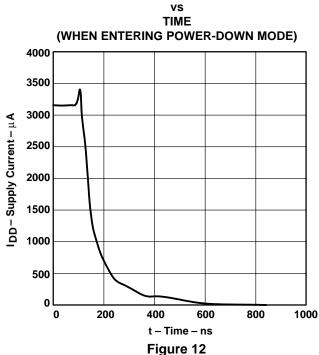


## TOTAL HARMONIC DISTORTION AND NOISE **FREQUENCY** THD - Total Harmonic Distortion And Noise - dB $V_{ref} = 1 V dc + 1 V p/p Sinewave,$ Output Full Scale -10 -20 -30 -40 -50 **Fast Mode** -60 -70 -80 5 10 20 30 50 100 f - Frequency - kHz

Figure 10



# SUPPLY CURRENT





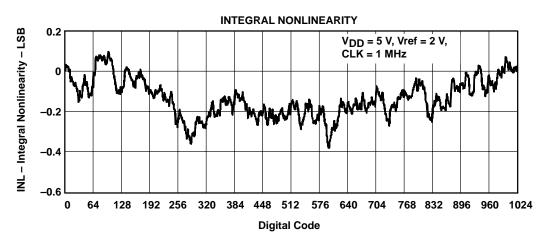


Figure 13

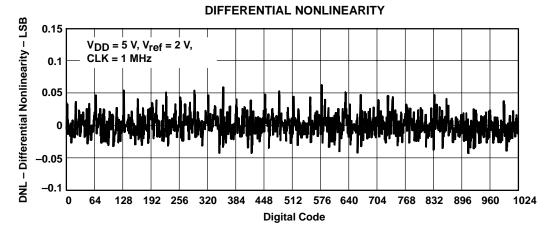


Figure 14



#### general function

The TLV5604 is a 10-bit single supply DAC based on a resistor string architecture. The device consists of a serial interface, speed and power-down control logic, a reference input buffer, a resistor string, and a rail-to-rail output buffer.

The output voltage (full scale determined by external reference) is given by:

2 REF 
$$\frac{\text{CODE}}{2^n}$$
 [V]

Where REF is the reference voltage and CODE is the digital input value within the range of  $0_{10}$  to  $2^n$ –1, where n=10 (bits). The 16-bit data word, consisting of control bits and the new DAC value, is illustrated in the *data* format section. A power-on reset initially resets the internal latches to a defined state (all bits zero).

#### serial interface

Explanation of data transfer: First, the device has to be enabled with  $\overline{CS}$  set to low. Then, a falling edge of FS starts shifting the data bit-per-bit (starting with the MSB) to the internal register on the falling edges of SCLK. After 16 bits have been transferred or FS rises, the content of the shift register is moved to the DAC latch, which updates the voltage output to the new level.

The serial interface of the TLV5604 can be used in two basic modes:

- Four wire (with chip select)
- Three wire (without chip select)

Using chip select (four wire mode), it is possible to have more than one device connected to the serial port of the data source (DSP or microcontroller). The interface is compatible with the TMS320 family. Figure 15 shows an example with two TLV5604s connected directly to a TMS320 DSP.

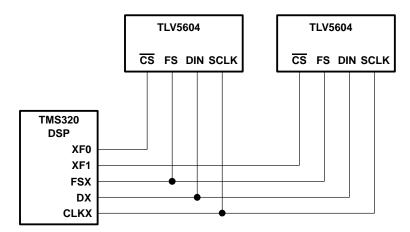
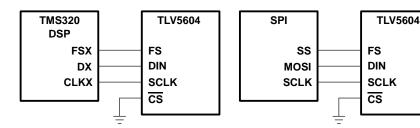


Figure 15. TMS320 Interface



#### serial interface (continued)

If there is no need to have more than one device on the serial bus, then  $\overline{CS}$  can be tied low. Figure 16 shows an example of how to connect the TLV5604 to a TMS320, SPI, or Microwire port using only three pins.



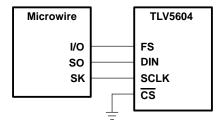


Figure 16. Three-Wire Interface

Notes on SPI and Microwire: Before the controller starts the data transfer, the software has to generate a falling edge on the I/O pin connected to FS. If the word width is 8 bits (SPI and Microwire), two write operations must be performed to program the TLV5604. After the write operation(s), the DAC output is updated automatically on the next positive clock edge following the sixteenth falling clock edge.

#### serial clock frequency and update rate

The maximum serial clock frequency is given by:

$$f_{SCLKmax} = \frac{1}{t_{wH(min)} + t_{wL(min)}} = 20 \text{ MHz}$$

The maximum update rate is:

$$f_{UPDATEmax} = \frac{1}{16 \left(t_{wH(min)} + t_{wL(min)}\right)} = 1.25 \text{ MHz}$$

Note that the maximum update rate is a theoretical value for the serial interface since the settling time of the TLV5604 has to be considered also.

#### data format

The 16-bit data word for the TLV5604 consists of two parts:

• Control bits (D15...D12)

• New DAC value (D11 . . . D0)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
A1	A0	PWR	SPD		New DAC value (10 bits)									Х	Х

X: don't care

SPD: Speed control bit.  $1 \rightarrow \text{fast mode}$   $0 \rightarrow \text{slow mode}$  PWR: Power control bit.  $1 \rightarrow \text{power down}$   $0 \rightarrow \text{normal operation}$ 



In power down mode, all amplifiers within the TLV5604 are disabled. A particular DAC (A, B, C, D) of the TLV5604 is selected by A1 and A0 within the input word.

A1	A0	DAC
0	0	А
0	1	В
1	0	С
1	1	D

#### TLV5604 interfaced to TMS320C203 DSP

#### Hardware interfacing

Figure 17 shows an example of how to connect the TLV5604 to a TMS320C203 DSP. The serial port is configured in burst mode, with FSX generated by the TMS320C203 to provide the Frame Sync (FS) input to the TLV5604. Data is transmitted on the DX line, with the serial clock input on the CLKX line. The general-purpose input/output port bits IO0 and IO1 are used to generate the Chip Select ( $\overline{\text{CS}}$ ) and DAC Latch Update ( $\overline{\text{LDAC}}$ ) inputs to the TLV5604. The active low Power Down ( $\overline{\text{PD}}$ ) is pulled high all the time to ensure the DACs are enabled.

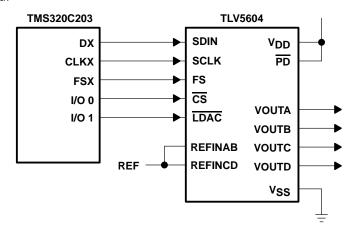


Figure 17. TLV5604 Interfaced with TMS320C203

#### **Software**

The application example generates a differential in-phase (sine) signal between the VOUTA and VOUTB pins, and it is quadrature (cosine) signal as the differential signal between VOUTC and VOUTD.

The on-chip timer is used to generate interrupts at a fixed frequency. The related interrupt service routine pulses LDAC low to update all 4 DACs simultaneously, then fetches and writes the next sample to all 4 DACs. The samples are stored in a look-up table, which describes two full periods of a sine wave.

The synchronous serial port of the DSP is used in burst mode. In this mode, the processor generates an FS pulse preceding the MSB of every data word. If multiple, contiguous words are transmitted, a violation of the tsu(C16-FS) timing requirement will occur. To avoid this, the program waits until the transmission of the previous word has been completed.



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```
; Processor: TMS320C203 runnning at 40 MHz;
; Description:
; This program generates a differential in-phase (sine) on (OUTA-OUTB) and it's
; quadrature (cosine) as a differential signal on (OUTC-OUTD).
; The DAC codes for the signal samples are stored as a table of 64 12-bit values,
; describing 2 periods of a sine function. A rolling pointer is used to address the
; table location in the first period of this waveform, from which the DAC A samples are ; read. The samples for the other 3 DACs are read at an offset to this rolling pointer:
; DAC
        Function Offset from rolling pointer;
  Α
        sine
                          0
                          16
  В
        inverse sine
 C
        cosine
        inverse cosine
; The on-chip timer is used to generate interrupts at a fixed rate. The interrupt
; service routine first pulses LDAC low to update all DACs simultaneously with the
; values which were written to them in the previous interrupt. Then all 4 DAC values are
; fetched and written out through the synchronous serial interface. Finally, the
; rolling pointer is incremented to address the next sample, ready for the next
; interrupt.
; © 1998, Texas Instruments Incorporated
      -----;
; -----I/O and memory mapped regs ------
           .include "regs.asm"
; -----jump vectors-----
                                _____
                 0h
           .ps
           b
                 start
           b
                 int.1
           b
                 int23
           b
                timer_isr
         ------ variables ------
temp
             .equ
                        0060h
               .equ
.equ
                        0061
r_ptr
iosr_stat
                        0062h
DACa_ptr
                        0063h
                 .equ
DACb_ptr
                        0064h
DACc_ptr
                        0065h
                 .equ
DACd_ptr
                      0066h
                 .equ
;----- constants ------
; DAC control bits to be OR'ed onto data
; all fast mode
DACa_control
                 .equ
                        01000h
                 .equ
DACb_control
                        05000h
                      09000h
                 .equ
DACc_control
                 .equ 0d000h
DACd_control
;----- tables -----
     .ds
            02000h
sinevals
      .word
              00800h
              0097Ch
      .word
              00AE9h
      .word
      .word
              00C3Ah
      .word
              00D61h
              00E53h
      .word
      .word
              00F07h
              00F76h
      .word
              00F9Ch
      .word
      .word
              00F76h
              00F07h
      .word
              00E53h
      .word
              00D61h
      .word
              00C3Ah
      .word
```



# 2.7-V TO 5.5-V 10-BIT 3- $\mu$ S QUADRUPLE DIGITAL-TO-ANALOG CONVERTERS WITH POWER DOWN

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```
.word
                 00AE9h
      .word
                 0097Ch
                00800h
       .word
       .word
                00684h
                00517h
      .word
                003C6h
       .word
       .word
                 0029Fh
      .word
                001ADh
      .word
                 000F9h
       .word
                0008Ah
                00064h
       .word
                0008Ah
                000F9h
      .word
       .word
                001ADh
                0029Fh
      .word
      .word
                003C6h
       .word
                00517h
      .word
                00684h
      .word
                00800h
                0097Ch
       .word
       .word
                00AE9h
      .word
                00C3Ah
                00D61h
       .word
       .word
                00E53h
      .word
                00F07h
       .word
                00F76h
       .word
                 00F9Ch
                00F76h
      .word
       .word
                00F07h
       .word
                00E53h
       .word
                00D61h
                 00C3Ah
      .word
                00AE9h
       .word
       .word
                0097Ch
      .word
                00800h
      .word
                00684h
       .word
                00517h
      .word
                003C6h
      .word
                0029Fh
                 001ADh
       .word
                000F9h
      .word
      .word
                0008Ah
       .word
                00064h
       .word
                0008Ah
      .word
                000F9h
      .word
                001ADh
       .word
                0029Fh
      .word
                003C6h
      .word
                00517h
      .word
; Main Program
      .ps 1000h
      .entry
start
; disable interrupts
;-----
      setc INTM ; disable maskable interrupts
splk #0ffffh, IFR ; clear all interrupts
splk #0004h, IMR ; timer interrupts unmasked
```



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```
set up the timer
 timer period set by values in PRD and TDDR
  period = (CLKOUT1 period) \times (1+PRD) \times (1+TDDR)
  examples for TMS320C203 with 40 MHz main clock
                     PRD
; Timer rate
              TDDR
   80 kHz
              9
                       24 (18h)
   50 kHz
                       39 (27h)
                0018h
prd_val.equ
tcr_val.equ 0029h
     splk
           #0000h, temp
                       ; clear timer
           temp, TIM
           #prd_val, temp  ; set PRD
     splk
     out
           temp, PRD
           #tcr_val, temp ; set TDDR, and TRB=1 for auto-reload
     splk
          temp, TCR
     out
; Configure IOO/1 as outputs to be :
; IOO CS

    and set high

; IO1 LDAC
          - and set high
;------
          temp, ASPCR ; configure as output
          temp
     lacl
     or
           #0003h
     sacl
           temp
           temp, ASPCR
     out.
     in
           temp, IOSR ; set them high
           temp
     lacl
           #0003h
     or
     sacl
           temp
          temp, IOSR
     out
; set up serial port for
; SSPCR.TXM=1
             Transmit mode - generate FSX
; SSPCR.MCM=1
             Clock mode - internal clock source
; SSPCR.FSM=1 Burst mode
     splk #0000Eh, temp
           temp, SSPCR ; reset transmitter
     out
     splk
           #0002Eh, temp
          temp, SSPCR
     out
; reset the rolling pointer
;-----
    lacl #000h saclr_ptr
; enable interrupts
;------
    clrc INTM
; enable maskable interrupts
; loop forever!
next idle
                  ;wait for interrupt
       b
            next
; all else fails stop here
done b done ; hang there
```



# 2.7-V TO 5.5-V 10-BIT 3-μS QUADRUPLE DIGITAL-TO-ANALOG CONVERTERS WITH POWER DOWN

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```
; Interrupt Service Routines
int1    ret    ; do nothing and return
int23    ret    ; do nothing and return
timer_isr:
             iosr_stat, IOSR ; store IOSR value into variable space
      in
      #0FFFDh
      and
                           ; reset IO1 - LDAC low
      sacl
            temp
            temp, IOSR ;
      out
      or
            #0002h
                          ; set IO1 - LDAC high
      sacl temp
            temp, IOSR
      out
                         ; reset IOO - CS low
            #0FFFEh
      and
      sacl temp
      out
            temp, IOSR
      lacl r_ptr ; load rolling pointer to accumulator add #sinevals ; add pointer to table start sacl DACa_ptr ; to get a pointer for next DAC a sample
      add #08h
                            ; add 8 to get to DAC C pointer
      sacl DACc_ptr
      add #08h
                            ; add 8 to get to DAC B pointer
      sacl DACb_ptr
      add
                            ; add 8 to get to DAC D pointer
           DACd_ptr
      sacl
            *,ar0
      mar
                            ; set ar0 as current AR
      ; DAC A
               ar0, DACa_ptr; ar0 points to DAC a sample
      lar
               * ; get DAC a sample into accumulator
      lacl
               #DACa_control; OR in DAC A control bits
               temp
      sacl
                           ;
              temp, SDTR ; send data
; We must wait for transmission to complete before writing next word to the SDTR.
; TLV5604 interface does not allow the use of burst mode with the full packet rate, as
; we need a CLKX -ve edge to clock in last bit before FS goes high again, to allow SPI
; compatibility.
           #016h ; wait long enough for this configuration
                            ; of MCLK/CLKOUT1 rate
      nop
      ; DAC B
      lar
                ar0, DACb_ptr; ar0 points to DAC a sample
                * ; get DAC a sample into accumulator
      lacl
                #DACb_control; OR in DAC B control bits
               temp, SDTR ; send data
               #016h ; wait long enough for this configuration
      rpt
                            ; of MCLK/CLKOUT1 rate
      nop
```



# 2.7-V TO 5.5-V 10-BIT 3-μS QUADRUPLE DIGITAL-TO-ANALOG CONVERTERS WITH POWER DOWN

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```
; DAC C
      lar
                ar0, DACc_ptr; ar0 points to DAC a sample
      lacl
                            ; get DAC a sample into accumulator
                #DACc_control; OR in DAC C control bits
      or
      sacl
                temp
                           ; send data
               temp, SDTR
      out
               #016h
                           ; wait long enough for this configuration
      rpt
                            ; of MCLK/CLKOUT1 rate
      nop
   ; DAC D
  lar
               ar0, DACd_ptr; ar0 points to DAC a sample
  lacl
                * ; get DAC a sample into accumulator
                #DACd_control; OR in DAC D control bits
  or
  sacl
               temp
                           ; send data
   out
               temp, SDTR
                           ; load rolling pointer to accumulator
   lacl
               r_ptr
                            ; increment rolling pointer
  add
               #1h
               #001Fh
  and
                           ; count 0-31 then wrap back round
                           ; store rolling pointer
  sacl
               r_ptr
                            ; wait long enough for this configuration
               #016h
  rpt
                            ; of MCLK/CLKOUT1 rate
   ; now take CS high again
  lacl
              iosr_stat
                           ; load acc with iosr status
                           ; set IOO - CS high
  or
               #0001h
  sacl
               temp
               temp, IOSR
                           ;
  out.
                            ; re-enable interrupts
               intm
  clrc
  ret
                            ; return from interrupt
.end
```



### TLV5604 interfaced to MCS®51 microcontroller

#### hardware interfacing

Figure 18 shows an example of how to connect the TLV5604 to an MCS $^{\circledR}$ 51 Microcontroller. The serial DAC input data and external control signals are sent via I/O Port 3 of the controller. The serial data is sent on the RxD line, with the serial clock output on the  $\overline{\text{TxD}}$  line. Port 3 bits 3, 4, and 5 are configured as outputs to provide the DAC latch update ( $\overline{\text{LDAC}}$ ), chip select ( $\overline{\text{CS}}$ ) and frame sync (FS) signals for the TLV5604. The active low power down pin ( $\overline{\text{PD}}$ ) of the TLV5604 is pulled high to ensure that the DACs are enabled.

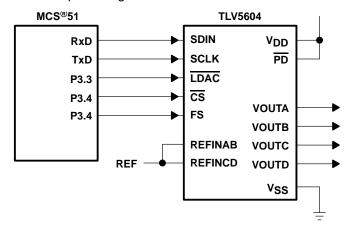


Figure 18. TLV5604 Interfaced with MCS®51

#### software

The example is the same as for the TMS320C203 in this datasheet, but adapted for a MCS®51 controller. It generates a differential in-phase (sine) signal between the VOUTA and VOUTB pins, and it's quadrature (cosine) signal as the differential signal between VOUTC and VOUTD.

The on-chip timer is used to generate interrupts at a fixed frequency. The related interrupt service routine pulses LDAC low to update all 4 DACs simultaneously, then fetches and writes the next sample to all 4 DACs. The samples are stored as a look-up table, which describes one full period of a sine wave.

The serial port of the controller is used in Mode 0, which transmits 8 bits of data on RxD, accompanied by a synchronous clock on TxD. Two writes concatenated together are required to write a complete word to the TLV5604. The  $\overline{\text{CS}}$  and FS signals are provided in the required fashion through control of IO port 3, which has bit addressable outputs.

MCS is a registered trademark of Intel Corporation.



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```
; Processor: 80C51
; Description:
; This program generates a differential in-phase (sine) on (OUTA-OUTB) and it's
 quadrature (cosine) as a differential signal on (OUTC-OUTD).
 © 1998, Texas Instruments Incorporated
  NAME
           GENIO
           SEGMENT
                    CODE
  MAIN
           SEGMENT CODE
   ISR
  SINTBL
           SEGMENT
                    CODE
                    DATA
   VAR1
           SEGMENT
         SEGMENT IDATA
  STACK
; Code start at address 0, jump to start
                        _____
          CSEG AT 0
           LJMP start
                         ; Execution starts at address 0 on power-up.
;-----
; Code in the timerO interrupt vector
CSEG AT 0BH
           LJMP timer0isr; Jump vector for timer 0 interrupt is 000Bh
; Global variables need space allocated
           RSEG VAR1
                 DS 1
Temp_ptr:
rolling_ptr:
; Interrupt service routine for timer 0 interrupts
           RSEG ISR
timer0isr:
            PUSH
                 PSW
            PUSH
                 ACC
            CLR
                  TNT1
                          ; pulse LDAC low
                          ; to latch all 4 previous values at the same time
            SETB
                 TNT1
                          ; 1st thing done in timer isr => fixed period
            CLR
                 TΩ
                           ; set CS low
   ; The signal to be output on each DAC is a sine function.
   ; One cycle of a sine wave is held in a table @ sinevals as 32 samples of msb,
    lsb pairs (64 bytes). We have one pointer which rolls round this table,
   ; rolling_ptr, incrementing by 2 bytes (1 sample) on each interrupt (at the end of
   ; this routine).
   ; The DAC samples are read at an offset to this rolling pointer:
   ; DAC Function Offset from rolling_ptr
     Α
         sine
                           0
     В
         inverse sine
                           32
     C
         cosine
                         48
        inverse cosine
     D
                       ; set DPTR to the start of the call; R7 holds the pointer into the sine table
  MOV
         DPTR, #sinevals
                          ; set DPTR to the start of the table of sine signal values
        R7,rolling_ptr
  MOV
  VOM
         A,R7
                          ; get DAC A msb
  MOVC
        A,@A+DPTR
                          ; msb of DAC A is in the ACC
                          ; transmit it - set FS low
         т1
   CLR
  MOV
         SBUF,A
                          ; send it out the serial port
                          ; increment the pointer in R7 ; to get the next byte from the table
   INC
        R7
  MOV
         A,R7
                          ; which is the lsb of this sample, now in ACC
  MOVC
       A,@A+DPTR
```



# 2.7-V TO 5.5-V 10-BIT 3- $\mu$ S QUADRUPLE DIGITAL-TO-ANALOG CONVERTERS WITH POWER DOWN

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```
A_MSB_TX:
          TI,A_MSB_TX ; wait for transmit to complete
   JNB
   CLR
          TΙ
                       ; clear for new transmit
   MOV
          SBUF,A
                       ; and send out the 1sb of DAC A
   ; DAC C next
   ; DAC C codes should be taken from 16 bytes (8 samples) further on in the sine table
   ; - this gives a cosine function  
                  ; pointer in R7
   VOM
          A,R7
          A,#0FH
                       ; add 15 - already done one INC
   ADD
                      ; wrap back round to 0 if > 64
   ANL
          A,#03FH
   MOV
          R7,A
                      ; pointer back in R7
        A,@A+DPTR
                      ; get DAC C msb from the table
   MOVC
                      ; set control bits to DAC C address
   ORL
         A,#01H
A_LSB_TX:
   JNB
          TI, A_LSB_TX ; wait for DAC A lsb transmit to complete
         T1
   SETB
                       ; toggle FS
   CLR
          т1
   CLR
          TТ
                       ; clear for new transmit
   VOM
          SBUF,A
                      ; and send out the msb of DAC C
   INC
                       ; increment the pointer in R7
         A,R7 ; to get the next byte from the table
A,@A+DPTR ; which is the lsb of this sample, now in ACC
   VOM
   MOVC
C_MSB_TX:
   JNB
          TI,C_MSB_TX ; wait for transmit to complete
                  ; clear for new transmit
   CLR
          TΙ
   MOV
          SBUF, A
                       ; and send out the 1sb of DAC C
   ; DAC B next
   ; DAC B codes should be taken from 16 bytes (8 samples) further on
   ; in the sine table - this gives an inverted sine function
   MOV
          A,R7
                       ; pointer in R7
          A,#OFH
                       ; add 15 - already done one INC
   ADD
                      ; wrap back round to 0 if > 64
          A,#03FH
   ANL
   MOV
         R7,A
                       ; pointer back in R7
   MOVC
         A,@A+DPTR
                      ; get DAC B msb from the table
   ORL
          A,#02H
                       ; set control bits to DAC B address
C_LSB_TX:
          TI,C_LSB_TX
                              ; wait for DAC C lsb transmit to complete
   JNB
   SETB
          Т1
                              ; toggle FS
   CLR
          т1
   CLR
                              ; clear for new transmit
   MOV
          SBUF,A
                              ; and send out the msb of DAC B
                              ; get DAC B LSB
   INC
          R7
                              ; increment the pointer in R7
   VOM
          A,R7
                              ; to get the next byte from the table
   MOVC
         A,@A+DPTR
                              ; which is the lsb of this sample, now in ACC
B_MSB_TX:
          TI,B_MSB_TX
   JNB
                              ; wait for transmit to complete
                              ; clear for new transmit
   CLR
   MOV
          SBUF,A
                              ; and send out the 1sb of DAC B
```



### TLV5604 2.7-V TO 5.5-V 10-BIT 3-μS QUADRUPLE DIGITAL-TO-ANALOG CONVERTERS WITH POWER DOWN

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```
; DAC D next
   ; DAC D codes should be taken from 16 bytes (8 samples) further on in the sine table
   ; - this gives an inverted cosine function
   MOV
         A,R7
                           ; pointer in R7
   ADD
         A,#0FH
                            ; add 15 - already done one INC
   ANT
         A,#03FH
                            ; wrap back round to 0 if > 64
   MOV
         R7,A
                            ; pointer back in R7
   MOVC A,@A+DPTR
                            ; get DAC D msb from the table
         A,#03H
                            ; set control bits to DAC D address
   ORT
B_LSB_TX:
                            ; wait for DAC B lsb transmit to complete
   JNB
         TI,B_LSB_TX
   SETB T1
                            ; toggle FS
   CLR
         т1
   CLR
         ΤТ
                            ; clear for new transmit
       SBUF,A
                            ; and send out the msb of DAC D
   MOV
   TNC
                            ; increment the pointer in R7
   MOV
         A,R7
                            ; to get the next byte from the table
   MOVC A,@A+DPTR
                            ; which is the lsb of this sample, now in ACC
D_MSB_TX:
   JNB TI,D_MSB_TX
                           ; wait for transmit to complete
   CLR
                            ; clear for new transmit
         TI
   MOV
         SBUF,A
                            ; and send out the 1sb of DAC D
   ; increment the rolling pointer to point to the next sample
   ; ready for the next interrupt
        A,rolling_ptr
                          ; add 2 to the rolling pointer
        A,#02H
   ADD
                           ; wrap back round to 0 if > 64
   ANL
        A,#03FH
       rolling_ptr,A
   MOV
                           ; store in memory again
D_LSB_TX:
   JNBTI,D_LSB_TX
                            ; wait for DAC D lsb transmit to complete
   CLR
       TI
                            ; clear for next transmit
   SETB T1
                            ; FS high
   SETB T0
                            ; CS high
   POP
         ACC
   POP
         PSW
; Stack needs definition
      RSEG STACK
      DS 10h
                           ; 16 Byte Stack!
```



# 2.7-V TO 5.5-V 10-BIT 3- $\mu$ S QUADRUPLE DIGITAL-TO-ANALOG CONVERTERS WITH POWER DOWN

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```
; Main program code
     RSEG MAIN
start:
     MOV
          SP,#STACK-1 ; first set Stack Pointer
     CLR
                         ; set serial port 0 to mode 0
           SCON, A
     MOV
                         ; set timer 0 to mode 2 - auto-reload
           TMOD, #02H
     VOM
           TH0, #038H
                         ; set THO for 5 kHs interrupts
                          ; set LDAC = 1
     SETB INT1
          T1
     SETB
                          ; set FS = 1
     SETB
                          ; set CS = 1
                      ; enable timer 0 interrupts
     SETB
           ET0
     SETB
                          ; enable all interrupts
           rolling_ptr,A ; set rolling pointer to 0
     SETB TR0
                         ; start timer 0
always:
     JMP always
                       ; while(1) !
; Table of 32 sine wave samples used as DAC data
;------
     RSEG SINTBL
sinevals:
             01000H
     DW
     DW
              0903EH
              05097H
     DW
     DW
              0305CH
     DW
              0в086н
     DW
              070CAH
             OFOEOH
     DW
     DW
              0F06EH
     DW
              0F039H
     DW
              0F06EH
     DW
              OFOEOH
     DW
              070CAH
              0B086H
     DW
     DW
              0305CH
     DW
              05097H
              0903EH
     DW
     DW
              01000H
     DW
              06021H
     DW
              0A0E8H
     DW
              0C063H
              040F9H
     DW
     DW
              080B5H
              0009FH
     DW
     DW
              00051H
     DW
              00026H
     DW
              00051H
     DW
              0009FH
     DW
              080B5H
     DW
              040F9H
     DW
              0C063H
     DW
              0A0E8H
     DW
              06021H
END
```



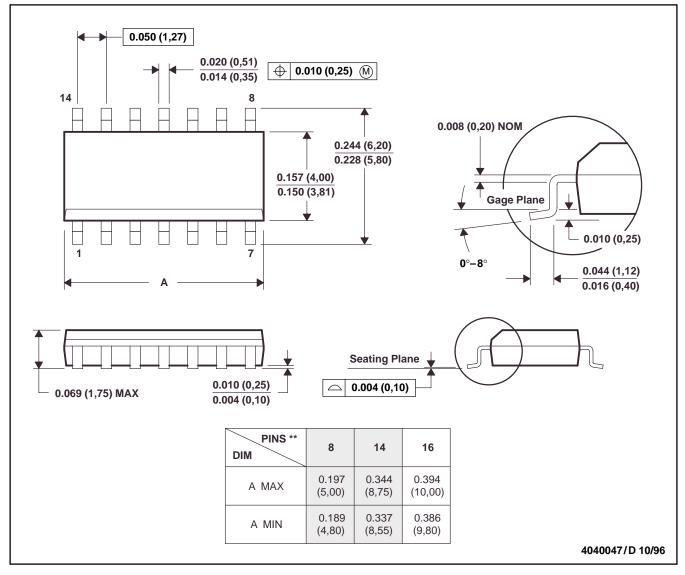
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#### MECHANICAL DATA

### D (R-PDSO-G\*\*)

#### 14 PIN SHOWN

#### PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).

D. Falls within JEDEC MS-012

# 2.7-V TO 5.5-V 10-BIT 3- $\mu$ S QUADRUPLE DIGITAL-TO-ANALOG CONVERTERS WITH POWER DOWN

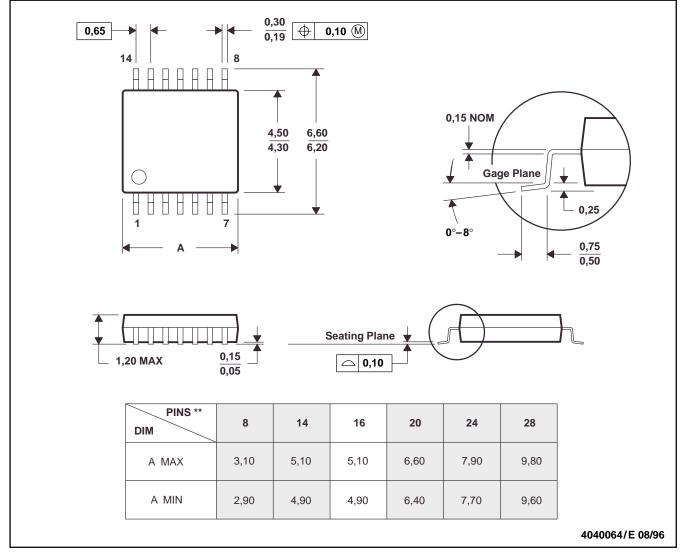
SLAS176B - DECEMBER 1997 - REVISED JULY 2002

#### **MECHANICAL DATA**

### PW (R-PDSO-G\*\*)

#### 14 PIN SHOWN

#### PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

#### PACKAGE OPTION ADDENDUM

www.ti.com 27-Aug-2009

#### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp (3)
TLV5604CD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV5604CDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV5604CDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV5604CDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV5604CPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV5604CPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV5604CPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV5604CPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV5604ID	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV5604IDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV5604IPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV5604IPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV5604IPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV5604IPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is



# **PACKAGE OPTION ADDENDUM**

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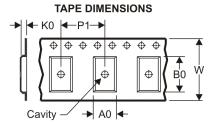
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# PACKAGE MATERIALS INFORMATION

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### TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

All differsions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV5604CDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TLV5604CPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV5604IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

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\*All dimensions are nominal

,								
	Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
	TLV5604CDR	SOIC	D	16	2500	346.0	346.0	33.0
	TLV5604CPWR	TSSOP	PW	16	2000	346.0	346.0	29.0
	TLV5604IPWR	TSSOP	PW	16	2000	346.0	346.0	29.0

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